Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

19-5361; Rev 7/11

TERIDIAN SEMICONDUCTOR CORP.

A Maxim Integrated Products Brand

71M6515H Energy Meter IC

DATA SHEET

JULY 2011

GENERAL DESCRIPTION

The 71M6515H is a high-accuracy analog front-end (AFE) IC that provides measurements for 3-quadrant 3-phase metering. The combination of a 21-bit sigma-delta A/D converter with a six-input analog front-end, a thermally compensated high-precision reference, and a compute engine results in high accuracy and wide dynamic range. Our Single Converter Technology® reduces cross talk and cost. This IC also provides RTC and battery backup for time-of-use (TOU) metering.

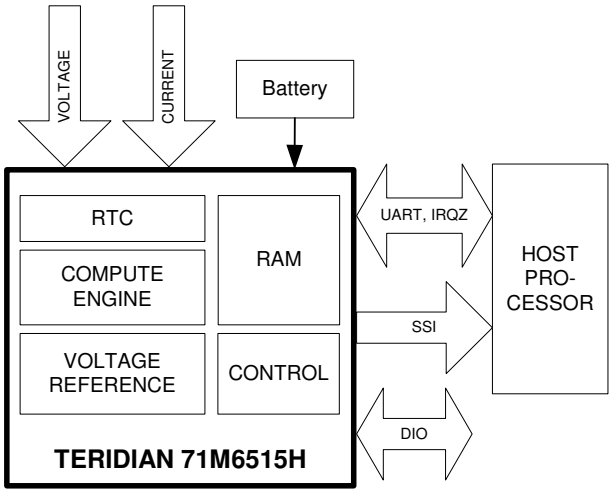


Figure 1: Meter Block Diagram

As shown in the block diagram (Figure 1), the host processor communicates with the 71M6515H through a UART interface using the programmable IRQZ interrupt. The 71M6515H calculates and accumulates meter measurements for each accumulation interval. A high-speed synchronous serial port (SSI) is provided to facilitate high-end metering. Integrated rectifying functions on the battery-backup circuit enable minimal external component usage and minimum back-up current. Also, eight multipurpose pins are provided for control of peripherals.

Single Converter Technology is a registered trademark of Maxim Integrated Products, Inc.

FEATURES

High Accuracy

- < 0.1% Wh accuracy over 2000:1 range
- Exceeds IEC 62053/ANSIC 12.20 specifications
- Up to 10ppm/°C precision ultra-stable voltage reference
- Single Converter Technology reduces cross talk and power consumption
- Six sensor inputs—referenced to V3P3
- Compatible with CTs, resistive shunts and Rogowski Coil sensors
- Digital temperature compensation
- Sag detection
- Measures Wh, VARh, VAh, Vrms, Irms, V-to-V phase and load angle on each phase
- Four-quadrant metering.
- Four low-jitter pulse outputs from selectable measurements
- Four pulse count registers
- Selectable default status for pulse pins
- Same calibration data for 46Hz to 64Hz line frequency
- Broad CT phase compensation (±7deg)

Battery Backup

- Powers real-time clock during power supply outage
- Compatible with Li-ion, NiCd, or super capacitor
- Battery backup current 2µA typical at 25°C

External Data Interface

- UART control interface, two selectable data rates
- 8 general-purpose I/O pins with alarm capability
- 5 or 10MHz selectable high-speed synchronous serial output for DSP interface
- IRQ output signal for alarms and end of measurement intervals
- Alarms on voltage sag, overvoltage, overcurrent

Low System Cost

- Power consumption 30mW at 3.3V typical
- Real-time clock with temperature compensation
- Built-in power-fault detection
- Single 32kHz crystal time base
- Single-supply operation (3.3V)
- 64-lead LQFP package

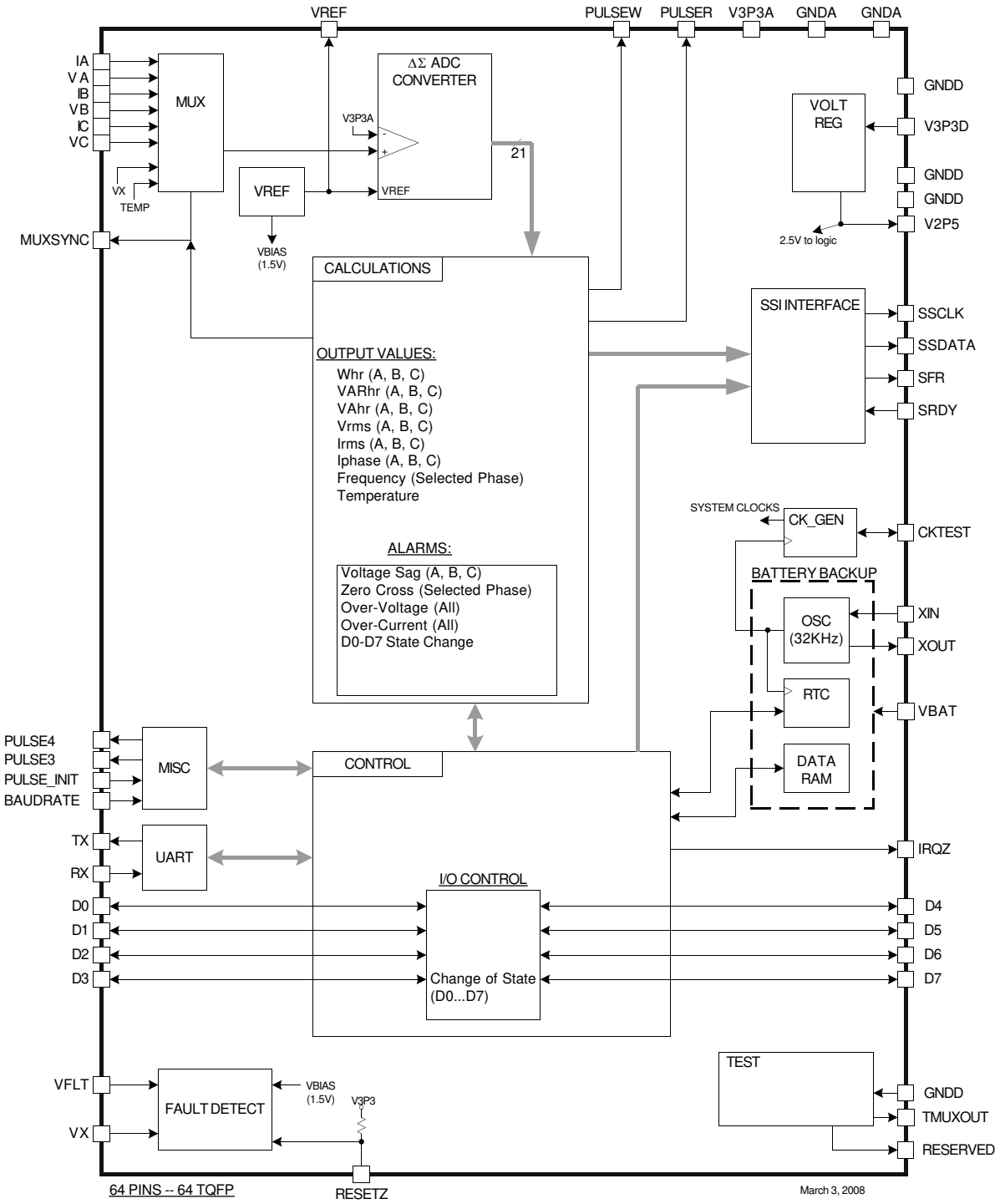


Figure 2: IC Functional Block Diagram

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supplies and Ground Pins:	
V3P3D, V3P3A	–0.5V to 4.6V
|V3P3D – V3P3A|	0V to 0.5V
VBAT	-0.5V to 4.6V
GNDD	-0.5V to +0.5V
Analog Output Pins:	
VREF	-1mA to 1mA, -0.5V to V3P3A+0.5V
V2P5	-1mA to 1mA, -0.5 to 3.0V
Analog Input Pins:	
IA, VA, IB, VB, IC, VC	-0.5V to V3P3A+1.0V
VFLT, VX	-0.5V to V3P3A+0.5V
XIN, XOUT	-0.5V to 3.0V
Digital Input Pins:	
RX	-0.5V to 3.6V
D0…D7	-0.5V to 6V
All other pins	-0.5V to V3P3D+0.5V
Operating junction temperature (peak, 100ms)	140 °C
Operating junction temperature (continuous)	125 °C
Storage temperature	–45 °C to 165 °C
Solder temperature – 10 second duration	250 °C
ESD Stress	
Pins IA, VA, IB, VB, IC, VC, RX, TX	6kV
All other pins	2kV

Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GNDA.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
3.3V Supply Voltage (**V3P3A, V3P3D**)[+]	Normal Operation	3.0	3.3	3.6	V
	Battery Backup	0		3.8	V
VBAT	No Battery	Externally Connect to V3P3D			
	Battery Backup	2.0		3.8	V
Operating Temperature		-40		85	ºC

[+] V3P3A and V3P3D should be shorted together on the circuit board. GNDD and GNDA should also be shorted on the circuit board.

LOGIC LEVELS

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Digital high-level input voltage, V_{IH}		2		V3P3D	V
Digital low-level input voltage, V_{IL}		–0.3		0.8	V
Digital high-level output voltage V_{OH}	I_{LOAD} = 1mA	V3P3D –0.4		V3P3D	V
	I_{LOAD} = 15mA	V3P3D-0.6[1]			V
Digital low-level output voltage V_{OL}	I_{LOAD} = 1mA	0		0.4	V
	I_{LOAD} = 15mA			0.8[1]	V
Input pull-up current, I_{IL}	VIN=0V				
RESETZ		10		100	µA
E_RXTX, E_ISYNC/BRKRQ		10		100	µA
E_RST		10		100	µA
Other digital inputs		-1		+1	µA
Input pull down current, I_{IH}	VIN=V3P3D				
TEST		10		100	µA
Other digital inputs		-1		+1	µA

[1] Guaranteed by design; not production tested.

SUPPLY CURRENT

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V3P3A + V3P3D	Normal Operation, **V3P3A=V3P3D**=3.3V VBAT=3.6V		8.8	11.5	mA
V3P3A current			3.7	4.7	mA
V3P3D current			5.1	6.8	mA
VBAT current		-300		300	nA
VBAT current, VBAT=3.6V	Battery backup, ≤25°C **V3P3A=V3P3D**=0V f_{OSC} = 32kHz		2	4	µA
	85°C		4	12[1]	µA

[1] Guaranteed by design; not production tested.

VREF

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VREF output voltage, VNOM(25)	Ta = 25ºC	1.193	1.195	1.197	V
VREF output impedance	I_{LOAD} = 10µA, -10µA			2.5	kΩ
VNOM definition [2]	VNOM(T) = VREF(22) + (T-22)TC1 + (T-22)^{2}TC2				V
VREF(T) deviation from VNOM(T) $\frac{VREF(T)-VNOM(T)}{VNOM}\frac{10^6}{\max(\lvert T-22\rvert,40)}$	Ta = -40ºC to +85ºC, for 71M6515H-IGT/F	-10[1]		+10[1]	PPM/ºC
	Ta = -40ºC to +85ºC, for 71M6515H-IGTW/F	-40[1]		+40[1]	PPM/ºC
VREF aging			±25		PPM/year

[1] Guaranteed by design; not production tested.

[2] This relationship describes the nominal behavior of VREF at different temperatures. The values of TC1 and TC2 are device specific in general and are programmed into the device at manufacturing.

2.5V VOLTAGE REGULATOR

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Voltage Overhead **V3P3D-V2P5**	Reduce V3P3 until V2P5 drops 200mV			440	mV
PSRR **ΔV2P5/ΔV3P3D**	**RESETZ**=1, I_{LOAD}=0	-3		+3	mV/V

RTC

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Range for date		2000	--	2255	year

RESETZ

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Reset pulse width		5			µs
Reset pulse fall time				1[1]	µs

[1] Guaranteed by design; not production tested.

CRYSTAL OSCILLATOR

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Maximum Output Power to Crystal[4]				1	µW
Xin to Xout Capacitance			3		pF
Capacitance to DGND Xin Xout			 5 5		 pF pF
Watchdog RTC_OK threshold				25	kHz

TEMPERATURE SENSOR

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Nominal Sensitivity (S_n)[4]	T_A=25ºC, T_A=85ºC Nominal relationship: $N(T)= S_n*T+N_n$		-900		LSB/ºC
Nominal Offset (N_n)[4]			40000 0		LSB
Temperature Error, relative to 25ºC error $ERR = (T-25) - \frac{(N(T)-N(25))}{S_n}$	T_A = -40ºC to +85ºC	-3[1]		+3[1]	ºC

[1] Guaranteed by design; not production tested.

PULSE GENERATOR TIMING SPECIFICATIONS

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
PULSEW, PULSER maximum rate	APULSE=2^{31}-1, WRATE=2^{15}-1			7.56	kHz
PULSE3, PULSE4 maximum rate	PULSE3=2^{31}-1, WRATE=2^{15}-1			0.15	kHz
Pulse count frequency	all pulse outputs			0.15	kHz

THERMAL CHARACTERISTICS

PARAMETER	CONDITION	VALUE	UNIT
Thermal resistance, junction to ambient ($R\theta_{JA}$)	Air velocity 0 m/s. Part soldered to PCB.	63.7	°C/W

UART HOST INTERFACE

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Baud Rate		19.2	-	38.4	kBaud
Character set			binary		
Data Format			8N1		
Byte-to-byte delay (6515H times out after maximum delay)	Host sending data to 6515H	10		20	ms
Byte-to-byte delay	6515H sending data to host	0		0.1	ms
Response time to read command	6515H has data ready	0.5		2	ms
Response time to read command when 71M6515H is post-processing data	Data not ready *CE_ONLY* = 1 *CE_ONLY* = 0 and *VAH_SELECT* = 0 *CE_ONLY* = 0 and *VAH_SELECT* = 1			 40 80 350	 ms ms ms

ADC CONVERTER, V3P3 REFERENCED

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Usable Input Range (Vin-**V3P3A**)		-250		250	mV peak
Voltage to Current cross talk: $\frac{10^6 * Vcrosstalk}{Vin}\cos(\angle Vin - \angle Vcrosstalk)$	*Vin* = 200mV peak, 65Hz, on VA, VB, or VC *Vcrosstalk* = largest measurement on IA, IB, or IC	-10[1]		+10[1]	µV/V
THD (First 10 harmonics) 250mV-pk 20mV-pk	Vin=65Hz, 64kpts FFT, Blackman-Harris window		 -75 -90		 dB dB
Input Impedance	Vin=65Hz	40		90	kΩ

Temperature Coefficient of Input Impedance	Vin=65Hz		1.7		Ω/°C
LSB size			355		nV/LSB
Digital Full Scale			±884736		LSB
ADC Gain Error vs. %Power Supply Variation $\frac{10^6 \Delta Nout_{PK}\ 357nV/V_{IN}}{100 \Delta V3P3A/3.3}$	Vin=200mV pk, 65Hz V3P3A=3.0V, 3.6V			50	PPM/ %
Input Offset (Vin-**V3P3A**)		-10		+10	mV

[1] Guaranteed by design; not production tested.

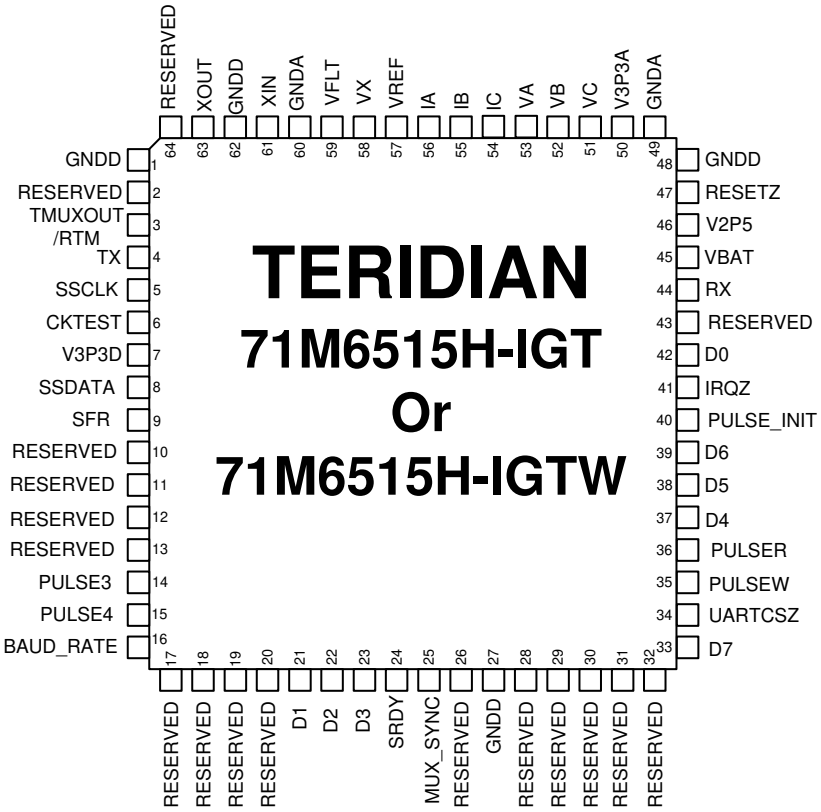
RECOMMENDED EXTERNAL COMPONENTS

NAME	FROM	TO	FUNCTION	VALUE	UNIT
C1	**V3P3A**	**AGND**	Bypass capacitor for 3.3V supply	≥0.1±20%	µF
C2	**V3P3D**	**DGND**	Bypass capacitor for 3.3V supply	≥0.1±20%	µF
XTAL	**XIN**	**XOUT**	32.768kHz crystal – electrically similar to ECS .327-12.5-17X or Vishay XT26T, load capacitance 12.5pF	32.768	kHz
CXS	**XIN**	**AGND**	Load capacitor for crystal (depends on crystal specs and board parasitics).	27±10%	pF
CXL	**XOUT**	**AGND**		27±10%	pF
C2P5	**V2P5**	**DGND**	Bypass capacitor for V2P5	≥0.1±20%	µF

FOOTNOTES:

1 This spec is guaranteed, has been verified in production samples, but is not measured in production.
2 This spec is guaranteed, has been verified in production samples, but is measured in production only at DC.
3 This spec is measured in production at the limits of the specified operating temperature.
4 This spec defines a nominal relationship rather than a measured parameter. Correct circuit operation is verified with other specs that use this nominal relationship as a reference

PIN CONFIGURATION AND PIN FUNCTION



Pins marked RESERVED should be left unconnected during normal use.

Analog Pin Description

Name	Pin No.	Type	Circuit	Description
IA, IB, IC	56 55 54	I	6	Line Current Sense Inputs: Voltage inputs to the internal A/D converter. Typically, they are connected to the output of a current transformer. The input is referenced to V3P3A. **Unused pins must be tied to V3P3A.**
VA, VB, VC	53 52 51	I	6	Line Voltage Sense Inputs: Voltage inputs to the internal A/D converter. Typically, they are connected to the output of a resistor divider. The input is referenced to V3P3A. **Unused pins must be tied to V3P3A.**
VFLT	59	I	7	Power Fault Input. **This pin must be tied to V3P3A.**
VX	58	I	6	Auxiliary input (not used). **This pin should be tied to VREF.**
VREF	57	I/O	9	Voltage Reference for the ADC.
XIN, XOUT	61 63	I	8	Crystal Inputs: A 32768Hz crystal should be connected across these pins. Typically, a 15pF capacitor is also connected from each pin to GNDA. See the datasheet of the crystal manufacturer for details.

Pin types: P = Power, O = Output, I = Input, I/O = Input/Output
The circuit number denotes the equivalent circuit, as specified under "I/O Equivalent Circuits".

Digital Pin Description

Unless otherwise indicated, all inputs and outputs are standard CMOS. Inputs do NOT have internal pull-ups or pull-downs.

Name	Pin No.	Type	Circuit	Description
CKTEST	6	I/O	4	Clock PLL output. Can be enabled and disabled by *CKOUT_DSB* (see Status Mask).
D0 D1 D2 D3 D4 D5 D6 D7	42 21 22 23 37 38 39 33	I/O	3, 4	Input/output pins 0 through 7. **These pins must be terminated to V3P3D or ground if configured as input pins.** **D0 through D7 are high impedance after reset or power-up and are configured as outputs and driven low 140ms after RESETZ goes high.**
PULSE4	15	O	4	The fourth pulse generator output
PULSE3	14	O	4	The third pulse generator output
PULSE_INIT	40	I	3	The pulse output initial power-up voltage (0: 0V, 1: 3.3V), default is 1. **This pin must be terminated to V3P3D or ground.**
BAUD_RATE	16	I	3	The UART baud rate (1: 38.4kbd, 0: 19.2kbd). **This pin must be terminated to V3P3D or ground.**
IRQZ	41	O	4	Interrupt output, low active. A falling edge indicates the end of a measurement frame, as well as alarms. Rises when status word is read.
MUXSYNC	25	O	4	Internal signal. MUXSYNC falls at the beginning of each conversion cycle (multiplexer frame).
RESETZ	47	I	1	Chip reset: Input pin with internal pull-up resistor, used to reset the chip into a known state. For normal operation, this pin is set to 1. To reset the chip, this pin is driven to 0 for 5 microseconds. No external reset circuitry is necessary for power-up reset.

Name	Pin No.	Type	Circuit	Description
UARTCSZ	34	I	3	Enables the UART when 0. The UART is disabled when this pin is set to 1. A positive pulse on this pin will reset the UART. **This pin must be terminated to ground.**
SRDY SFR SSCLK SSDATA	24 9 5 8	I O O O	3 4 4 4	High-Speed Synchronous Interface (SSI). **The SRDY input should be tied to ground.** SSI frame pulse output, one SSCLK wide. SSI clock output (5MHz or 10MHz selectable). SSI data output, changes on the rising edge of SSCLK.
RX	44	I	3	UART serial Interface receiver input. **The voltage at this pin must not exceed 3.6V**. **This pin must be terminated to V3P3D or ground.**
TX	4	O	4	UART serial Interface transmitter output.
TMUXOUT	3	O	4	Digital output test multiplexer. Controlled by *TMUX[2:0]*.
PULSER PULSEW	36 35	O O	4 4	Selectable pulse output (default: VARh pulse). Selectable pulse output (default: Wh pulse).

Power/Ground Pin Description

Name	Pin No.	Type	Description
GNDA	49,60	P	Analog ground: This pin should be connected directly to the ground plane.
GNDD	1,27, 48,62	P	Digital ground: These pins must be connected directly to the ground plane.
V3P3A	50	P	Analog power: A 3.3V analog power supply should be connected to this pin.
V3P3D	7	P	Digital power supply: A 3.3V digital power supply should be connected to this pin.
VBAT	45	P	Battery backup power supply. A battery or super-capacitor is to be connected between VBAT and GNDD. If no battery is used, connect VBAT to V3P3D.
V2P5	46	O	Output of the 2.5V regulator. A 0.1µF capacitor should be connected from this pin to GND.

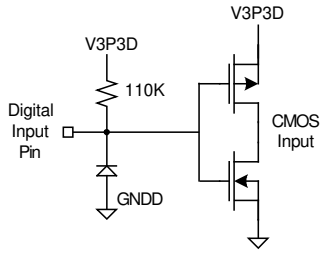
Pin types: P = Power, O = Output, I = Input, I/O = Input/Output
The circuit number denotes the equivalent circuit, as specified under "I/O Equivalent Circuits".

Reserved Pins

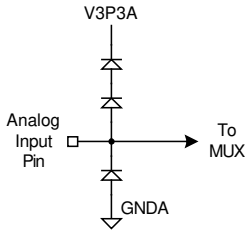
Pins labeled RESERVED are not to be connected.

Name	Pin No.	Description
RESERVED	2,10,11,12, 13,17,18,19, 20,26,28,29, 30,31,32,43, 64	**DO NOT CONNECT THESE PINS!**

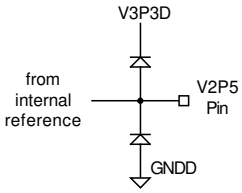
I/O Equivalent Circuits



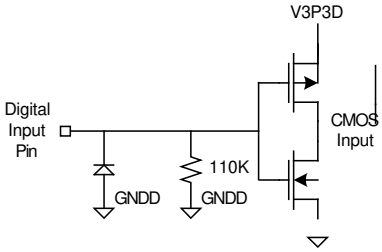
Digital Input Equivalent Circuit Type 1:
Standard Digital Input or pin configured as DIO Input with Internal Pull-Up



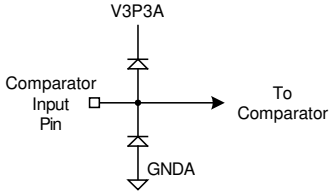
Analog Input Equivalent Circuit Type 6:
ADC Input



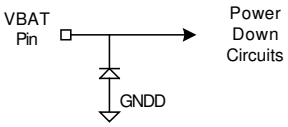
V2P5 Equivalent Circuit Type 10:
V2P5



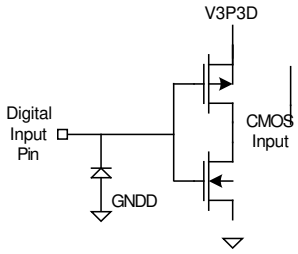
Digital Input Type 2:
Pin configured as DIO Input with Internal Pull-Down



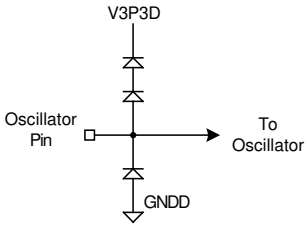
Comparator Input Equivalent Circuit Type 7:
Comparator Input



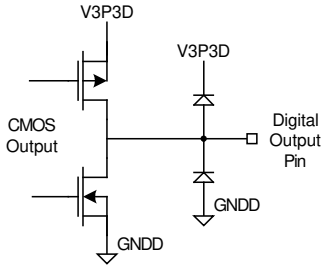
VBAT Equivalent Circuit Type 12:
VBAT Power



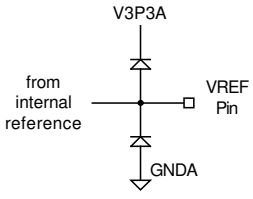
Digital Input Type 3:
Standard Digital Input or pin configured as DIO Input



Oscillator Equivalent Circuit Type 8:
Oscillator I/O



Digital Output Equivalent Circuit Type 4:
Standard Digital Output or pin configured as DIO Output



VREF Equivalent Circuit Type 9:
VREF

TYPICAL PERFORMANCE CHARACTERISTICS

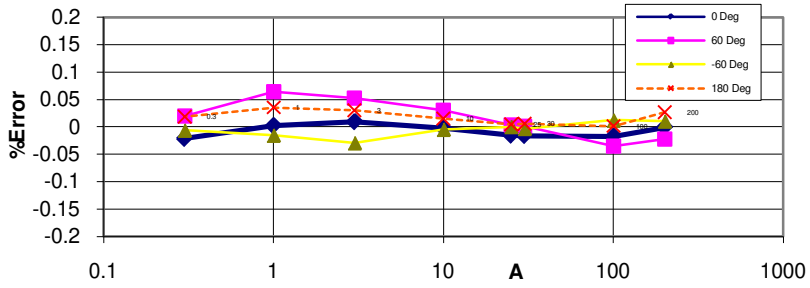


Figure 3: Wh Accuracy, 0.3A - 200A/240V

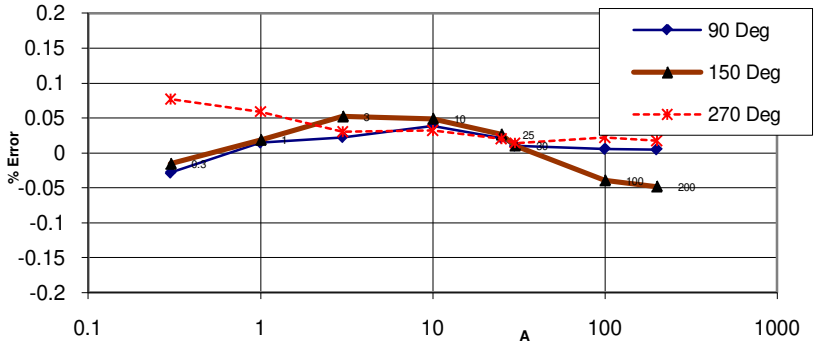
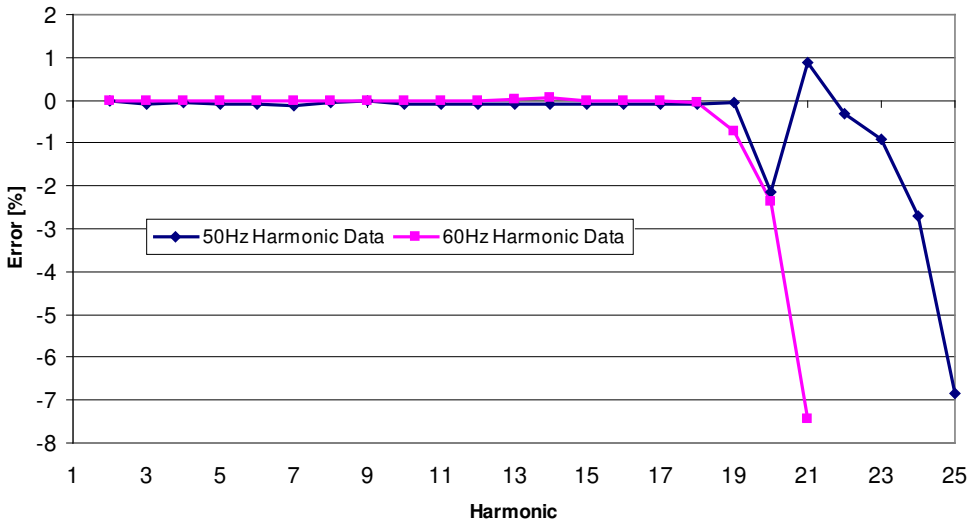


Figure 4: VARh Accuracy for 0.3A to 200A/240V Performance



Measured at current distortion amplitude of 40% and voltage distortion amplitude of 10%.

Figure 5: Meter Accuracy over Harmonics at 240V, 30A

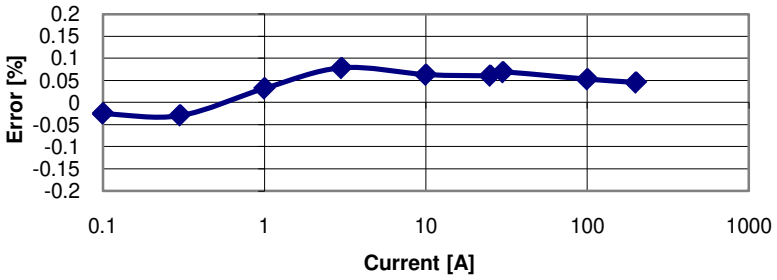


Figure 6: Typical VAh Accuracy for VAh Using Vector Method

FUNCTIONAL DESCRIPTION

THEORY OF OPERATION

The 71M6515H integrates the primary functional blocks required to implement a solid-state electricity meter front end. Included on-chip are an analog front end (AFE), a digital computation engine (CE), a voltage reference, a real time clock, and I/O pins. Various current sensor technologies are supported including Current Transformers (CT), Resistive Shunts, and Rogowski (*di/dt)* Coils.

In a typical application, the 71M6515H sequentially digitizes the voltage inputs on pins IA, VA, IB, VB, IC, VC and performs calculations to measure active energy (Wh), reactive energy (VARh), and apparent energy (VAh). In addition to these measurement functions, the real time clock function allows the device to record time of use (TOU) metering information for multi-rate applications.

The 71M6515H contains a temperature-trimmed ultra-precise voltage reference, and the on-chip digital temperature compensation mechanism includes a temperature sensor and associated controls for correction of unwanted temperature effects on measurement. RTC accuracy can be greatly improved by supplying correction coefficients derived from crystal characterization. The combination of both features enables designers to produce electricity meters with exceptional accuracy over the industrial temperature range.

Meter Equations

The 71M6515H implements the equations in Table 1. Register *EQU* specifies the equation to be used. In one sample time, each of the six inputs is converted and the selected equation updated. In a typical application, IA, IB, IC are connected to current transformers that sense the current on each phase of the line voltage. VA, VB, and VC are typically connected to voltage sensors (resistor dividers) with respect to NEUTRAL. NEUTRAL is to be connected to V3P3A, the analog supply voltage. **NEUTRAL is the zero reference for all analog measurements.**

EQU	Watt & VAR Formula	Application	Channels used from MUX sequence Mux State:					
			0	1	2	3	4	5
0	VA IA	1 element, 2W 1ø	IA	VA	-	-	-	-
1*	VA(IA-IB)/2	1 element, 3W 1ø	IA	VA	IB	-	-	-
2	VA IA + VB IB	2 element, 3W 3 øDelta	IA	VA	IB	VB	-	-
3*	VA (IA - IB)/2 + VC IC	2 element, 4W 3ø Delta	IA	VA	IB	-	IC	VC
4*	VA(IA-IB)/2 + VB(IC-IB)/2)	2 element, 4W 3ø Wye	IA	VA	IB	VB	IC	-
5	VA IA + VB IB + VC IC	3 element, 4W 3ø Wye	IA	VA	IB	VB	IC	VC

Note: Equations 1*, 3*, 4* available only when *IMAGE* = 00 (CT mode).

Table 1: Meter Equations

Table 2 shows how the elements of the meter are mapped for the six possible equations.

EQU	Watt & VAR Formula (WSUM/VARSUM)	Element Output Mapping					
		W0SUM/ VAR0SUM	W1SUM/ VAR1SUM	W2SUM/ VAR2SUM	I0SQ SUM	I1SQ SUM	I2SQ SUM
0	VA IA (1 element, 2W 1ϕ)	VA*IA	-	-	IA	-	-
1	VA*(IA-IB)/2 (1 element, 3W 1ϕ)	VA*(IA-IB)/2	VA*IB	-	IA-IB	IB	-
2	VA*IA + VB*IB (2 element, 3W 3ϕ Delta)	VA*IA	VB*IB	-	IA	IB	-
3	VA*(IA-IB)/2 + VC*IC (2 element, 4W 3ϕ Delta)	VA*(IA-IB)/2	-	VC*IC	IA-IB	IB	IC
4	VA*(IA-IB)/2 + VB*(IC-IB)/2 (2 element, 4W 3ϕ Wye)	VA*(IA-IB)/2	VB*(IC-IB)/2		IA-IB	IC-IB	IC
5	VA*IA + VB*IB + VC*IC (3 element, 4W 3ϕ Wye)	VA*IA	VB*IB	VC*IC	IA	IB	IC

Table 2: Meter Element Output Mapping

ANALOG FRONT END

A/D Converter (ADC)

A single delta-sigma A/D converter (ADC) digitizes the inputs to the device. The resolution of the ADC is 21 bits. The ADC operates at 5MHz oversampling rate and places the digital results in CE memory. Each analog input is sampled at 2520Hz. Once each accumulation interval, it refreshes the temperature value that is placed in the *TEMP_RAW* register. **The analog reference for all inputs is V3P3A, i.e. the ADC processes voltages between the input pins and V3P3A.**

Voltage Reference

The device includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques as well as production trims to minimize errors caused by component mismatch and drift. The result is a voltage output with a predictable temperature coefficient.

The CE compensates for temperature characteristics of the voltage reference by modifying the gain applied to the V and I channels based on the coefficients *PPMC* and *PPMC2*. See the section "TEMPERATURE COMPENSATION" for details.

DIGITAL COMPUTATION

The six ADC outputs are processed and accumulated digitally. The default product summation is based on 42*60 (if the *SUM_CYCLES* register is set to 60) samples per accumulation interval. At the end of each accumulation interval, a ready interrupt (IRQZ) is signaled (if enabled with the *READY* bit in *STMASK*), indicating that fresh data is available to the host. For instance, if *SUM_CYCLES* =30, the IRQZ rate will be 2Hz (500ms).

A dedicated 32-bit Computation Engine (CE) performs the precision computations necessary to accurately measure energy. Internal CE calculations include frequency-insensitive offset cancellation on all six channels and a frequency insensitive 90° phase shifter for VAR calculations. The CE also includes LPF smoothing filters after each product and squaring circuit to attenuate ripple and eliminate beat frequencies between the power line fundamental and the accumulation time. The CE directly calculates Watts, VARs, V^2, and I^2 and accumulates them for one interval.

At the end of each CE computation cycle, the accumulated data are post-processed to calculate RMS amplitudes, phase angles, and VAh. When post-processing is complete, the IRQZ signal is activated.

The minimum combined cycle time for CE and post-processor is 400ms, which makes the maximum frequency for the IRQZ signal 2.5Hz.

If the 71M6515H is interfacing to an external DSP (typically, but not necessarily through the SSI interface), the host may turn off post-processing by setting the *CE_ONLY* bit in the *CONFIG* word. This will permit setting *SUM_CYCLES* below its recommended lower limit of 24. *SUM_CYCLES* may then be reduced to 1, creating an accumulation interval of only 42 samples. The outputs available in CE only mode are limited to temperature, frequency, voltage phases, input signal zero crossings, plus WSUM and VARSUM for each phase and VSQSUM, ISQSUM, and ISQFRACT for each phase.

Pulse Generators

The chip contains four pulse generators connected to the pins PULSEW, PULSER, PULSE3, and PULSE4 that create low jitter pulses from 32-bit data. The peak time jitter for PULSEW and PULSER is the 397µs MUX frame period, and is independent of the rate of the generator or the length of time the generator is monitored. Thus, if the pulse generator is monitored for 1 second, the peak jitter is 400PPM. After 10 seconds, the peak jitter is 40PPM.

PULSE3 and PULSE4 are updated at a slower rate and have four times higher jitter, i.e. 160PPM after 10 seconds.

The average jitter is always zero. If it is attempted to drive either pulse generator faster than its maximum rate, it will simply output at its maximum rate without exhibiting any roll-over characteristics.

Pulse generator inputs may be from three sources:

- Internal (directly from the CE), PULSEW and PULSER only
- External (controlled by the host writing to registers *APULSEW, APULSER, APULSE3, APULSE4*)
- Post-processed values

The source is selected individually for each pulse output with the *PULSEW_SRC, PULSER_SRC, PULSE3_SRC,* and *PULSE4_SRC* registers. Figure 7 shows internal pulse generation for the PULSEW output selected by writing the value 35 into the *PULSEW_SRC* register.

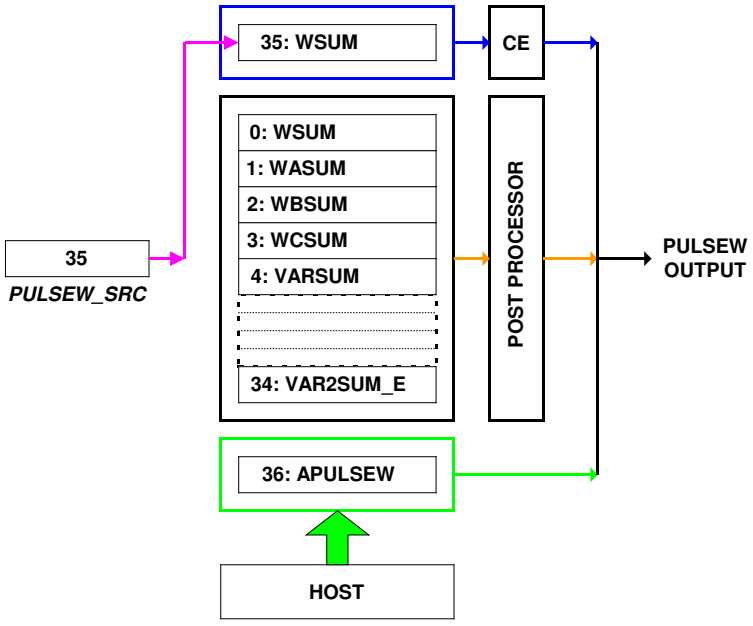


Figure 7: Internal Pulse Generation Selected in the *PULSEW_SRC* Register

Internal data is pulsed out during the accumulation interval immediately following its accumulation interval. Post-processed values are pulsed out one accumulation interval after that.

The pulse generator output rate depends on its input value, *WRATE*, *PULSE_SLOW*, and *PULSE_FAST*. Additionally, its maximum pulse width (negative going pulse) is controlled by *PULSEWIDTH*. High frequency pulses will have 50% duty cycle until their rate slows enough that their pulse width is limited by *PULSEWIDTH*.

In internal and post-processed modes, the pulse rate, expressed as Kh (Wh per pulse) is given by the formula:

$$Kh = \frac{VMAX\ IMAX}{In\_8 \cdot SUM\_CYCLES \cdot WRATE \cdot X} 1.5757 \quad Wh / Pulse$$

where
VMAX is the meter voltage corresponding to an input voltage of 176mV (rms) at the VA, VB, and VC input pins ,
IMAX is the meter current corresponding to an input voltage of 176mV (rms) at the IA, IB, and IC input pins,
In_8 is the additional ADC gain (1 or 8), as controlled by the *IA_X*, *IB_X* and *IC_X* bits in the *CONFIG* register.
X is the pulse speed factor determined from Table 3.

PULSE_SLOW	*PULSE_FAST*	X
0	0	$1.5*2^{2}=6$
0	1	$1.5*2^{6}=96$
1	0	$1.5*2^{-4}=0.09375$
1 (default)	1 (default)	1.5

Table 3: Pulse Speed Factor X

In external pulse mode, the pulse rate is given by the formula:

Rate(Hz) = *WRATE* * X * input * $35.82*10^{-12}$,

where **input** is the value in registers *APULSER, APULSEW. APULSE3* or *APULSE4,*
X is the pulse speed factor determined from Table 3.

External pulse generation can be seen as providing the raw voltage and current readings equivalent to $V_{in}*I_{in}$ / LSB directly to the pulse generator.

The maximum pulse rate is 7.56kHz for PULSEW and PULSER, and 150Hz for PULSE3 and PULSE4.

In external pulse mode, the pulse generators load their data at the beginning of each CE accumulation interval, preserving any partially implemented pulses from the previous interval. The source of data is controlled by the entries in the *PULSE_SRCS* register. *PULSER_SRCS* contains 8-bit entries for each pulse source, PULSEW, PULSER, PULSE3, and PULSE4. See the register description for details.

The procedure for accurate external pulse generation controlled by the host is:

1) Respond to a READY interrupt by reading the accumulated values.
2) Process the accumulated values.
3) Write the processed value(s) to *APULSER, APULSEW, APULSE3,* or *APULSE4*. The host must write to *APULSER, APULSEW, APULSE3,* and *APULSE4* before the next READY interrupt for the pulse generation to be beginning in the following accumulation interval.

Figure 8 illustrates pulse generator timing.

Regardless of the source, the pulse generators should receive new data during each accumulation interval. If this does not occur and if the corresponding bit in the *STMASK* register is set, an *APULSE_ERR* interrupt will be issued.

The PULSEW, PULSER, PULSE3 and PULSE4 pins are suitable for driving LEDs through a current limiting resistor. The LED should be connected so it is on when the pulse pin is low.

The pin PULSE_INIT determines the logic level applied to the pulse pins on power-up, i.e. with PULSE_INIT low, the pulse pins will be initialized to low (default = 1).

The pulse width P_W is controlled with the *PULSEWIDTH* register for the PULSER and PULSEW output pins per the following formula:

$$P_W = \frac{2 \cdot PULSEWIDTH + 1}{2520.6}$$

The PULSE3 and PULSE4 output pins will always generate pulses with 50% duty cycle.

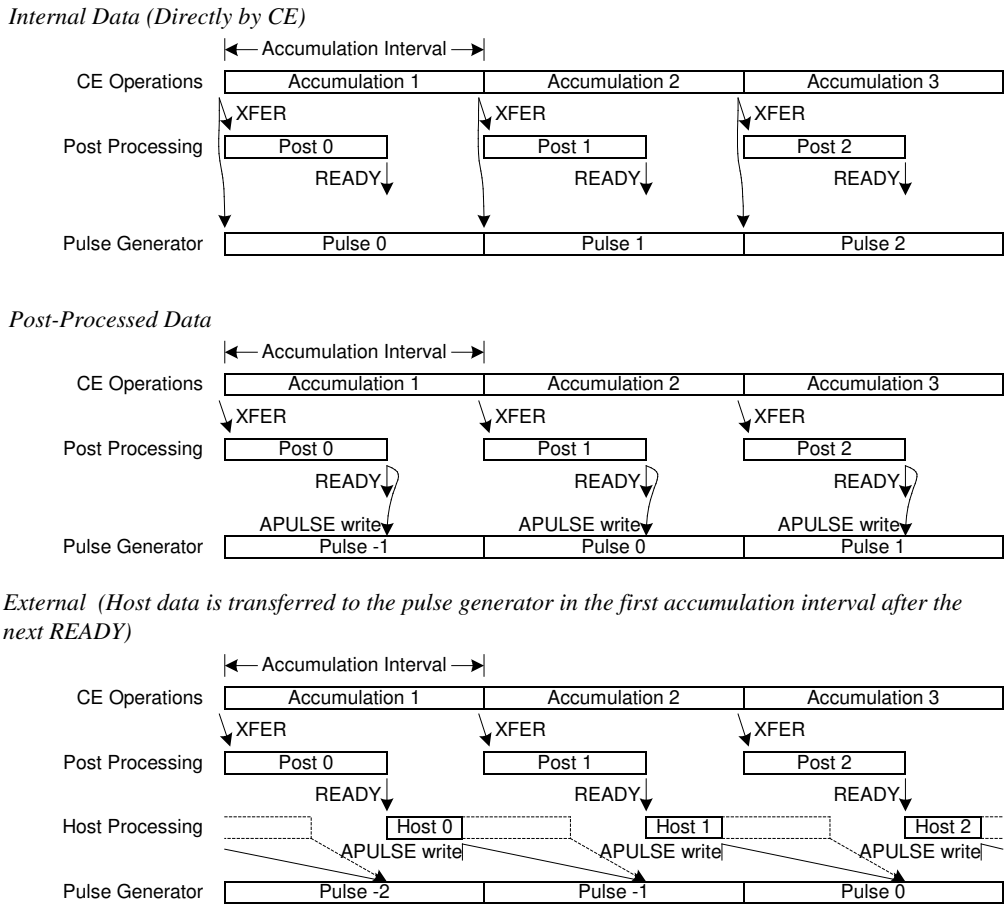


Figure 8: Pulse Generator Timing

Internal Resources

Oscillator

The oscillator drives a standard 32.768kHz watch crystal. Crystals of this type are accurate and do not require a high current oscillator circuit. The 71M6515H oscillator has been designed specifically to handle watch crystals and is compatible with their high impedance and limited power handling capability. The oscillator power dissipation is very low to maximize the lifetime of any battery backup device attached to VBAT. Using PLL techniques, all internal clocks, such as the 4.915MHz clock for the ADC and the post-processor, are derived from the watch crystal frequency.

Real-Time Clock (RTC)

The RTC is driven directly by the crystal oscillator. In the absence of V3P3, it is powered by the battery-backed up supply. The RTC consists of a counter chain and output registers. The counter chain consists of registers for seconds, minutes, hours, day of week, day of month, month, and year. The nominal quadratic temperature coefficient of the crystal is automatically compensated in the RTC. **The RTC is capable of processing leap years.**

I/O Peripherals

The 71M6515H includes several I/O peripheral functions that improve the functionality of the device and reduce the component count for most meter applications. The I/O peripherals include a UART and digital I/O.

Digital I/O

The device includes eight pins of general purpose digital I/O (D0…D7). Each pin can be configured independently as an input or output with the *D_DIR* bits. Inputs are standard CMOS with no pull-ups or pull-downs. Outputs are standard CMOS. The DIO pins are controlled by the *D_CONFIG* register.

Immediately after reset or power-up, D0 through D7 are in tri-state mode. 140 ms after reset, D0 through D7 are configured as outputs and driven low.

UART Host Interface

The UART is a dedicated 2-wire serial interface, which can communicate with the host processor. The operation of each pin is as follows:

RX: Is the pin accepting the serial input data. It inputs data to internal registers. The bytes are input LSB first. The voltage applied to this pin must be restricted to 0 to 3.6V.

TX: Is the pin used for serial output data. It outputs the contents of a block of internal registers. The bytes are output LSB first.

BAUD_RATE: The baud rate can be selected with the BAUD_RATE pin (38.4bps when high, 19.2bps when low).

UARTCSZ: This pin enables the UART when low. The UART can be reset by taking UARTCSZ briefly to the high state and then low again.

The 71M6515H has several on-chip registers, which can be read and written. All transfers start with a stream of 8-bit bytes (LSB first) from the host on the RX input, followed by a (possibly null) stream of 8-bit bytes (LSB first) to the host on the TX output (see Figure 9 and Figure 10). The UART is configured as 8N1 (8 bits, no parity, 1 stop bit).

If the *READY* bit in *STMASK* is enabled, the IRQZ pin can be used to signal data availability to the host. If data read cycles exceeding 1 second are used, care should be taken to prevent data overflow.

UART Write Register Operation

The registers are written by sending a byte, consisting of a starting register address in the seven MSBs and '0' in the LSB indicating this is a write operation. It is followed by a one byte length of bytes to write. If more bytes arrive than fit in the addressed register, subsequent registers will be written. The bytes are processed in "big-endian" order (i.e. most significant byte first). See Figure 9 (read bits and bytes from left to right).

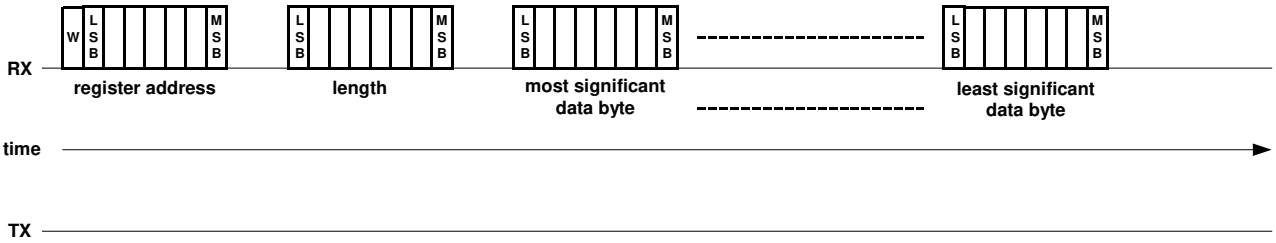


Figure 9: UART Write Operation

UART Read Register Operation

The registers are read by sending a byte, consisting of a start register address in the seven MSBs and '1' in the LSB indicating this is a read operation. It is followed by a one byte length of bytes to read. If more bytes are asked for than the size of the addressed register, subsequent registers will be read. The bytes are in "big-endian" order (i.e. most significant byte first). See Figure 10.

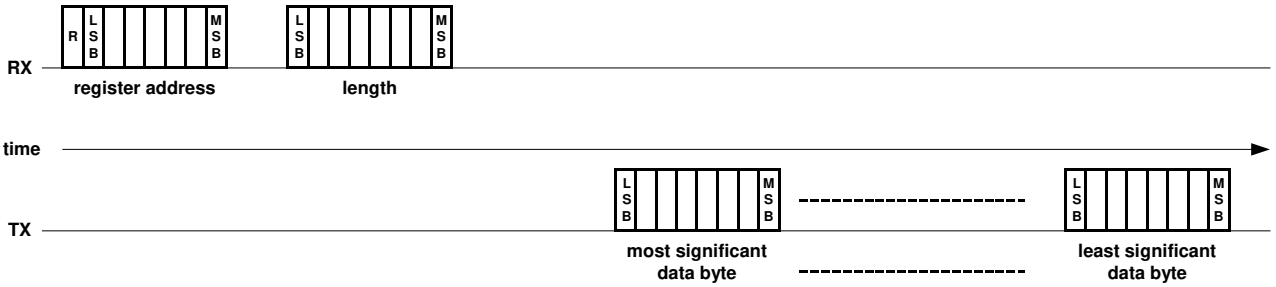


Figure 10: UART Read Operation

Note: In both register read and write operations, the register address can be 0 through 127 (0x7F). The register address byte is obtained by left-shifting the register address by one bit and setting bit 0 to 1 for read or setting bit 0 to 0 for write.

Synchronous Serial Interface (SSI)

A high speed, handshake, serial interface is available to send a contiguous block of CE data to an external data logger or DSP. The block of data, configurable as to location and size, is sent at the beginning of each ADC multiplex cycle. The SSI interface is enabled by the *SSI_EN* bit and consists of the outputs SSCLK, SSDATA, and SFR and of the SRDY input pin. The interface is compatible with 16-bit and 32-bit processors. The operation of each pin is as follows:

SSCLK: This pin provides the serial clock. The clock can be 5MHz or 10MHz, as specified by the *SSI_10M* bit. The *SSI_CKGATE* bit controls whether SSCLK runs continuously or is gated off when no SSI activity is occurring. If SSCLK is gated, it will begin three cycles before SFR rises and will persist three cycles after the last data bit is output.

SSDATA: This pin provides the serial output data. SSDATA changes on the rising edge of SSCLK and outputs the contents of a block of CE words starting with address *SSI_STRT* and ending with *SSI_END*. The words are output MSB first. SSDATA is stable with the falling edge of SSCLK.

SFR: This pin provides the framing pulse. Although CE words are always 32 bits, the SSI interface will frame the entire data block as a single field, as multiple 16 bit fields, or as multiple 32 bit fields. The SFR pulse is one clock cycle wide, changes state on the rising edge of SSCLK and precedes the first bit of each field. The field size is set with *SSI_FSIZE*: 0-entire data block, 1-8 bit fields, 2-16 bit fields, 3-32 bit fields. The polarity of the SFR pulse can be inverted with *SSI_FPOL*. The first SFR pulse in a frame will rise on the third SSCLK clock period after MUX_SYNC (fourth SSCLK period, if SSCLK is 10MHz). MUX_SYNC can be used to synchronize the fields arriving at the data logger or DSP.

SRDY: The SRDY input should always be tied to GND.

The SSI timing is shown in Figure 11.

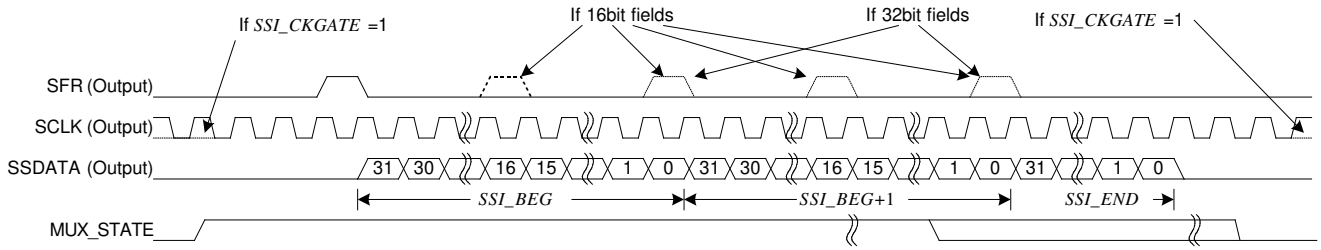


Figure 11: SSI Timing (*SSI_FPOL* = *SSI_RDYPOL* = 0)

Fault and Reset Behavior

Reset Mode

When RESETZ is pulled low or when VFLT < V3P3/2, all activity (i.e. sampling of analog signals, CE, generation of digital outputs) in the chip stops while the analog circuits are active. The exceptions are the oscillator and RTC module, which continue to run. Additionally, all I/O Register bits are cleared. As long as VFLT > V3P3/2, the internal 2.5V regulator will continue to provide power to the digital section.

Once initiated, the reset mode will persist until the reset timer times out. This will occur in 4100 cycles of the real time clock after RESETZ goes high, at which time the 71M6515H will begin executing its preboot and boot sequences.

Power Fault Circuit

The power fault comparator compares the voltage at the VFLT pin to V3P3/2. The comparator output internally enables the battery backup protection for oscillator, RTC and RAM during the power fail mode.

Temperature Compensation

Voltage Reference

The internal voltage reference of the 71M6515H is calibrated at 25°C during device manufacture. The 71M6515H is given additional temperature-related calibrations which further compensate its ADC gain and allow it to achieve 10PPM/°C over ±60°C temperature range.

Temperature Sensor

The device includes an on-chip temperature sensor for determining the temperature of the bandgap reference. The primary use of the temperature data is to determine the magnitude of compensation required to offset thermal drift in the system. The temperature sensor is read once per accumulation interval.

Temperature measurement can be implemented with the following steps:

1) At a known temperature T_N, read the *TEMP_RAW* register and write the value into *TEMP_NOM* register.
2) Read the *DELTA_T* register at the known temperature. The obtained value should be <±0.1°C.
3) The temperature T (in °C) at any environment can be obtained by reading the *DELTA_T* register and applying the following formula:

$$T = T_N + \frac{DELTA\_T}{10}$$

Temperature Compensation for Energy Measurements

TEMP_NOM is one of the calibration parameters that must be loaded by the host in order to enable temperature measurement and thereby temperature compensation.

PPMC and *PPMC2*, the linear and quadratic compensation coefficients, compensate for temperature drift in the 71M6515H reference that affects the meter performance. *PPMC* and *PPMC2* describe how the 71M6515H calculations are to respond to temperature. This means they should be the negative of the meter behavior before compensation. *PPMC* and *PPMC2* are scaled from PPM/°C and PPM/°C^2 values. See the register description for details. Temperature compensation can be selected to operate in one of two modes shown in the table below:

Temperature Compensation Mode	*DEFAULT_PPM* Bit in *CONFIG* Register	*PPMC*, *PPMC2* Calculation
Internal (CE)	1	By post-processor, based on stored VREF characteristics
External (host)	0	By host

When the part is first powered up, *TEMP_NOM*, *PPMC*, and *PPMC2* are zero. When the host writes its calibration value into *TEMP_NOM* (after setting the *DEFAULT_PPM* bit on the *CONFIG* register to 1), *PPMC* and *PPMC2* will automatically be initialized to the values that best compensate for the temperature drift of the internal reference. These parameters will be individually customized for 71M6515H parts. If, for some reason, the host writes to *TEMP_NOM* again, *PPMC* and *PPMC2* will not be changed since they will no longer be zero.

If *TEMP_NOM* is not loaded by the host, *PPMC* and *PPMC2* are ignored, and their values are permanently held at zero. If *TEMP_NOM* is zero, no temperature compensation occurs, even if *PPMC* and *PPMC2* are loaded.

If the host wishes to provide its own compensation, it should read *PPMC* and *PPMC2* and modify them by merging the additional compensation into to them. In that case, the *DEFAULT_PPM* bit in the CONFIG register must be zero.

Temperature Compensation for the Crystal and RTC

The crystal oscillator contributes negligible error to energy calculations. However, sometimes specifications for the real time clock (RTC) require better accuracy than that provided by the untrimmed watch crystal. The 71M6515H therefore allows calibration of the RTC clock. Calibration requires that frequency tolerance and frequency stability either be obtained from the manufacturer or be independently measured (the RTC clock is available on the TMUX pin). Calibration does not change the frequency of the RTC clock, but rather increments or decrements the clock by one second when sufficient error has accumulated. Positive correction makes the clock run faster.

The formula for the RTC correction factor is as follows:

$$\text{CORRECTION [PPM]} = \frac{Y\_CALC0}{10} + \frac{Y\_CALC1}{100}\Delta T + \frac{Y\_CALC2}{1000}\Delta T^2$$

Where ***Y_CALC0*** = 10 * crystal frequency deviation from ideal (measured)
Y_CALC1 = 100 * crystal skew (nominally zero)
Y_CALC2 = 1000 * crystal frequency stability (specified)
ΔT = T - Calibration Temperature in °C

Calibration

Calibration Factors for CT and Resistive Shunt

Once installed in a meter, the TERIDIAN 71M6515H IC has to be calibrated for the tolerances of current sensors, voltage dividers and signal conditioning components. The room temperature reading of its temperature sensor must also be entered. These calibration factors must be stored by the host and, upon power up, loaded into the TERIDIAN 71M6515H. Typical calibration constants are listed in Table 4.

Name	Description
CAL_IA	Gain factors for current and voltage of each phase.
CAL_VA	
CAL_IB	
CAL_VB	
CAL_IC	
CAL_VC	
TEMP_NOM	The value of *TEMP_RAW* at nominal temperature.
PHADJ_A	Phase compensation for each current. If phase compensation is 0 or if current sensors have predictable phase, PHADJ may not need to be measured on every meter.
PHADJ_B	
PHADJ_C	

Table 4: Typical Calibration Parameters (CT)

Gain adjustment (*CAL_Xn* parameters) is used to compensate for tolerances of components used for signal conditioning, especially the resistive components. A 1% increase in *CAL_Xn* will cause a 1% increase in the channel gain.

The phase compensation circuit in the TERIDIAN 71M6515H is optimized for operation with current transformers (CT's). These devices have a low frequency pole and therefore have a slight amount of phase lead at 50 or 60Hz—more at 50Hz than at 60Hz. The phase lead diminishes at higher harmonics. When *PHADJ_n* is calibrated as shown below at either 50Hz or 60Hz, the CT will be correctly compensated from below 25Hz to beyond 1100Hz.

This phase compensator is markedly superior to the more common technique of programming a time delay to compensate for CT phase. The time delay technique results in phase compensation that is correct at only one frequency, and actually amplifies the phase error at harmonics of the frequency.

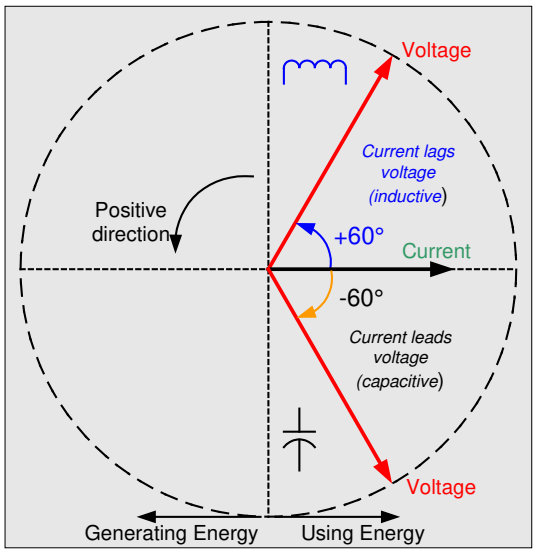
Calibration Factors for Rogowski Coil Sensors

If *IMAGE* is set to 01, i.e. the 71M6515H can be operated with Rogowski Coil sensors. In this case, one more calibration factor per phase is needed. The *PHADJ* parameters have non-zero defaults and do not obey the same formula used for CT calibration. The feedthrough parameter has to be determined by a separate crosstalk measurement. Table 5 shows the parameters involved in the calibration procedure for the Rogowski sensor.

Name	Description
CAL_IA	Gain constants for current and voltage of each phase.
CAL_VA	
CAL_IB	
CAL_VB	
CAL_IC	
CAL_VC	
TEMP_NOM	The value of *TEMP_RAW* at nominal temperature.
PHADJ_A	Phase compensation for each current. If phase compensation is 0 or if current sensors have predictable phase, *PHADJ* may not need to be measured on every meter.
PHADJ_B	
PHADJ_C	
VFEED_A	Feedthrough compensation for each current.
VFEED_B	
VFEED_C	

Table 5: Typical Calibration Parameters (Rogowski)

General Notes on Calibration



The calibration procedures described below should be followed after interfacing the voltage and current sensors to the 71M6515H chip. When properly interfaced, the V3P3 power supply is connected to the meter neutral and is the DC reference for each input. Each voltage and current waveform, as seen by the 6515H, is scaled to be less than 250mV (peak).

Each meter phase must be calibrated individually. The procedures below show how to calibrate a meter phase with either three or five measurements. Note that there is no need to calibrate for VARh if the Wh measurement is calibrated correctly. Note that positive load angles correspond to lagging current (see Figure 12).

For a typical calibration, a meter calibration system is used to apply a calibrated load, e.g. 240V at 30A, while interfacing the voltage and current sensors to the 71M6515H. This load should result in an observable pulse rate at the PULSEW output depending on the selected energy per pulse. For example, 7.2kW will result in an energy rate corresponding to 7200Wh/3600s = 2Wh/s, i.e., when 7.2kW are applied per phase (resulting in a total power of 21.6kW, equivalent to 6Wh/s) and a Kh of 3.2 (Wh/pulse) has been configured, a pulse rate of 6Wh/3.2Whs = 1.875Hz will be established.

Figure 12: Definition of Load Angles

It is entirely possible to calibrate piece-wise, i.e. in segments, to compensate for non-linear sensors. For example, one set of calibration factors can be applied by the host when the current is below 0.5A, while another set is applied when the current is at or above 0.5A.

Calibration Procedure for CT and Resistive Shunt

A typical meter has phase and gain errors as shown by ϕ_S, A_{XI}, and A_{XV} in Figure 13. Following the typical meter convention of current phase being in the lag direction, the small amount of phase lead in a typical current sensor is represented as $-\phi_S$. The errors shown in Figure 13 represent the sum of all gain and phase errors. They include errors in voltage attenuators, current sensors, signal conditioning circuits, and in ADC gains. In other words, no errors are made in the 'input' or 'meter' boxes.

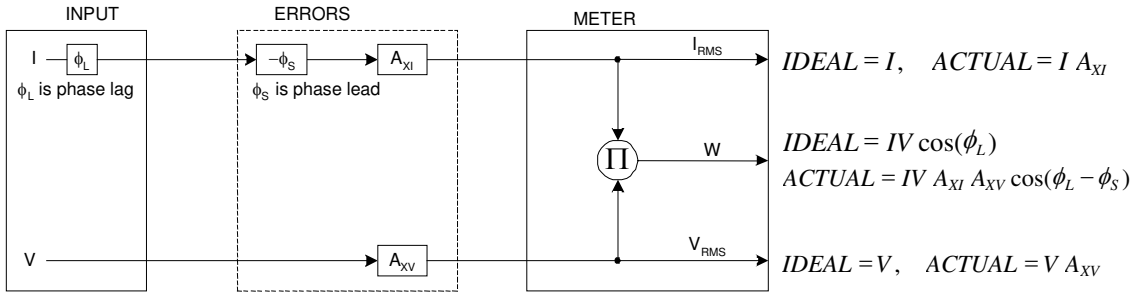


Figure 13: Watt Meter with Gain and Phase Errors.

During the calibration phase, we measure errors and then introduce correction factors to nullify their effect. With three unknowns to determine, we must make at least three measurements. If we make more measurements, we can average the results.