71M6531D/F, 71M6532D/F
Energy Meter IC

Simplifying System Integration^{TM}

DATA SHEET

June 2010

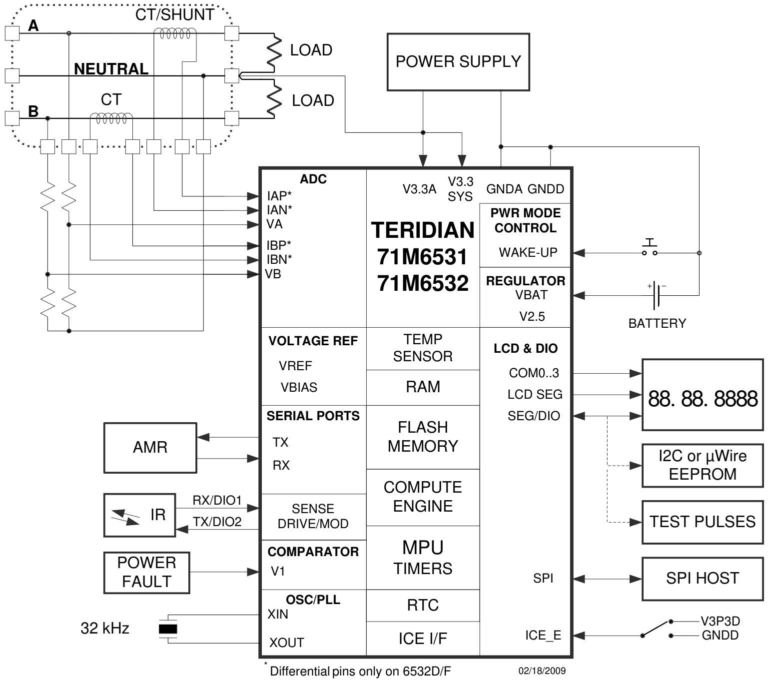
GENERAL DESCRIPTION

The Teridian 71M6531D/F and 71M6532D/F are highly integrated SOCs with an MPU core, RTC, FLASH and LCD driver. Teridian's patented Single Converter Technology® with a 22-bit delta-sigma ADC, four analog inputs, digital temperature compensation, precision voltage reference, battery voltage monitor and 32-bit computation engine (CE) supports a wide range of residential metering applications with very few low-cost external components.

A 32-kHz crystal time base for the entire system and internal battery backup support for RAM and RTC further reduce system cost. The IC supports 2-wire, and 3-wire single-phase and dual-phase residential metering along with tamper-detection mechanisms. The 71M6531D/F offers single-ended inputs for two current channels and two single-ended voltage inputs. The 71M6532D/F has two differential current inputs and three single-ended voltage inputs.

Maximum design flexibility is provided by multiple UARTs, I^{2}C, µWire, up to 21 DIO pins and in-system programmable FLASH memory, which can be updated with data or application code in operation.

A complete array of ICE and development tools, programming libraries and reference designs enable rapid development and certification of TOU, AMR and Prepay meters that comply with worldwide electricity metering standards.



FEATURES

- Wh accuracy < 0.1% over 2000:1 current range
- Exceeds IEC62053/ANSI C12.20 standards
- Four sensor inputs
- Low-jitter Wh and VARh plus two additional pulse test outputs (4 total, 10 kHz maximum) with pulse count
- Four-quadrant metering
- Tamper detection (Neutral current with CT, Rogowski or shunt, magnetic tamper input)
- Line frequency count for RTC
- Digital temperature compensation
- Sag detection for phase A and B
- Independent 32-bit compute engine
- 46-64 Hz line frequency range with same calibration. Phase compensation (± 7°)
- Three battery modes with wake-up on timer or push-button:
  - Brownout mode (52 µA typ.)
  - LCD mode (21 µA typ., DAC active)
  - Sleep mode (0.7 µA typ.)
- Energy display during mains power failure
- 39 mW typical consumption @ 3.3 V, MPU clock frequency 614 kHz
- 22-bit delta-sigma ADC with 3360 Hz or 2520 Hz sample rate
- 8-bit MPU (80515),1 clock cycle per instruction, 10 MHz maximum, with integrated ICE for debug
- RTC for TOU functions with clock-rate adjust register
- Hardware watchdog timer, power fail monitor
- LCD driver with 4 common segment drivers:
  - Up to 156 (71M6531D/F) or 268 pixels (71M6532D/F)
- Up to 22 (71M6531D/F) or 43 (71M6532D/F) general-purpose I/O pins. Digital I/O pins compatible with 5 V inputs
- 32 kHz time base
- High-speed slave SPI interface to data RAM
- Two UARTs for IR and AMR, IR driver with modulation
- FLASH memory with security and in-system program update:
  - 128 KB (71M6531D/32D)
  - 256 KB (71M6531F/32F)
- 4 KB MPU XRAM
- Industrial temperature range
- 68-pin QFN package for 71M6531D/F pin-compatible with 71M6521, 100-pin LQFP package for 71M6532D/F, lead free

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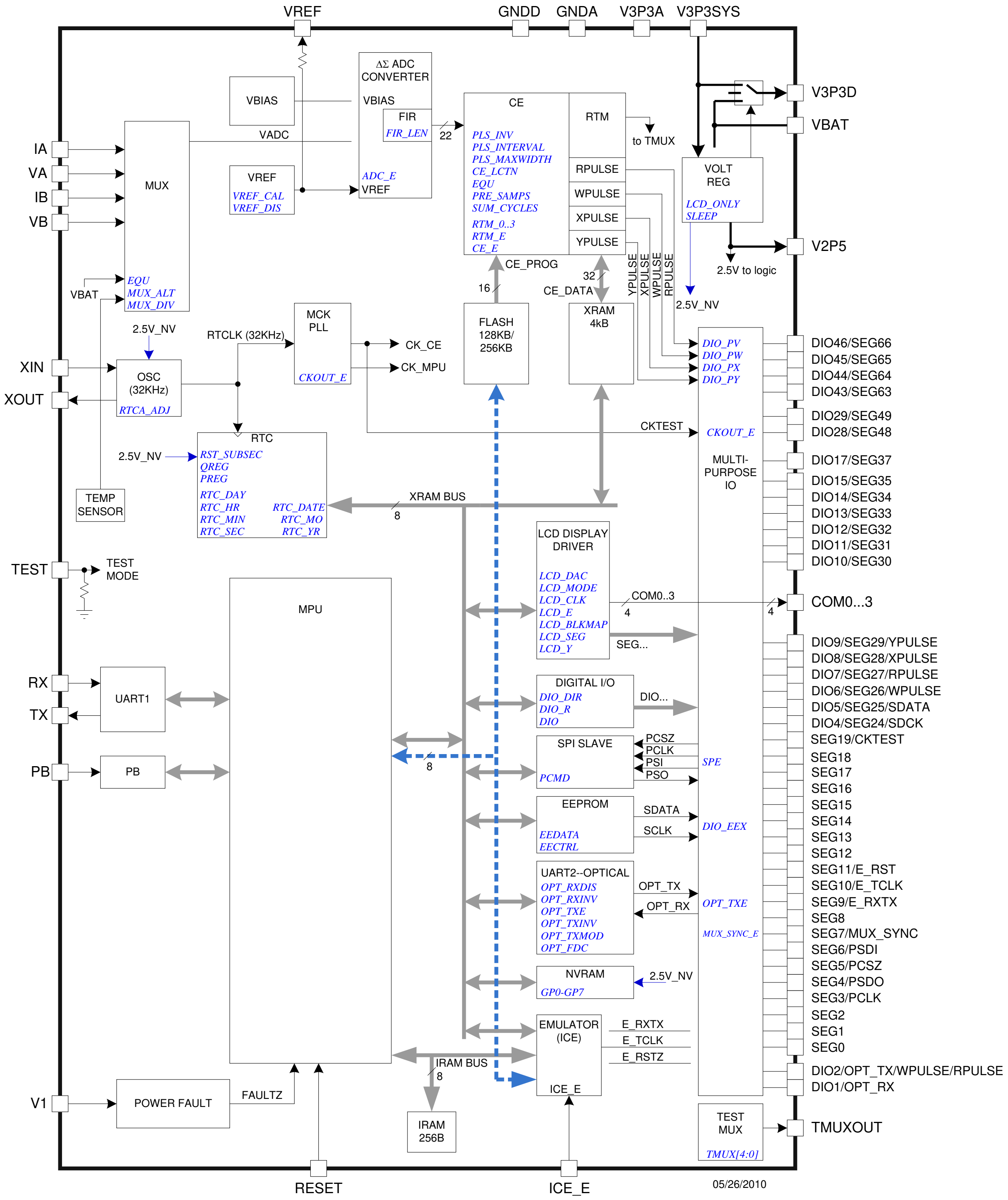

Figure 1: 71M6531D/F IC Functional Block Diagram

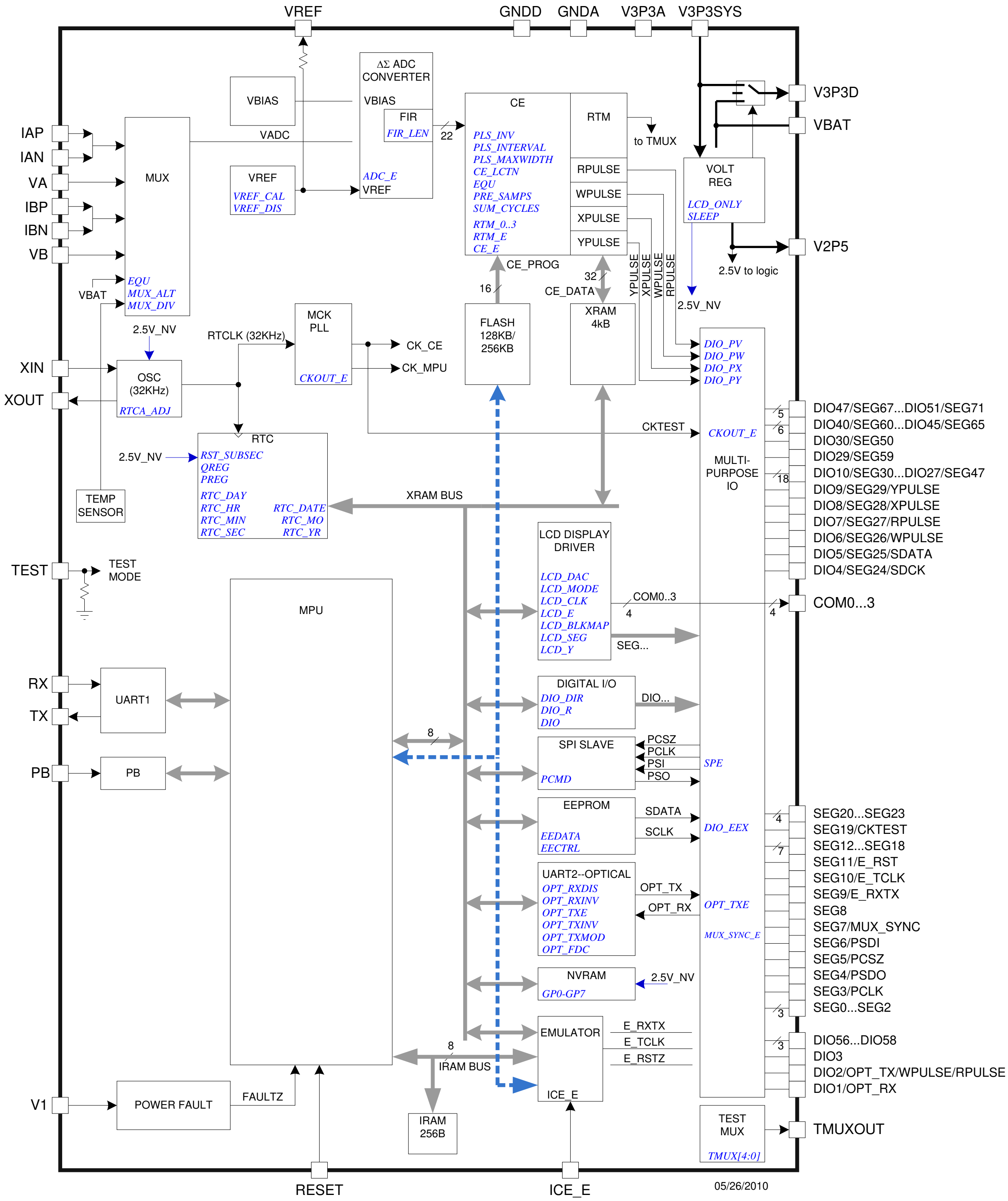

Figure 2: 71M6532D/F IC Functional Block Diagram

1 Hardware Description

1.1 Hardware Overview

The Teridian 71M6531D/F and 71M6532D/F single-chip energy meters integrates all primary functional blocks required to implement a solid-state electricity meter. Included on the chips are:

- An analog front end (AFE)
- An Independent digital computation engine (CE)
- An 8051-compatible microprocessor (MPU) which executes one instruction per clock cycle (80515)
- A voltage reference
- A temperature sensor
- LCD drivers
- RAM and Flash memory
- A real time clock (RTC)
- A variety of I/O pins

Various current sensor technologies are supported including Current Transformers (CT), Resistive Shunts and Rogowski coils.

In a typical application, the 32-bit compute engine (CE) of the 71M6531D/F and 71M6532D/F sequentially process the samples from the voltage inputs on pins IA, VA, IB, VB and performs calculations to measure active energy (Wh) and reactive energy (VARh), as well as A^2h and V^2h for four-quadrant metering. These measurements are then accessed by the MPU, processed further and output using the peripheral devices available to the MPU.

In addition to advanced measurement functions, the real time clock function allows the 71M6531D/F and 71M6532D/F to record time of use (TOU) metering information for multi-rate applications and to time-stamp tamper events. Measurements can be displayed on 3.3 V LCDs commonly used in low-temperature environments. Flexible mapping of LCD display segments facilitate integration of existing custom LCDs. Design trade-off between the number of LCD segments and DIO pins can be implemented in software to accommodate various requirements.

In addition to the temperature-trimmed ultra-precision voltage reference, the on-chip digital temperature compensation mechanism includes a temperature sensor and associated controls for correction of unwanted temperature effects on measurement and RTC accuracy, e.g. to meet the requirements of ANSI and IEC standards. Temperature-dependent external components such as a crystal oscillator, current transformers (CTs) and their corresponding signal conditioning circuits can be characterized and their correction factors can be programmed to produce electricity meters with exceptional accuracy over the industrial temperature range.

One of the two internal UARTs is adapted to support an Infrared LED with internal drive and sense configuration and can also function as a standard UART. The optical output can be modulated at 38 kHz. This flexibility makes it possible to implement AMR meters with an IR interface. A block diagram of the 71M6531D/F IC is shown in Figure 1. A block diagram of the 71M6532D/F IC is shown in Figure 2.

1.2 Analog Front End (AFE)

The AFE consists of an input multiplexer, a delta-sigma A/D converter and a voltage reference.

1.2.1 Signal Input Pins

All analog signal input pins are sensitive to voltage. In the 71M6531D/F, the VA and VB pins, as well as the IA and IB pins are single-ended. In the 71M6532D/F, the IAP/IAN and IBP/IBN pins can be programmed individually to be differential (see I/O RAM bit *SEL_IAN* and *SEL_IBN*) or single-ended. The differential signal is applied between the IAP and IAN input pins and between the IBP and IBN input pins. Single-ended signals are applied to the IAP and IBP input pins whereas the common signal, return, is the V3P3A pin. When using the differential mode, inputs can be chopped, i.e. a connection from V3P3A to IAP or IAN (or IBP an IBN, respectively) alternates in each multiplexer cycle.

1.2.2 Input Multiplexer

The input multiplexer supports up to four input signals that are applied to pins IA (IAP/IAN), VA, IB (IBP/IBN), and VB of the device. Additionally, using the alternate multiplexer selection, it has the ability to select temperature and the battery voltage. The multiplexer can be operated in two modes:

- During a normal multiplexer cycle, the signals from the IA (IAP/IAN), IB (IBP/IBN), VA and VB pins are selected.
- During the alternate multiplexer cycle, the temperature signal (TEMP) and the battery monitor are selected, along with some of the voltage and/or current signal sources shown in Table 1. To prevent unnecessary drainage on the battery, the battery monitor is only active when enabled with the *BME* bit (0x2020[6]) in the I/O RAM.

The alternate multiplexer cycles are usually performed infrequently (every second or so) by the MPU. In order to prevent disruption of the voltage tracking PLL and voltage allpass networks, VA is not replaced in the ALT selections. Table 1 details the regular and alternative multiplexer sequences. The computation engine (CE) fills in missing samples due to an ALT multiplexer sequence.

Table 1: Inputs Selected in Regular and Alternate Multiplexer Cycles

Time Slot	Regular Slot			Alternate Slot		
	Register	Typical Selections		Register	Typical Selections	
		RAM Address	Signal for ADC		RAM Address	Signal for ADC
0	*SLOT0_SEL[3:0]*	0	IA	*SLOT0_ALTSEL[3:0]*	A	**TEMP**
1	*SLOT1_SEL[3:0]*	1	VB	*SLOT1_ALTSEL[3:0]*	1	VB
2	*SLOT2_SEL[3:0]*	2	IB	*SLOT2_ALTSEL[3:0]*	B	**VBAT**
3	*SLOT3_SEL[3:0]*	3	VA	*SLOT3_ALTSEL[3:0]*	3	VA
–	*SLOT4_SEL[3:0]*	–	–	*SLOT4_ALTSEL[3:0]*	–	–
–	*SLOT5_SEL[3:0]*	–	–	*SLOT5_ALTSEL[3:0]*	–	–
–	*SLOT6_SEL[3:0]*	–	–	*SLOT6_ALTSEL[3:0]*	–	–
–	*SLOT7_SEL[3:0]*	–	–	*SLOT7_ALTSEL[3:0]*	–	–
–	*SLOT8_SEL[3:0]*	–	–	*SLOT8_ALTSEL[3:0]*	–	–
–	*SLOT9_SEL[3:0]*	–	–	*SLOT9_ALTSEL[3:0]*	–	–

The sequence of sampled channels is fully programmable using I/O RAM registers. *SLOTn_SEL[3:0]* selects the input for the nth state in a standard multiplexer frame, while *SLOTn_ALTSEL[3:0]* selects the input for the nth state in an alternate multiplexer frame. The states shown in Table 1 are examples for possible multiplexer state sequences.

In a typical application, IA (IAN/IAP) and IB (IBN/IBP) are connected to current transformers that sense the current on each phase of the line voltage. VA and VB are typically connected to voltage sensors through resistor dividers.

The multiplexer control circuit (MUX_CTRL signal) controls multiplexer advance, FIR initiation and VREF chopping. Additionally, MUX_CTRL launches each pass through the CE program. Conceptually, MUX_CTRL is clocked by CK32, the 32768 Hz clock from the PLL block. The behavior of MUX_CTRL is governed by *MUX_ALT*, *EQU[2:0]*, *CHOP_E[1:0]* and *MUX_DIV[3:0]*.

The *MUX_ALT* bit requests an alternative multiplexer frame. The bit may be asserted on any MPU cycle and may be subsequently de-asserted on any cycle including the next one. A rising edge on *MUX_ALT* will cause MUX_CTRL to wait until the next multiplexer frame and implement a single alternate multiplexer frame.

Another control input to the MUX is *MUX_DIV[3:0]*. These four bits can request from 1 to 10 multiplexer states per frame. The multiplexer always starts at the beginning of its list and proceeds until the number of states defined by *MUX_DIV[3:0]* have been converted.

The duration of each multiplexer state depends on the number of ADC samples processed by the FIR, which is set by *FIR_LEN[1:0]*. Each multiplexer state will start on the rising edge of CK32. The MUX_CTRL signal sends an FIR_START command to begin the calculation of a sample value from the ADC bit stream by the FIR. Upon receipt of the FIR_DONE signal from the FIR, the multiplexer will wait until the next CK32 rising edge to increment its state and initiate the next FIR conversion. FIR conversions require 1, 2, or 3 CK32 cycles. The number of CK32 cycles is determined by *FIR_LEN[1:0]*, as shown in Table 2.

1.2.3 A/D Converter (ADC)

A single delta-sigma A/D converter digitizes the voltage and current inputs to the 71M6531D/F and 71M6532D/F. The resolution of the ADC is programmable using the I/O RAM *M40MHZ* and *M26MHZ* bits (see Table 2). The CE code must be tailored for use with the selected ADC resolution.

Table 2: ADC Resolution

Setting for [*M40MHZ, M26MHZ*]	*FIR_LEN[1:0]*	CK32 Cycles	FIR CE Cycles	Resolution
[00], [10] or [11]	0	1	138	18 bits
	1	2	288	21 bits
	2	3	384	22 bits
[01]	0	1	186	19 bits
	1	2	384	22 bits
	2	3	588	24 bits

Initiation of each ADC conversion is controlled by MUX_CTRL as described above. At the end of each ADC conversion, the FIR filter output data is stored into the CE RAM location determined by the MUX selection.

1.2.4 FIR Filter

The finite impulse response filter is an integral part of the ADC and it is optimized for use with the multiplexer. The purpose of the FIR filter is to decimate the ADC output to the desired resolution. At the end of each ADC conversion, the output data is stored into the fixed CE RAM location determined by the multiplexer selection as shown in Table 3. FIR data is stored LSB justified, but shifted left by eight bits.

Table 3: ADC RAM Locations

Address (HEX)	Name	Address (HEX)	Name
0x00	IA	0x09	AUX
0x01	VB	0x0A	TEMP
0x02	IB	0x0B	VBAT
0x03	VA		

1.2.5 Voltage References

The device includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques. The reference is trimmed to minimize errors caused by component mismatch and drift. The result is a voltage output with a predictable temperature coefficient.

The amplifier within the reference is chopper stabilized, i.e. the polarity can be switched by the MPU using *CHOP_E[1:0]* (*IORAM 0x2002[5:4]*). The *CHOP_E[1:0]* field enables the MPU to operate the chopper circuit in regular or inverted operation, or in toggling mode. When the chopper circuit is toggled in between multiplexer cycles, DC offsets on the measured signals will automatically be averaged out.

The general topology of a chopped amplifier is shown in Figure 3.

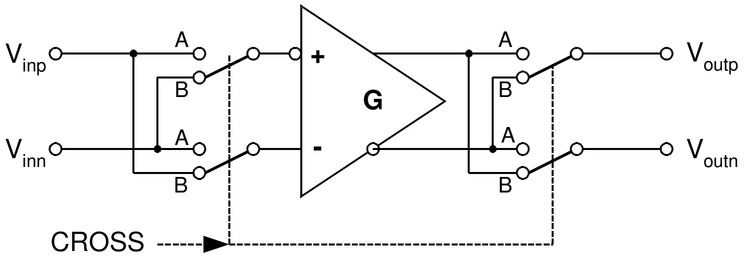

Figure 3: General Topology of a Chopped Amplifier

It is assumed that an offset voltage Voff appears at the positive amplifier input. With all switches, as controlled by CROSS, in the A position, the output voltage is:

Voutp – Voutn = G (Vinp + Voff – Vinn) = G (Vinp – Vinn) + G Voff

With all switches set to the B position by applying the inverted CROSS signal, the output voltage is:

Voutn – Voutp = G (Vinn – Vinp + Voff) = G (Vinn – Vinp) + G Voff, or

Voutp – Voutn = G (Vinp – Vinn) - G Voff

Thus, when CROSS is toggled, e.g. after each multiplexer cycle, the offset will alternately appear on the output as positive and negative, which results in the offset effectively being eliminated, regardless of its polarity or magnitude.

When CROSS is high, the connection of the amplifier input devices is reversed. This preserves the overall polarity of that amplifier gain; it inverts its input offset. By alternately reversing the connection, the amplifier's offset is averaged to zero. This removes the most significant long-term drift mechanism in the voltage reference. The *CHOP_E[1:0]* field controls the behavior of CROSS. The CROSS signal will reverse the amplifier connection in the voltage reference in order to negate the effects of its offset. On the first CK32 rising edge after the last multiplexer state of its sequence, the multiplexer will wait one additional CK32 cycle before beginning a new frame. At the beginning of this cycle, the value of CROSS will be updated according to the *CHOP_E[1:0]* field. The extra CK32 cycle allows time for the chopped VREF to settle. During this cycle, MUXSYNC is held high. The leading edge of MUXSYNC initiates a pass through the CE program sequence. The beginning of the sequence is the serial readout of the four RTM words.

CHOP_E[1:0] has four states: positive, reverse and two toggle states. In the positive state, *CHOP_E[1:0]* = 01, CROSS and CHOP_CLK are held low. In the reverse state, *CHOP_E[1:0]* = 10, CROSS and CHOP_CLK are held high. In the first toggle state, *CHOP_E[1:0]* = 00, CROSS is automatically toggled near the end of each multiplexer frame and an ALT frame is forced during the last multiplexer frame in each SUM cycle. It is desirable that CROSS take on alternate values during each ALT frame. For this reason, if *CHOP_E[1:0]* = 00, CROSS will not toggle at the end of the multiplexer frame immediately preceding the ALT frame in each accumulation interval.

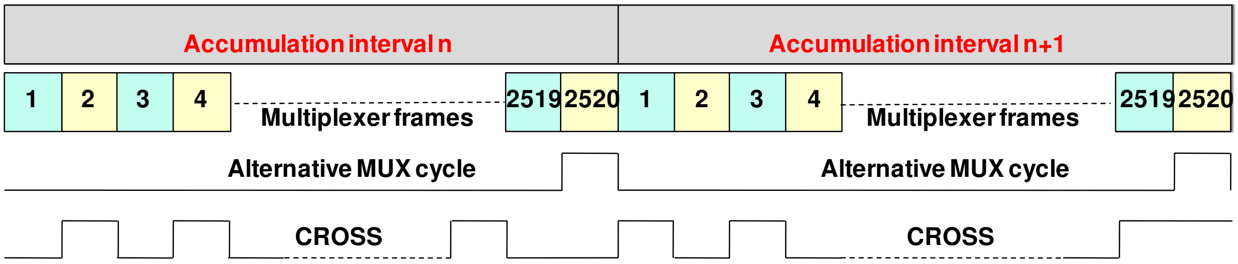

Figure 4: CROSS Signal with *CHOP_E[1:0]* = 00

Figure 4 shows CROSS over two accumulation interval when *CHOP_E[1:0]* = 00: At the end of the first interval, CROSS is low, at the end of the second interval, CROSS is high. The offset error for the two temperature measurements taken during the ALT multiplexer frames will be averaged to zero. Note that the number of multiplexer frames in an accumulation interval is always even. Operation with *CHOP_E[1:0]* = 00 does not require control of the chopping mechanism by the MPU while eliminating the offset for temperature measurement.

In the second toggle state, *CHOP_E[1:0]* = 11, no ALT frame is forced during the last multiplexer cycle in an accumulation interval and CROSS always toggles near the end of each multiplexer frame.

The internal bias voltage, VBIAS (typically 1.6 V), is used by the ADC when measuring the temperature and battery monitor signals.

1.2.6 Temperature Sensor

The 71M6531D/F and 71M6532D/F include an on-chip temperature sensor implemented as a bandgap reference. It is used to determine the die temperature. The MPU may request an alternate multiplexer cycle containing the temperature sensor output by asserting *MUX_ALT*.

The primary use of the temperature data is to determine the magnitude of compensation required to offset the thermal drift in the system (see Section 3.4 Temperature Compensation).

1.2.7 Battery Monitor

The battery voltage is measured by the ADC during alternative multiplexer frames if the *BME* (Battery Measure Enable) bit in the I/O RAM is set. While *BME* is set, an on-chip 45 kΩ load resistor is applied to the battery and a scaled fraction of the battery voltage is applied to the ADC input. After each alternative MUX frame, the result of the ADC conversion is available at XRAM address 0x0B. *BME* is ignored and assumed zero when system power is not available (V1 < VBIAS). See Section 5.4.4 Battery Monitor.

1.2.8 AFE Functional Description

The AFE functions as a data acquisition system, controlled by the MPU. The main signals (IA, VA, IB and VB) are sampled, and the ADC counts obtained are stored in XRAM where they can be accessed by the CE and, if necessary, by the MPU. Alternate multiplexer cycles are initiated less frequently by the MPU to gather access to the slow temperature and battery signals.

Figure 5 shows the block diagram of the AFE, with current inputs shown only as differential pair of pins (for the 71M6531D/F, the current input for phase A is a single pin [IA]).

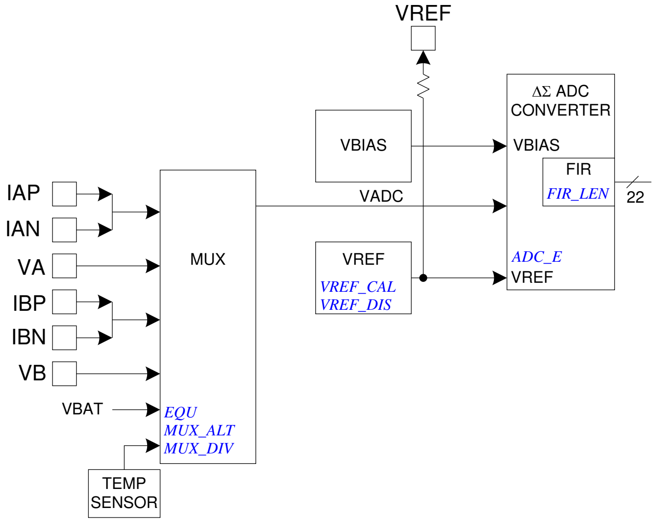

Figure 5: AFE Block Diagram (Shown for the 71M6532D/F)

1.3 Digital Computation Engine (CE)

The CE, a dedicated 32-bit signal processor, performs the precision computations necessary to accurately measure energy. The CE calculations and processes include:

- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied with the constant sample time).
- Frequency-insensitive delay cancellation on all four channels (to compensate for the delay between samples caused by the multiplexing scheme).
- 90° phase shifter (for VAR calculations).
- Pulse generation.
- Monitoring of the input signal frequency (for frequency and phase information).
- Monitoring of the input signal amplitude (for sag detection).
- Scaling of the processed samples based on calibration coefficients.
- Scaling of all samples based on temperature compensation information (71M6532D/F only).

The CE program resides in flash memory. Common access to flash memory by CE and MPU is controlled by a memory share circuit. Each CE instruction word is two bytes long. Allocated flash space for the CE program cannot exceed 4096 16-bit words (8 KB). The CE program counter begins a pass through the CE code each time multiplexer state 0 begins. The code pass ends when a HALT instruction is executed. For proper operation, the code pass must be completed before the multiplexer cycle ends (see Section 2.2 System Timing Summary).

The CE program must begin on a 1-KB boundary of the flash address. The I/O RAM register *CE_LCTN[7:0]* defines which 1-KB boundary contains the CE code. Thus, the first CE instruction is located at 1024**CE_LCTN[7:0]*.

The CE can access up to 4 KB of data RAM (XRAM), or 1024 32-bit data words, starting at RAM address 0x0000.

The XRAM can be accessed by the FIR filter block, the RTM circuit, the CE, and the MPU. Assigned time slots are reserved for FIR, and MPU, respectively, to prevent bus contention for XRAM data access.

The MPU can read and write the XRAM as the primary means of data communication between the two processors. Table 4 shows the CE addresses in XRAM allocated to analog inputs from the AFE.

Table 4: XRAM Locations for ADC Results

Address (HEX)	Name	Description
0x00	IA	Phase A current
0x01	VA	Phase A voltage
0x02	IB	Phase B current
0x03	VB	Phase B voltage
0x04...0x09	–	Not used
0x0A	TEMP	Temperature
0x0B	VBAT	Battery Voltage

The CE is aided by support hardware to facilitate implementation of equations, pulse counters and accumulators. This hardware is controlled through I/O RAM locations *EQU[2:0]* (equation assist), the *DIO_PV* and *DIO_PW* (pulse count assist) bits and *PRE_SAMPS[1:0]* and *SUM_CYCLES[5:0]* (accumulation assist).

PRE_SAMPS[1:0] and *SUM_CYCLES[5:0]* support a dual level accumulation scheme where the first accumulator accumulates results from *PRE_SAMPS[1:0]* samples and the second accumulator accumulates up to *SUM_CYCLES[5:0]* of the first accumulator results. The integration time for each energy output is *PRE_SAMPS[1:0]* * *SUM_CYCLES[5:0]*/2520.6 (with *MUX_DIV[3:0]* = 1). The CE hardware issues the XFER_BUSY interrupt when the accumulation is complete.

1.3.1 Meter Equations

The 71M6531D/F and 71M6532D/F provide hardware assistance to the CE in order to support various meter equations. This assistance is controlled through I/O RAM location *EQU[2:0]* (equation assist). The Compute Engine (CE) firmware for residential configurations implements the equations listed in Table 5. *EQU[2:0]* specifies the equation to be used based on the number of phases used for metering.

Table 5: Meter Equations

EQU[2:0]	Description	Watt and VAR Formula			Mux Sequence	ALT Mux Sequence
		Element 0	**Element 1**	**Element 2**		
0	1 element, 2 W, 1ϕ with neutral current sense	VA · IA	VA · IB	N/A	Sequence is programmable with *SLOTn_SEL[3:0]*	Sequence is programmable with *SLOTn_ALTSEL[3:0]*
1	1 element, 3 W, 1ϕ	VA(IA-IB)/2	N/A	N/A		
2	2 element, 3 W, 3ϕ Delta	VA · IA	VB · IB	N/A		

✓ Not all CE codes support all equations.

1.3.2 Real-Time Monitor

The CE contains a Real-Time Monitor (RTM), which can be programmed to monitor four selectable XRAM locations at full sample rate. The four monitored locations are serially output to the TMUXOUT pin via the digital output multiplexer at the beginning of each CE code pass. The RTM can be enabled and disabled with the *RTM_E* bit. The RTM output is clocked by CKTEST (pin SEG19/CKTEST), with the clock output enabled by setting *CKOUT_E* = 1. Each RTM word is clocked out in 35 cycles and contains a leading flag bit. See Figure 20 for the RTM output format. RTM is low when not in use.

1.3.3 Pulse Generators

The 71M6531D/F and 71M6532D/F provide four pulse generators, RPULSE, WPULSE, XPULSE and YPULSE, as well as increased hardware support for the two original pulse generators (RPULSE and WPULSE). The pulse generators can be used to output CE status indicators, SAG for example, to DIO pins.

The polarity of the pulses may be inverted with the *PLS_INV* bit. When this bit is set, the pulses are active high, rather than the more usual active low. *PLS_INV* inverts all the pulse outputs.

XPULSE and YPULSE

Pulses generated by the CE may be exported to the XPULSE and YPULSE pulse outputs. Pins DIO8 and DIO9 are used for these pulses. Generally, the XPULSE and YPULSE outputs are updated once on each pass of the CE code, resulting in a pulse frequency up to a maximum of 1260Hz (assuming a MUX frame is 13 CK32 cycles).

The YPULSE pin can be used by the CE code to generate interrupts based on sag events. This method is faster than checking the sag bits by the MPU at every CE_BUSY interrupt. See Section 4.3.6 CE Status and Control for details.

RPULSE and WPULSE

During each CE code pass, the hardware stores exported WPULSE AND RPULSE sign bits in an 8-bit FIFO and outputs them at a specified interval. This permits the CE code to calculate the RPULSE and WPULSE outputs at the beginning of its code pass and to rely on hardware to spread them over the MUX frame. The FIFO is reset at the beginning of each MUX frame. The *PLS_INTERVAL* register controls the delay to the first pulse update and the interval between subsequent updates. Its LSB is 4 CK_FIR cycles. If zero, the FIFO is deactivated and the DFFs are updated immediately. Thus, NINTERVAL is 4 * *PLS_INTERVAL*.

Since the FIFO resets at the beginning of each MUX frame, the user must specify *PLS_INTERVAL* so that all of the pulse updates are output before the MUX frame completes. For instance, if the CE code outputs 5 updates per MUX interval and if the MUX interval is 1950 cycles long, the ideal value for the interval is 1950/5/4 = 97.5. If *PLS_INTERVAL* = 98, the fifth output will occur too late and be lost. In this case, the proper value for *PLS_INTERVAL* is 97.

Hardware also provides a maximum pulse width feature. The *PLS_MAXWIDTH* register selects a maximum negative pulse width to be Nmax updates according to the formula: Nmax = (2**PLS_MAXWIDTH*+1). If *PLS_MAXWIDTH* = 255, no width checking is performed.

The WPULSE and RPULSE pulse generator outputs are available on DIO6 and DIO7, respectively. They can also be output on OPT_TX (see *OPT_TXE[1:0]* for details).

1.3.4 Data RAM (XRAM)

The CE and MPU use a single general-purpose Data RAM (also referred to as XRAM). The Data RAM is 1024 32-bit words, shared between the CE and the MPU using a time-multiplex method. This reduces MPU wait states when accessing CE data. When the MPU and CE are clocking at maximum frequency (10 MHz), the DRAM will make up to four accesses during each 100 ns interval. These consist of two MPU accesses, one CE access and one SPI access.

The Data RAM is 32 bits wide and uses an external multiplexer so as to appear byte-wide to the MPU. The Data RAM hardware will convert an MPU byte write operation into a read-modify-write operation that requires two Data RAM accesses. The second access is guaranteed to be available because the MPU cannot access the XRAM on two consecutive instructions unless it is using the same address.

In addition to the reduction of wait states, this arrangement permits the MPU to easily use unneeded CE data memory. Likewise, the amount of memory the CE uses is not limited by the size of a dedicated CE data RAM.

1.3.5 Delay Compensation

When measuring the energy of a phase (i.e., Wh and VARh) in a service, the voltage and current for that phase must be sampled at the same instant. Otherwise, the phase difference, Φ, introduces errors.

$$\phi = \frac{t_{delay}}{T} \cdot 360^o = t_{delay} \cdot f \cdot 360^o$$

Where f is the frequency of the input signal and t_{delay} is the sampling delay between voltage and current.

In traditional meter ICs, sampling is accomplished by using two A/D converters per phase (one for voltage and the other one for current) controlled to sample simultaneously. Teridian's patented Single-Converter Technology®, however, exploits the 32-bit signal processing capability of its CE to implement "constant delay" all-pass filters. These all-pass filters correct for the conversion time difference between the voltage and the corresponding current samples that are obtained with a single multiplexed A/D converter.

The "constant delay" all-pass filters provide a broad-band delay β, that is precisely matched to the difference in sample time between the voltage and the current of a given phase. This digital filter does not affect the amplitude of the signal, but provides a precisely controlled phase response. The delay compensation implemented in the CE aligns the voltage samples with their corresponding current samples by routing the voltage samples through the all-pass filter, thus delaying the voltage samples by β, resulting in the residual phase error β – Φ. The residual phase error is negligible, and is typically less than ±1.5 milli-degrees at 100Hz, thus it does not contribute to errors in the energy measurements.

1.3.6 CE Functional Overview

The ADC processes one sample per channel per multiplexer cycle. Figure 6 shows the timing of the samples taken during one multiplexer cycle.

The number of samples processed during one accumulation cycle is controlled by *PRE_SAMPS[1:0]* (*IORAM 0x2001[7:6]*) and *SUM_CYCLES[5:0] (IORAM 0x2001[5:0]*). The integration time for each energy output is:

PRE_SAMPS[1:0] * *SUM_CYCLES[5:0]* / 2520.6, where 2520.6 is the sample rate [Hz]

For example, *PRE_SAMPS[1:0]* = 42 and *SUM_CYCLES[5:0]* = 50 will establish 2100 samples per accumulation cycle. *PRE_SAMPS[1:0]* = 100 and *SUM_CYCLES[5:0]* = 21 will result in the exact same accumulation cycle of 2100 samples or 833 ms. After an accumulation cycle is completed, the XFER_BUSY interrupt signals to the MPU that accumulated data are available.

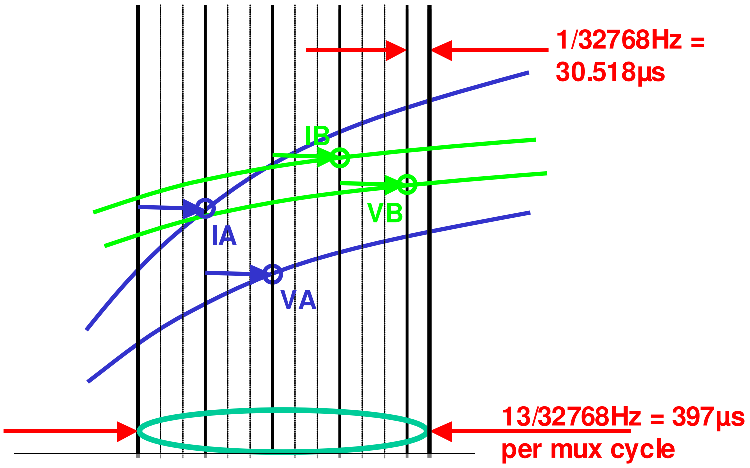

Figure 6: Samples from Multiplexer Cycle

The end of each multiplexer cycle is signaled to the MPU by the CE_BUSY interrupt. At the end of each multiplexer cycle status information, such as sag data and the digitized input signal, is available to the MPU.

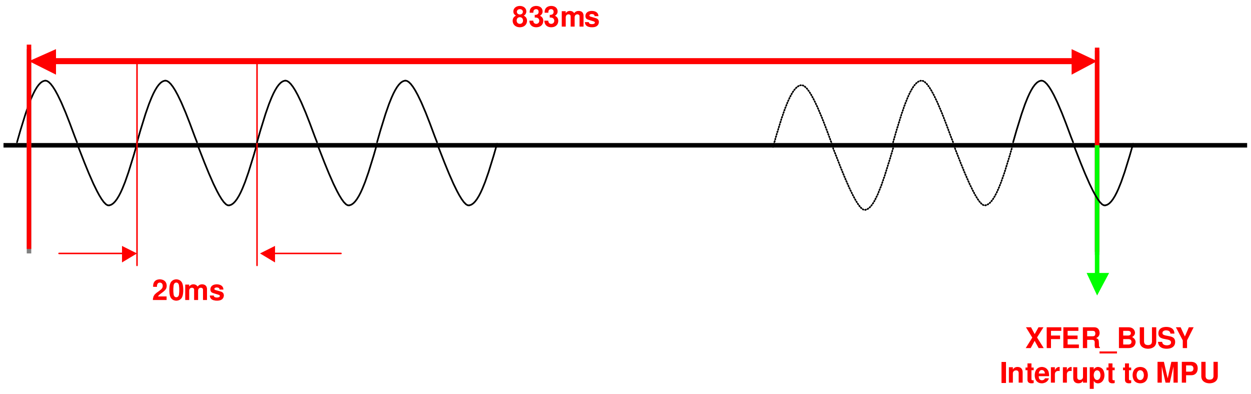

Figure 7: Accumulation Interval

Figure 7 shows the accumulation interval resulting from *PRE_SAMPS[1:0]* = 42 and *SUM_CYCLES[5:0]* = 50, consisting of 2100 samples of 397 µs each, followed by the XFER_BUSY interrupt. The sampling in this example is applied to a 50 Hz signal.

There is no correlation between the line signal frequency and the choice of *PRE_SAMPS[1:0]* or *SUM_CYCLES[5:0]* (even though when *SUM_CYCLES[5:0]* = 42 one set of *SUM_CYCLES[5:0]* happens to sample a period of 16.6 ms). Furthermore, sampling does not have to start when the line voltage crosses the zero line and the length of the accumulation interval need not be an integer multiple of the signal cycles.

1.4 80515 MPU Core

The 71M6531D/F and 71M6532D/F include an 80515 MPU (8-bit, 8051-compatible) that processes most instructions in one clock cycle. Using a 10-MHz clock results in a processing throughput of 10 MIPS. The 80515 architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Normally, a machine cycle is aligned with a memory fetch, therefore, most of the 1-byte instructions are performed in a single machine cycle (MPU clock cycle). This leads to an 8x average performance improvement (in terms of MIPS) over the Intel® 8051 device running at the same clock frequency.

Table 6 shows the CKMPU frequency as a function of the allowed combinations of the MPU clock divider *MPU_DIV[2:0]* and the MCK divider bits *M40MHZ* and *M26MHZ*. Actual processor clocking speed can be adjusted to the total processing demand of the application (metering calculations, AMR management, memory management, LCD driver management and I/O management) using the I/O RAM field *MPU_DIV[2:0]* and the MCK divider bits *M40MHZ* and *M26MHZ*, as shown in Table 6.

Table 6: CKMPU Clock Frequencies

MPU_DIV [2:0]	[*M40MHZ, M26MHZ*] Values		
	[1,0]	[0,1]	[0,0]
000	9.8304 MHz	6.5536 MHz	4.9152 MHz
001	4.9152 MHz	3.2768 MHz	2.4576 MHz
010	2.4576 MHz	1.6384 MHz	1.2288 MHz
011	1.2288 MHz	819.2 kHz	614.4 kHz
100	614.4 kHz	409.6 kHz	307.2 kHz
101	307.2 kHz	204.8 kHz	153.6 kHz
110	153.6 kHz	102.4 kHz	76.80 kHz
111	153.6 kHz	102.4 kHz	76.8 kHz

Typical measurement and metering functions based on the results provided by the internal 32-bit compute engine (CE) are available for the MPU as part of Teridian's standard library. Teridian provides demonstration source code to help reduce the design cycle.

1.4.1 Memory Organization and Addressing

The 80515 MPU core incorporates the Harvard architecture with separate code and data spaces. Memory organization in the 80515 is similar to that of the industry standard 8051. There are four memory areas: Program memory (Flash, shared by MPU and CE), external RAM (Data RAM, shared by the CE and MPU, Configuration or I/O RAM), and internal data memory (Internal RAM). Table 7 shows the memory map.

Program Memory

The 80515 can address up to 64 KB of program memory space from 0x0000 to 0xFFFF. Program memory is read when the MPU fetches instructions or performs a MOVC operation. Access to program memory above 0x7FFF is controlled by the *FL_BANK[2:0]* register (SFR 0xB6).

After reset, the MPU starts program execution from program memory location 0x0000. The lower part of the program memory includes reset and interrupt vectors. The interrupt vectors are spaced at 8-byte intervals, starting from 0x0003.

MPU External Data Memory (XRAM)

Both internal and external memory is physically located on the 71M6531 device. The external memory referred to in this documentation is only external to the 80515 MPU core.

4 KB of RAM starting at address 0x0000 is shared by the CE and MPU. The CE normally uses the first 1 KB, leaving 3 KB for the MPU. Different versions of the CE code use varying amounts. Consult the documentation for the specific code version being used for the exact limit.

✓ If the MPU overwrites the CE's working RAM, the CE's output may be corrupted. If the CE is disabled, the first 0x40 bytes of RAM are still unusable while *MUX_DIV[3:0]* ≠ 0 because the 71M6531 ADC writes to these locations. Setting *MUX_DIV[3:0]* = 0 disables the ADC output preventing the CE from writing the first 0x40 bytes of RAM.

The 80515 writes into external data memory when the MPU executes a MOVX @Ri,A or MOVX @DPTR,A instruction. The MPU reads external data memory by executing a MOVX A,@Ri or MOVX A,@DPTR instruction (SFR *PDATA* provides the upper 8 bytes for the MOVX A,@Ri instruction).

Internal and External Memory Map

Table 7 shows the address, type, use and size of the various memory components.

✓ Only the memory ranges shown in Table 7 contain physical memory.

Table 7: Memory Map

Address (hex)	Memory Technology	Memory Type	Name	Typical Usage	Memory Size (bytes)
00000-1FFFF/ 00000-3FFFF	Flash Memory	Non-volatile	Program memory for MPU and CE	MPU Program and non-volatile data	128 KB/ 256 KB[†]
				CE program (on 1 KB boundary)	8 KB max.
0000-0FFF	Static RAM	Volatile	External RAM (XRAM)	Shared by CE and MPU	4 KB
2000-20BF, 20C8-20FF	Static RAM	Volatile	Configuration RAM, I/O RAM	Hardware control	256
20C0-20C7	Static RAM	Non-volatile (battery)	Configuration RAM, I/O RAM	Battery-buffered memory	8
0000-00FF	Static RAM	Volatile	Internal RAM	Part of 80515 Core	256

[†] Memory size depends on the IC. See Section1.5.5 Physical Memory for details.

MOVX Addressing

There are two types of instructions differing in whether they provide an 8-bit or 16-bit indirect address to the external data RAM.

In the first type, MOVX A,@Ri, the contents of R0 or R1 in the current register bank provide the eight lower-ordered bits of address. The eight high-ordered bits of the address are specified with the *PDATA* SFR. This method allows the user paged access (256 pages of 256 bytes each) to all ranges of the external data RAM.

In the second type of MOVX instruction, MOVX A,@DPTR, the data pointer generates a 16-bit address. This form is faster and more efficient when accessing very large data arrays (up to 64 KB), since no additional instructions are needed to set up the eight high ordered bits of the address.

It is possible to mix the two MOVX types. This provides the user with four separate data pointers, two with direct access and two with paged access, to the entire 64 KB of external memory range.

Dual Data Pointer

The Dual Data Pointer accelerates the block moves of data. The standard *DPTR* is a 16-bit register that is used to address external memory or peripherals. In the 80515 core, the standard data pointer is called *DPTR*, the second data pointer is called *DPTR1*. The data pointer select bit, located in the LSB of the *DPS* register (*DPS*[0]), chooses the active pointer. *DPTR* is selected when *DPS*[0] = 0 and *DPTR1* is selected when *DPS*[0] = 1.

The user switches between pointers by toggling the LSB of the *DPS* register. The values in the data pointers are not affected by the LSB of the *DPS* register. All *DPTR* related instructions use the currently selected *DPTR* for any activity.

✓ The second data pointer may not be supported by certain compilers.

💡 *DPTR1* is useful for copy routines, where it can make the inner loop of the routine two instructions faster compared to the reloading of *DPTR* from registers. Any interrupt routine using *DPTR1* must save and restore *DPS*, *DPTR* and *DPTR1*, which increases stack usage and slows down interrupt latency.

💡 By selecting the Evatronics R80515 core in the Keil compiler project settings and by using the compiler directive “MODC2”, dual data pointers are enabled in certain library routines.

An alternative data pointer is available in the form of the *PDATA* register (SFR 0xBF), sometimes referred to as *USR2*). It defines the high byte of a 16-bit address when reading or writing XDATA with the instruction MOVX A,@Ri or MOVX @Ri,A.

Internal Data Memory Map and Access

The Internal data memory provides 256 bytes (0x00 to 0xFF) of data memory. The internal data memory address is always 1 byte wide. Table 8 shows the internal data memory map.

The Special Function Registers (SFR) occupy the upper 128 bytes. The SFR area of internal data memory is available only by direct addressing. Indirect addressing of this area accesses the upper 128 bytes of Internal RAM. The lower 128 bytes contain working registers and bit addressable memory. The lower 32 bytes form four banks of eight registers (R0-R7). Two bits on the program memory status word (*PSW*) select which bank is in use. The next 16 bytes form a block of bit addressable memory space at bit addresses 0x00-0x7F. All of the bytes in the lower 128 bytes are accessible through direct or indirect addressing.

Table 8: Internal Data Memory Map

Address Range		Direct addressing	Indirect addressing
0x80	0xFF	Special Function Registers (SFRs)	RAM
0x30	0x7F	Byte addressable area	
0x20	0x2F	Bit addressable area	
0x00	0x1F	Register banks R0…R7	

1.4.2 Special Function Registers (SFRs)

A map of the Special Function Registers is shown in Table 9.

Only a few addresses in the SFR memory space are occupied, the others are not implemented. A read access to unimplemented addresses will return undefined data, while a write access will have no effect. SFRs specific to the 71M6531D/F and 71M6532D/F are shown in **bold** print on a gray field. The registers at 0x80, 0x88, 0x90, etc., are bit addressable, all others are byte addressable. See the restrictions for the *INTBITS* register in Table 14.

Table 9: Special Function Register Map

Hex/ Bin	Bit Addressable	Byte Addressable							Bin/ Hex
	X000	X001	X010	X011	X100	X101	X110	X111	
F8	***INTBITS***								FF
F0	*B*								F7
E8	***IFLAGS***								EF
E0	*A*								E7
D8	*WDCON*								DF
D0	*PSW*								D7
C8	*T2CON*								CF
C0	*IRCON*								C7
B8	*IEN1*	*IP1*	*S0RELH*	*S1RELH*				*PDATA*	BF
B0	***P3***		***FLSHCTL***				***FL_BANK***	***PGADR***	B7
A8	*IEN0*	*IP0*	*S0RELL*						AF
A0	***P2***	***DIR2***	***DIR0***						A7
98	*S0CON*	*S0BUF*	*IEN2*	*S1CON*	*S1BUF*	*S1RELL*	***EEDATA***	***EECTRL***	9F
90	***P1***	***DIR1***	*DPS*		***ERASE***				97
88	*TCON*	*TMOD*	*TL0*	*TL1*	*TH0*	*TH1*	*CKCON*		8F
80	*P0*	*SP*	*DPL*	*DPH*	*DPL1*	*DPH1*		*PCON*	87

1.4.3 Generic 80515 Special Function Registers

Table 10 shows the location, description and reset or power-up value of the generic 80515 SFRs. Additional descriptions of the registers can be found at the page numbers listed in the table.

Table 10: Generic 80515 SFRs - Location and Reset Values

Name	Address (Hex)	Reset value (Hex)	Description	Page
P0	0x80	0xFF	Port 0	24
SP	0x81	0x07	Stack Pointer	23
DPL	0x82	0x00	Data Pointer Low 0	23
DPH	0x83	0x00	Data Pointer High 0	23
DPL1	0x84	0x00	Data Pointer Low 1	23
DPH1	0x85	0x00	Data Pointer High 1	23
PCON	0x87	0x00	UART Speed Control, Idle and Stop mode Control	28
TCON	0x88	0x00	Timer/Counter Control	31
TMOD	0x89	0x00	Timer Mode Control	29
TL0	0x8A	0x00	Timer 0, low byte	28
TL1	0x8B	0x00	Timer 1, high byte	28
TH0	0x8C	0x00	Timer 0, low byte	28
TH1	0x8D	0x00	Timer 1, high byte	28
CKCON	0x8E	0x01	Clock Control (Stretch=1)	24
P1	0x90	0xFF	Port 1	23
DPS	0x92	0x00	Data Pointer select Register	20
S0CON	0x98	0x00	Serial Port 0, Control Register	27
S0BUF	0x99	0x00	Serial Port 0, Data Buffer	26
IEN2	0x9A	0x00	Interrupt Enable Register 2	31
S1CON	0x9B	0x00	Serial Port 1, Control Register	27
S1BUF	0x9C	0x00	Serial Port 1, Data Buffer	26
S1RELL	0x9D	0x00	Serial Port 1, Reload Register, low byte	26
P2	0xA0	0xFF	Port 2	23
IEN0	0xA8	0x00	Interrupt Enable Register 0	30
IP0	0xA9	0x00	Interrupt Priority Register 0	33
S0RELL	0xAA	0xD9	Serial Port 0, Reload Register, low byte	26
P3	0xB0	0xFF	Port 3	23
IEN1	0xB8	0x00	Interrupt Enable Register 1	31
IP1	0xB9	0x00	Interrupt Priority Register 1	33
S0RELH	0xBA	0x03	Serial Port 0, Reload Register, high byte	26
S1RELH	0xBB	0x03	Serial Port 1, Reload Register, high byte	26
PDATA	0xBF	0x00	High address byte for MOVX@Ri - also called *USR2*	20
IRCON	0xC0	0x00	Interrupt Request Control Register	31
T2CON	0xC8	0x00	Polarity for INT2 and INT3	31
PSW	0xD0	0x00	Program Status Word	23
WDCON	0xD8	0x00	Baud Rate Control Register (only WDCON[7] bit used)	26
A	0xE0	0x00	Accumulator	23
B	0xF0	0x00	B Register	23

Accumulator (*ACC, A, SFR 0xE0*):

ACC is the accumulator register. Most instructions use the accumulator to hold the operand. The mnemonics for accumulator-specific instructions refer to accumulator as *A*, not *ACC*.

***B* Register (*SFR 0xF0*):**

The *B* register is used during multiply and divide instructions. It can also be used as a scratch-pad register to hold temporary data.

Program Status Word (*PSW, SFR 0xD0*):

This register contains various flags and control bits for the selection of the register banks (see Table 11).

Table 11: *PSW* Bit Functions (*SFR 0xD0*)

<table>
<tr><th><i>PSW</i> Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>7</td><td><i>CV</i></td><td>Carry flag.</td></tr>
<tr><td>6</td><td><i>AC</i></td><td>Auxiliary Carry flag for BCD operations.</td></tr>
<tr><td>5</td><td><i>F0</i></td><td>General-purpose Flag 0 available for user.
✓ F0 is not to be confused with the F0 flag in the <i>CESTATUS</i> register.</td></tr>
<tr><td>4</td><td><i>RS1</i></td><td rowspan="2">Register bank select control bits. The contents of <i>RS1</i> and <i>RS0</i> select the working register bank:
<table>
<tr><th><i>RS1/RS0</i></th><th>Bank selected</th><th>Location</th></tr>
<tr><td>00</td><td>Bank 0</td><td>0x00 – 0x07</td></tr>
<tr><td>01</td><td>Bank 1</td><td>0x08 – 0x0F</td></tr>
<tr><td>10</td><td>Bank 2</td><td>0x10 – 0x17</td></tr>
<tr><td>11</td><td>Bank 3</td><td>0x18 – 0x1F</td></tr>
</table></td></tr>
<tr><td>3</td><td><i>RS0</i></td></tr>
<tr><td>2</td><td><i>OV</i></td><td>Overflow flag.</td></tr>
<tr><td>1</td><td>-</td><td>User defined flag.</td></tr>
<tr><td>0</td><td><i>P</i></td><td>Parity flag, affected by hardware to indicate odd or even number of one bits in the Accumulator, i.e. even parity.</td></tr>
</table>

Stack Pointer (*SP, SFR 0x81*):

The stack pointer is a 1-byte register initialized to 0x07 after reset. This register is incremented before PUSH and CALL instructions, causing the stack to begin at location 0x08.

Data Pointer:

The data pointers (*DPTR* and *DPRT1*) are 2 bytes wide. The lower part is *DPL(SFR 0x82)* and *DPL1 (SFR0x84)* and the highest is *DPH (SFR0x83)* and *DPH1 (SFR 0x85)*. The data pointers can be loaded as two registers (e.g. MOV DPL,#data8). They are generally used to access external code or data space (e.g. MOVC A,@A+DPTR or MOVX A,@DPTR respectively).

Program Counter:

The program counter (*PC*) is 2 bytes wide and initialized to 0x0000 after reset. The *PC* is incremented when fetching operation code or when operating on data from program memory.

Port Registers:

The I/O ports are controlled by Special Function Registers *P0*, *P1* and *P2* as shown in Table 12. The contents of the SFR can be observed on corresponding pins on the chip. Writing a 1 to any of the ports causes the corresponding pin to be at high level (V3P3). Writing a 0 causes the corresponding pin to be held at a low level (GND). The data direction registers *DIR0*, *DIR1* and *DIR2* define individual pins as input or output pins (see Sections 1.5.7 Digital I/O – 71M6531D/F or 1.5.8 Digital I/O – 71M6532D/F).

Table 12: Port Registers

Register	SFR Address	R/W	Description
P0	0x80	R/W	Register for port 0 read and write operations.
DIR0	0xA2	R/W	Data direction register for port 0. Setting a bit to 1 indicates that the corresponding pin is an output.
P1	0x90	R/W	Register for port 1 read and write operations.
DIR1	0x91	R/W	Data direction register for port 1.
P2	0xA0	R/W	Register for port 2 read and write operations.
DIR2	0xA1	R/W	Data direction register for port 2.

All DIO ports on the chip are bi-directional. Each of them consists of a Latch (SFR *P0* to *P2*), an output driver and an input buffer, therefore the MPU can output or read data through any of these ports. Even if a DIO pin is configured as an output, the state of the pin can still be read by the MPU, for example when counting pulses issued via DIO pins that are under CE control.

The technique of reading the status of or generating interrupts based on DIO pins configured as outputs can be used to implement pulse counting.

Clock Stretching (*CKCON[2:0], SFR 0x8E*)

The *CKCON[2:0]* field defines the stretch memory cycles that could be used for MOVX instructions when accessing slow external peripherals. The practical value of this register for the 71M653x is to guarantee access to XRAM between CE, MPU, and SPI. The default setting of *CKCON[2:0]* (001) should not be changed.Table 13 shows how the signals of the External Memory Interface change when stretch values are set from 0 to 7. The widths of the signals are counted in MPU clock cycles. The post-reset state of the *CKCON[2:0]* field (001), which is shown in **bold** in the table, performs the MOVX instructions with a stretch value equal to 1.

Table 13: Stretch Memory Cycle Width

CKCON[2:0]	Stretch Value	Read signal width		Write signal width	
		memaddr	memrd	memaddr	memwr
000	0	1	1	2	1
001	**1**	**2**	**2**	**3**	**1**
010	2	3	3	4	2
011	3	4	4	5	3
100	4	5	5	6	4
101	5	6	6	7	5
110	6	7	7	8	6
111	7	8	8	9	7

1.4.4 Special Function Registers (SFRs) Specific to the 71M6531D/F and 71M6532D/F

Table 14 shows the location and description of the SFRs specific to the 71M6531D/F and 71M6532D/F.

Table 14: 71M6531D/F and 71M6532D/F Specific SFRs

Register (Alternate Name)	SFR Address	Bit Field Name	R/W	Description
EEDATA	0x9E		R/W	I^{2}C EEPROM interface data register.
EECTRL	0x9F		R/W	I^{2}C EEPROM interface control register. See Section 1.5.14 EEPROM Interface for a description of the command and status bits available for *EECTRL*.

Register (Alternate Name)	SFR Address	Bit Field Name	R/W	Description
ERASE *(FLSH_ERASE)*	0x94		W	This register is used to initiate either the Flash Mass Erase cycle or the Flash Page Erase cycle. See the Flash Memory section for details.
FL_BANK	0xB6[2:0]		R/W	Flash Bank Selection.
PGADDR *(FLSH_PGADR[5:0])*	0xB7		R/W	Flash Page Erase Address register. Contains the flash memory page address (page 0 through page 127) that will be erased during the Page Erase cycle (default = 0x00). Must be re-written for each new Page Erase cycle.
FLSHCRL	0xB2[0]	*FLSH_PWE*	R/W	Program Write Enable: 0: MOVX commands refer to XRAM Space, normal operation (default). 1: MOVX @DPTR,A moves A to Program Space (Flash) @ DPTR.
	0xB2[1]	*FLSH_MEEN*	W	Mass Erase Enable: 0: Mass Erase disabled (default). 1: Mass Erase enabled. Must be re-written for each new Mass Erase cycle.
	0xB2[6]	*SECURE*	R/W	Enables security provisions that prevent external reading of flash memory and CE program RAM. This bit is reset on chip reset and may only be set. Attempts to write zero are ignored.
	0xB2[7]	*PREBOOT*	R	Indicates that the preboot sequence is active.
IFLAGS	0xE8[0]	*IE_XFER*	R/W	This flag monitors the XFER_BUSY interrupt. It is set by hardware and must be cleared by the interrupt handler.
	0xE8[1]	*IE_RTC*	R/W	This flag monitors the RTC_1SEC interrupt. It is set by the hardware and must be cleared by the interrupt handler.
	0xE8[2]	*FWCOL1*	R/W	This flag indicates that a flash write was in progress while the CE was busy.
	0xE8[3]	*FWCOL0*	R/W	This flag indicates that a flash write was attempted when the CE was attempting to begin a code pass.
	0xE8[4]	*IE_PB*	R/W	This flag indicates that the wake-up pushbutton was pressed.
	0xE8[5]	*IE_WAKE*	R/W	This flag indicates that the MPU was awakened by the autowake timer.
	0xE8[6]	*PLL_RISE*	R/W	PLL_RISE Interrupt Flag: Write 0 to clear the *PLL_RISE* interrupt flag.
	0xE8[7]	*PLL_FALL*	R/W	PLL_FALL Interrupt Flag: Write 0 to clear the *PLL_FALL* interrupt flag.
INTBITS (*INT0 … INT6*)	0xF8[6:0]	*INT6 … INT0*	R	Interrupt inputs. The MPU may read these bits to see the status of external interrupts *INT0* up to *INT6*. These bits do not have any memory and are primarily intended for debug use.
	0xF8[7]	*WD_RST*	W	The WDT is reset when a 1 is written to this bit.
	✓ Only byte operations on the entire *INTBITS* register should be used when writing. The byte must have all bits set except the bits that are to be cleared.			