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19-5376; Rev 2; 11/11

# 71M6541D/F/G and 71M6542F/G Energy Meter ICs

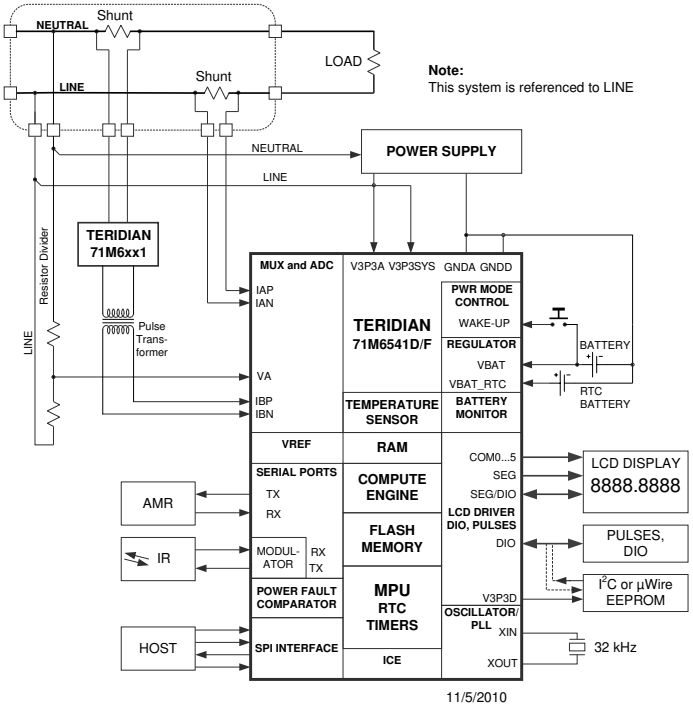
**DATA SHEET**

## GENERAL DESCRIPTION

The 71M6541D/71M6541F/71M6541G/71M6542F/71M6542G are Teridian™ 4th-generation single-phase metering SoCs with a 5MHz 8051-compatible MPU core, low-power RTC with digital temperature compensation, flash memory, and LCD driver. Our Single Converter Technology® with a 22-bit delta-sigma ADC, three or four analog inputs, digital temperature compensation, precision voltage reference, and a 32-bit computation engine (CE) supports a wide range of metering applications with very few external components.

The 71M6541/2 devices support optional interfaces to the Teridian 71M6x01 series of isolated sensors, which offer BOM cost reduction, immunity to magnetic tamper, and enhanced reliability. Other features include an SPI interface, advanced power management, ultra-low-power operation in active and battery modes, 3/5KB shared RAM and 32/64/128KB of flash memory that can be programmed in the field with code and/or data during meter operation and the ability to drive up to six LCD segments per SEG driver pin. High processing and sampling rates combined with differential inputs offer a powerful metering platform for residential meters.

A complete array of code development tools, demonstration code, and reference designs enable rapid development and certification of meters that meet all ANSI and IEC electricity metering standards worldwide.




*Teridian is a trademark and Single Converter Technology is a registered trademark of Maxim Integrated Products, Inc.*
*MICROWIRE is a registered trademark of National Semiconductor Corp.*

## FEATURES

- 0.1% Accuracy Over 2000:1 Current Range
- Exceeds IEC 62053/ANSI C12.20 Standards
- Two Current Sensor Inputs with Selectable Differential Mode
- Selectable Gain of 1 or 8 for One Current Input to Support Shunts
- High-Speed Wh/VARh Pulse Outputs with Programmable Width
- 32KB Flash, 3KB RAM (71M6541D)
- 64KB Flash, 5KB RAM (71M6541F/42F)
- 128KB Flash, 5KB RAM (71M6541G/42G)
- Up to Four Pulse Outputs with Pulse Count
- Four-Quadrant Metering
- Digital Temperature Compensation:
  - Metrology Compensation
  - Accurate RTC for TOU Functions with Automatic Temperature Compensation for Crystal in All Power Modes
- Independent 32-Bit Compute Engine
- 46-64Hz Line Frequency Range with the Same Calibration
- Phase Compensation (±10°)
- Three Battery-Backup Modes:
  - Brownout Mode (BRN)
  - LCD Mode (LCD)
  - Sleep Mode (SLP)
- Wake-Up on Pin Events and Wake-On Timer
- 1µA in Sleep Mode
- Flash Security
- In-System Program Update
- 8-Bit MPU (80515), Up to 5 MIPS
- Full-Speed MPU Clock in Brownout Mode
- LCD Driver:
  - Up to 6 Commons/Up to 56 Pins
- 5V LCD Driver with DAC
- Up to 51 Multifunction DIO Pins
- Hardware Watchdog Timer (WDT)
- $I^2C$/MICROWIRE® EEPROM Interface
- SPI Interface with Flash Program Capability
- Two UARTs for IR and AMR
- IR LED Driver with Modulation
- Industrial Temperature Range
- 64-Pin (71M6541D/F/G) and 100-pin (71M6542F/G) Lead(Pb)-Free LQFP Package

**For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.**

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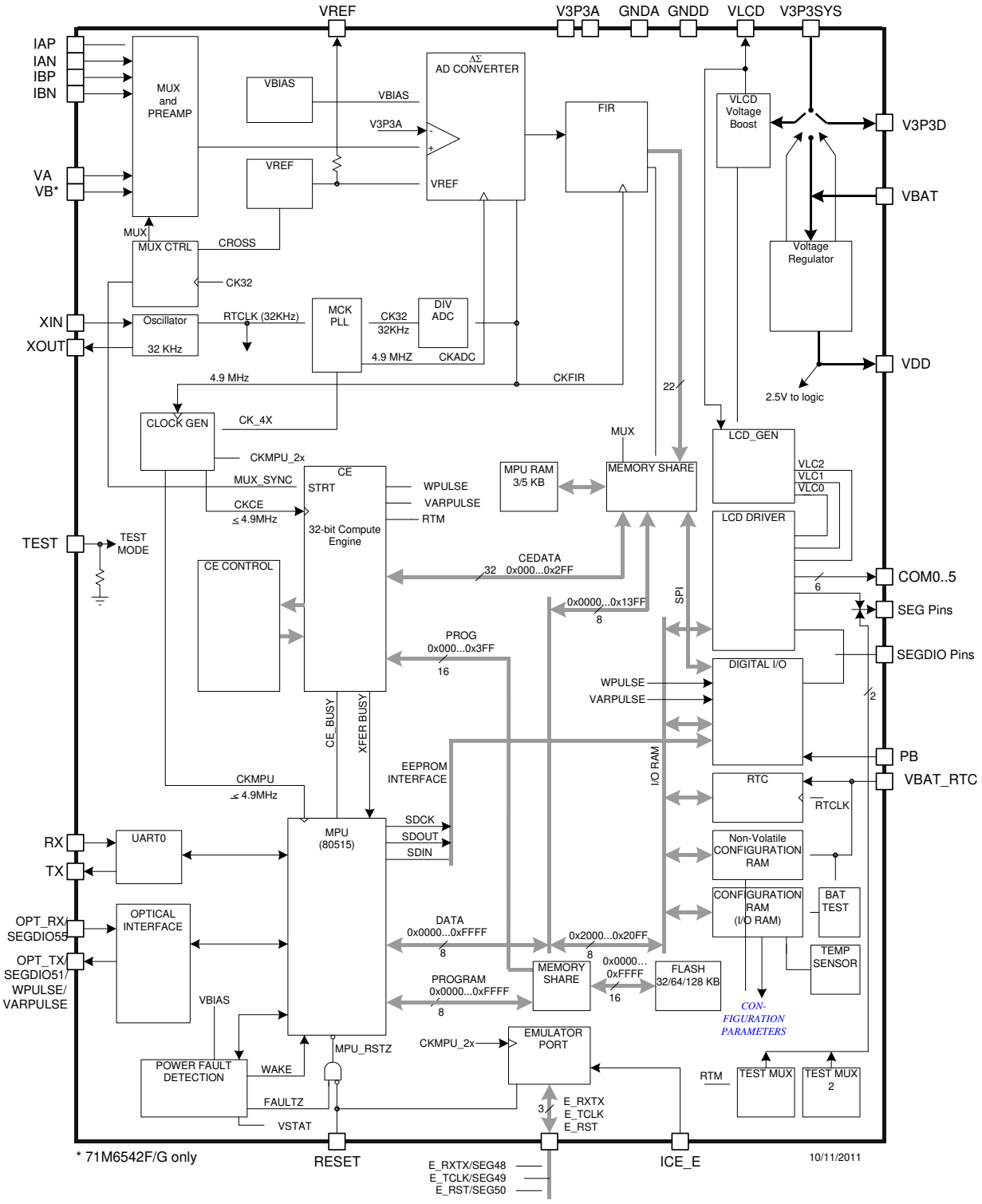


**Figure 1: IC Functional Block Diagram**

# 1 Introduction

This data sheet covers the 71M6541D (32KB), 71M6541F (64KB), 71M6541G (128KB), 71M6542F (64KB), and 71M6542G (128KB) fourth generation Teridian energy measurement SoCs. The term "71M654x" is used when discussing a device feature or behavior that is applicable to all four part numbers. The appropriate part number is indicated when a device feature or behavior is being discussed that applies only to a specific part number. This data sheet also covers basic details about the companion 71M6x01 isolated current sensor device. For more complete information on the 71M6x01 sensors, refer to the 71M6xxx Data Sheet.

This document covers the use of the 71M654x with locally connected sensors as well when it is used in conjunction with the 71M6x01 isolated current sensor. The 71M654x and 71M6x01 chipset make it possible to use one non-isolated and one isolated shunt current sensor to create single-phase and two-phase energy meters using inexpensive shunt resistors, while achieving unprecedented performance with this type of sensor technology. The 71M654x SoCs also support configurations involving one locally connected shunt and one locally connected Current Transformer (CT), or two CTs.

To facilitate document navigation, hyperlinks are often used to reference figures, tables and section headings that are located in other parts of the document. All hyperlinks in this document are highlighted in blue. Hyperlinks are used extensively to increase the level of detail and clarity provided within each section by referencing other relevant parts of the document. To further facilitate document navigation, this document is published as a PDF document with bookmarks enabled.

The reader is also encouraged to obtain and review the documents listed in 8 Related Information on page 163 of this document.

# 2 Hardware Description

## 2.1 Hardware Overview

The Teridian 71M6541D/F/G and 71M6542F/G single-chip energy meter ICs integrate all primary functional blocks required to implement a solid-state residential electricity meter. Included on the chip are:

- An analog front end (AFE) featuring a 22-bit second-order sigma-delta ADC
- An independent 32-bit digital computation engine (CE) to implement DSP functions
- An 8051-compatible microprocessor (MPU) which executes one instruction per clock cycle (80515)
- A precision voltage reference (VREF)
- A temperature sensor for digital temperature compensation:
  - Metrology digital temperature compensation (MPU)
  - Automatic RTC digital temperature compensation operational in all power states
- LCD drivers
- RAM and Flash memory
- A real time clock (RTC)
- A variety of I/O pins
- A power failure interrupt
- A zero-crossing interrupt
- Selectable current sensor interfaces for locally-connected sensors as well as isolated sensors (i.e., using the 71M6x01 companion IC with a shunt resistor sensor)
- Resistive Shunt and Current Transformers are supported

Resistive Shunts and Current Transformers (CT) current sensors are supported. Resistive shunt current sensors may be connected directly to the 71M654x device or isolated using a companion 71M6x01 isolator IC in order to implement a variety of single-phase / split-phase (71M6541D/F/G) or two-phase (71M6542F/G) metering configurations. An inexpensive, small size pulse transformer is used to isolate the 71M6x01 isolated sensor from the 71M654x. The 71M654x performs digital communications bi-directionally with the 71M6x01 and also provides power to the 71M6x01 through the isolating pulse transformer. Isolated (remote) shunt current sensors are connected to the differential input of the 71M6x01. Included on the 71M6x01 companion isolator chip are:

- Digital isolation communications interface
- An analog front end (AFE)
- A precision voltage reference (VREF)
- A temperature sensor (for digital temperature compensation)
- A fully differential shunt resistor sensor input
- A pre-amplifier to optimize shunt current sensor performance
- Isolated power circuitry obtains dc power from pulses sent by the 71M654x

In a typical application, the 32-bit compute engine (CE) of the 71M654x sequentially processes the samples from the voltage inputs on analog input pins and from the external 71M6x01 isolated sensors and performs calculations to measure active energy (Wh) and reactive energy (VARh), as well as $A^2h$, and $V^2h$ for four-quadrant metering. These measurements are then accessed by the MPU, processed further and output using the peripheral devices available to the MPU.

In addition to advanced measurement functions, the clock function allows the 71M6541D/F/G and 71M6542F/G to record time-of-use (TOU) metering information for multi-rate applications and to time-stamp tamper or other events. Measurements can be displayed on 3.3 V LCDs commonly used in low-temperature environments. An on-chip charge pump is available to drive 5 V LCDs. Flexible mapping of LCD display segments facilitate integration of existing custom LCDs. Design trade-off between the number of LCD segments and DIO pins can be implemented in software to accommodate various requirements.

In addition to the temperature-trimmed ultra-precision voltage reference, the on-chip digital temperature compensation mechanism includes a temperature sensor and associated controls for correction of unwanted temperature effects on measurement and RTC accuracy, e.g., to meet the requirements of ANSI and IEC

standards. Temperature-dependent external components such as crystal oscillator, resistive shunts, current transformers (CTs) and their corresponding signal conditioning circuits can be characterized and their correction factors can be programmed to produce electricity meters with exceptional accuracy over the industrial temperature range.

One of the two internal UARTs is adapted to support an Infrared LED with internal drive and sense configuration and can also function as a standard UART. The optical output can be modulated at 38 kHz. This flexibility makes it possible to implement AMR meters with an IR interface. A block diagram of the IC is shown in Figure 1.

## 2.2 Analog Front End (AFE)

The AFE functions as a data acquisition system, controlled by the MPU. When used with locally connected sensors, as seen in Figure 2, the analog input signals (IAP-IAN, VA and IBP-IBN) are multiplexed to the ADC input and sampled by the ADC. The ADC output is decimated by the FIR filter and stored in CE RAM where it can be accessed and processed by the CE.

See Figure 6 for the multiplexer sequence corresponding to Figure 2. See Figure 35 for the meter configuration corresponding to Figure 2.

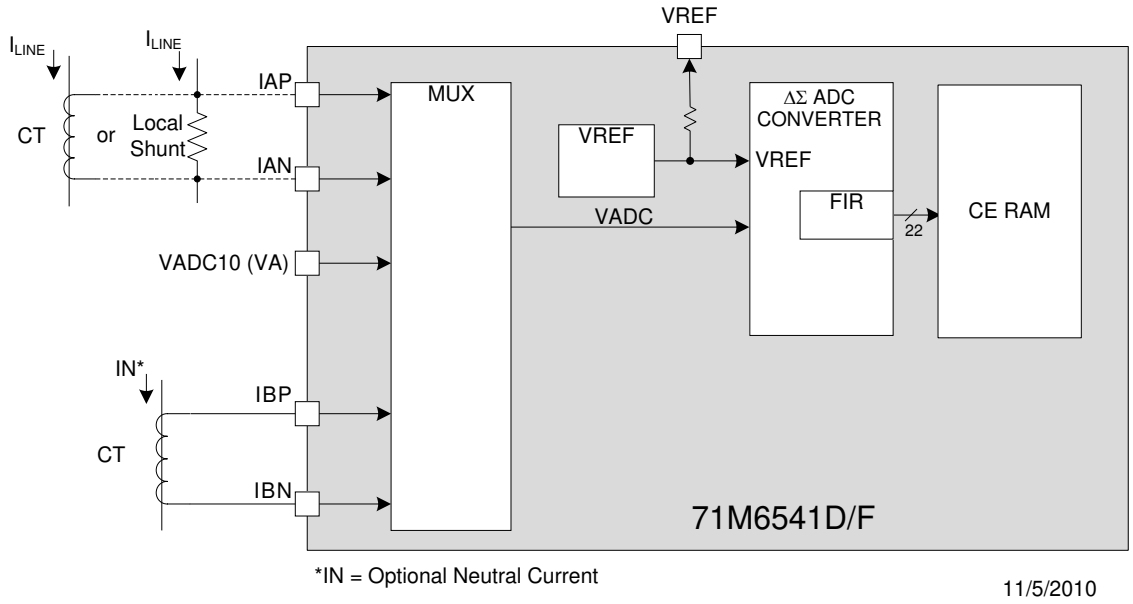


**Figure 2. 71M6541D/F/G AFE Block Diagram (Local Sensors)**

Figure 3 shows the 71M6541D/F/G multiplexer interface with one local and one remote resistive shunt sensor. As seen in Figure 3, when a remote isolated shunt sensor is connected via the 71M6x01, the samples associated with this current channel are not routed to the multiplexer, and are instead transferred digitally to the 71M6541D/F/G via the digital isolation interface and are directly stored in CE RAM.

See Figure 6 for the multiplexer timing sequence corresponding to Figure 3. See Figure 36 for the meter configurations corresponding to Figure 3.

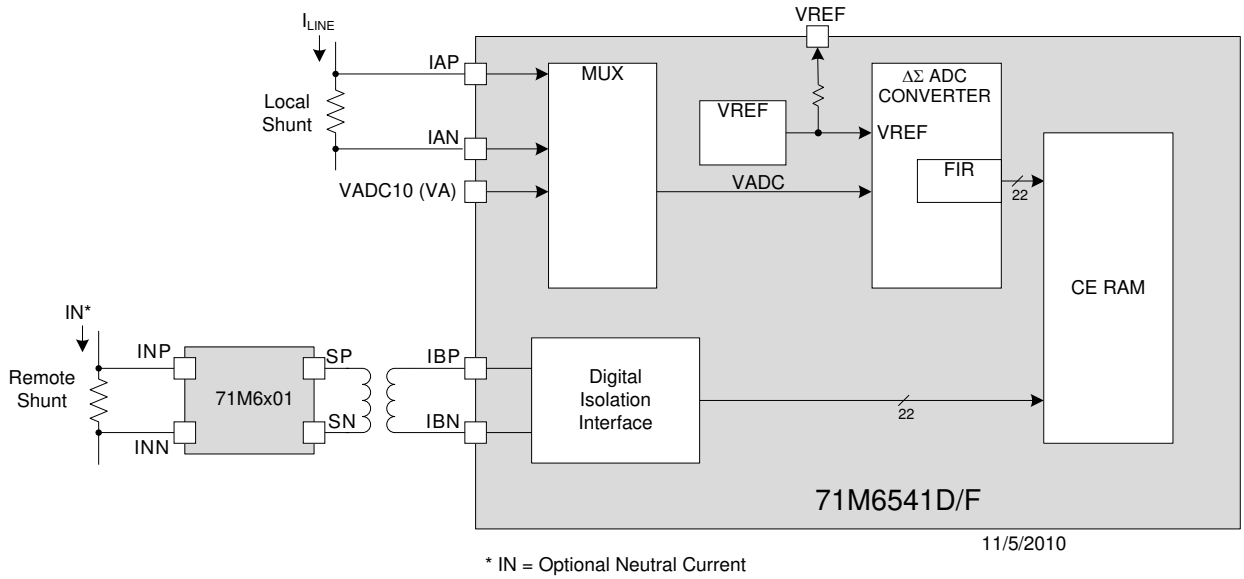


**Figure 3. 71M6541D/F/G AFE Block Diagram with 71M6x01**

Figure 4 shows the 71M6542F/G AFE with locally connected sensors. The analog input signals (IAP-IAN, VA, IBP-IBN and VB) are multiplexed to the ADC input and sampled by the ADC. The ADC output is decimated by the FIR filter and stored in CE RAM where it can be accessed and processed by the CE.

See Figure 7 for the multiplexer timing sequence corresponding to Figure 4. See Figure 37 for the meter configuration corresponding to Figure 4.

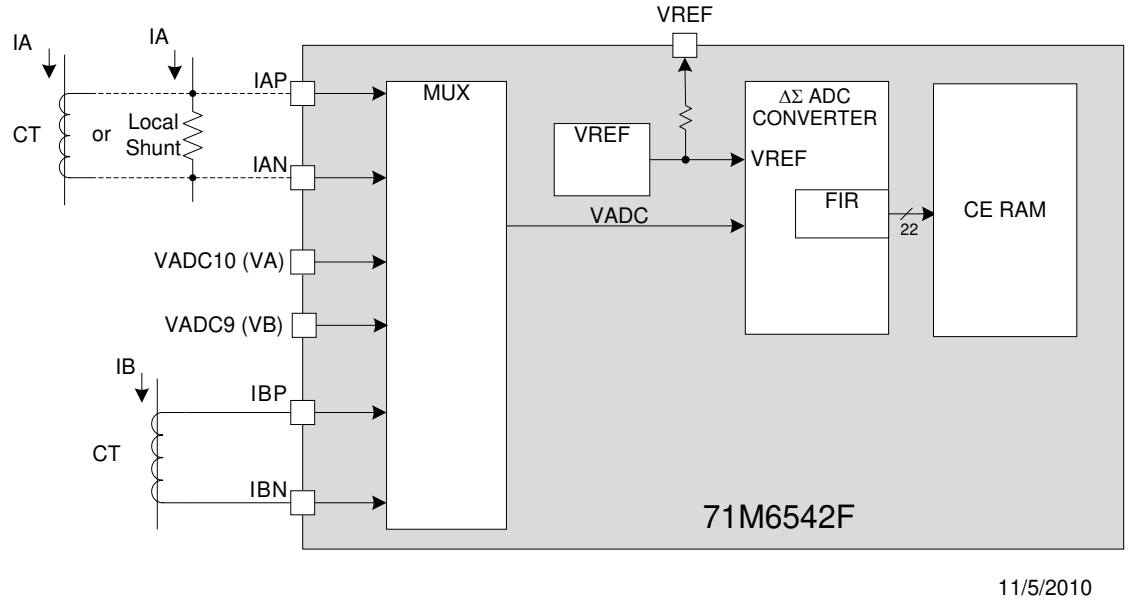


**Figure 4. 71M6542F/G AFE Block Diagram (Local Sensors)**

Figure 5 shows the 71M6542F/G multiplexer interface with one local and one remote resistive shunt sensor. As seen in Figure 5, when a remote isolated shunt sensor is connected via the 71M6x01, the samples associated with this current channel are not routed to the multiplexer, and are instead transferred digitally to the 71M6542F/G via the digital isolation interface and are directly stored in CE RAM.

See Figure 6 for the multiplexer timing sequence corresponding to Figure 5. See Figure 38 for the meter configurations corresponding to Figure 5.

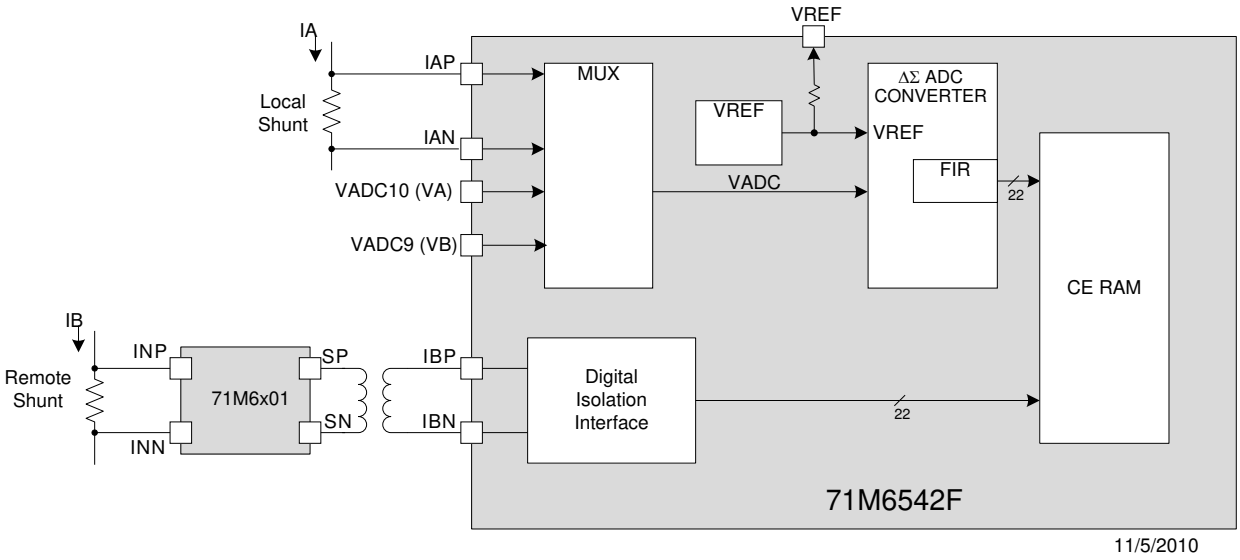


**Figure 5. 71M6542F/G AFE Block Diagram with 71M6x01**

### 2.2.1 Signal Input Pins

The 71M6541D/F/G features five ADC inputs. The 71M6542F/G features six ADC inputs.

IAP-IAN and IBP-IBN are intended for use as current sensor inputs. These four current sensor inputs can be configured as four single-ended inputs, or can be paired to form two differential inputs. For best performance, it is recommended to configure the current sensor inputs as differential inputs (i.e., IAP-IAN and IBP-IBN). The first differential input (IAP-IAN) features a pre-amplifier with a selectable gain of 1 or 8, and is intended for direct connection to a shunt resistor sensor, and can also be used with a Current Transformer (CT). The remaining differential pair (i.e., IBP-IBN) may be used with CTs, or may be enabled to interface to a remote 71M6x01 isolated current sensor providing isolation for a shunt resistor sensor using a low cost pulse transformer.

The remaining input in the 71M6541D/F/G (VA) is single-ended, and is intended for sensing the line voltage in a single-phase meter application using Equation 0 or 1 (see 2.3.4 Meter Equations on page 25). The 71M6542F/G features an additional single-ended voltage sensing input (VB) to support bi-phase applications using Equation 2. These single-ended inputs are referenced to the V3P3A pin.

All analog signal input pins measure voltage. In the case of shunt current sensors, currents are sensed as a voltage drop in the shunt resistor sensor. Referring to Figure 3, shunt sensors can be connected directly to the 71M654x (referred to as a 'local' shunt sensor) or connected via an isolated 71M6x01 (referred to as a 'remote' shunt sensor). In the case of Current Transformers (CT), the current is measured as a voltage across a burden resistor that is connected to the secondary winding of the CT. Meanwhile, line voltages are sensed through resistive voltage dividers. The VA and VB pins (VB is available in the 71M6542F/G only) are single-ended and their common return is the V3P3A pin.

Pins IAP-IAN can be programmed individually to be differential or single-ended as determined by the *DIFFA_E* (*I/O RAM 0x210C[4]*) control bit. However, for most applications, IAP-IAN are configured as a differential input to work with a shunt or CT directly interfaced to the IAP-IAN differential input with the appropriate external signal conditioning components (see 4.2 Direct Connection of Sensors on page 92).

The performance of the IAP-IAN pins can be enhanced by enabling a pre-amplifier with a fixed gain of 8, using the I/O RAM control bit *PRE_E (I/O RAM 0x2704[5])*. When *PRE_E* = 1, IAP-IAN become the inputs to the 8x pre-amplifier, and the output of this amplifier is supplied to the multiplexer. The 8x amplification is useful when current sensors with low sensitivity, such as shunt resistors, are used. With *PRE_E* set, the IAP-IAN input signal amplitude is restricted to 31.25 mV peak.

For the 71M654x application utilizing two shunt resistor sensors (Figure 3), the IAP-IAN pins are configured for differential mode to interface to a local shunt by setting the *DIFFA_E* control bit. Meanwhile, the IBP-IBN pins are re-configured as digital balanced pair to communicate with a Teridian 71M6x01 Isolated Sensor interface by setting the *RMT_E* control bit (*I/O RAM 0x2709[3]*). The 71M6x01 communicates with the 71M654x using a bi-directional digital data stream through an isolating low-cost pulse transformer. The 71M654x also supplies power to the 71M6x01 through the isolating transformer. This type of interface is further described at the end of this chapter (see 2.2.8 71M6x01 Isolated Sensor Interface (Remote Sensor Interface)).

For use with Current Transformers (CTs), as shown in Figure 2, the *RMT_E* control bit is reset, so that the IBP-IBN pins are configured as local analog inputs. The IAP-IAN pins cannot be configured as a remote sensor interface.

### 2.2.2 Input Multiplexer

When operating with local sensors, the input multiplexer sequentially applies the input signals from the analog input pins to the input of the ADC (see Figure 2 and Figure 4). One complete sampling sequence is called a multiplexer frame. The multiplexer of the 71M6541D/F/G can select up to three input signals (IAP-IAN, VA, and IBP-IBN) per multiplexer frame as controlled by the I/O RAM control field *MUX_DIV[3:0] (I/O RAM 0x2100[7:4])* (see Figure 6). The multiplexer of the 71M6542F/G adds the VB signal to achieve a total of four inputs (see Figure 7). The multiplexer always starts at state 1 and proceeds until as many states as determined by *MUX_DIV[3:0]* have been converted.

The 71M6541D/F/G and 71M6542F/G each require a unique CE code that is written for the specific application. Moreover, each CE code requires specific AFE and MUX settings in order to function properly. Table 1 provides the CE code and settings corresponding to the local sensor configurations shown in Figure 2 and Figure 4. Table 2 provides the CE code and settings corresponding to the local/remote sensor configuration utilizing the 71M6x01 as shown in Figure 3 and Figure 5.

**Table 1. Required CE Code and Settings for Local Sensors**

| I/O RAM Mnemonic | I/O RAM Location | 71M6541D/F/G (hex) | 71M6542F/G (hex) | |
|---|---|---|---|---|
| | | | Eq. 0 or 1 | Eq. 2 |
| *FIR_LEN[1:0]* | 210C[2:1] | 1 | 1 | 2 |
| *ADC_DIV* | 2200[5] | 1 | 1 | 0 |
| *PLL_FAST* | 2200[4] | 1 | 1 | 1 |
| *MUX_DIV[3:0]* | 2100[7:4] | 3 | 3 | 4 |
| *MUX0_SEL[3:0]* | 2105[3:0] | 0 | 0 | 0 |
| *MUX1_SEL[3:0]* | 2105[7:4] | A | A | A |
| *MUX2_SEL[3:0]* | 2104[3:0] | 2 | 2 | 2 |
| *MUX3_SEL[3:0]* | 2104[7:4] | 1 | 1 | 9 |
| *RMT_E* | 2709[3] | 0 | 0 | 0 |
| *DIFFA_E* | 210C[4] | 1 | 1 | 1 |
| *DIFFB_E* | 210C[5] | 1 | 1 | 1 |
| *EQU[2:0]* | 2106[7:5] | 0 or 1 | 0 or 1 | 2 |
| CE Code | -- | CE41A01 | CE41A01 | CE41A04 |
| Equations | -- | 0 or 1 | 0 or 1 | 2 |
| Current Sensor Types | -- | 1 Shunt and 1 CT or 2 CTs | 1 Shunt and 1 CT or 2 CTs | 1 Shunt and 1 CT or 2 CTs |
| Applicable Figure | -- | Figure 2 | Figure 4 | Figure 4 |

**Notes:**
Teridian updates the CE code periodically. Please contact your local Teridian representative to obtain the latest CE code and the associated settings. The configuration presented in this table is set by the MPU demonstration code during initialization.

**Table 2. Required CE Code and Settings for 71M6x01 isolated Sensor**

| I/O RAM Mnemonic | I/O RAM Location | 71M6541D/F/G (hex) | 71M6542F/G (hex) |
|---|---|---|---|
| *FIR_LEN[1:0]* | 210C[2:1] | 1 | 1 |
| *ADC_DIV* | 2200[5] | 1 | 1 |
| *PLL_FAST* | 2200[4] | 1 | 1 |
| *MUX_DIV[3:0]* | 2100[7:4] | 3 | 3 |
| *MUX0_SEL[3:0]* | 2105[3:0] | 0 | 0 |
| *MUX1_SEL[3:0]* | 2105[7:4] | A | A |
| *MUX2_SEL[3:0]*[1] | 2104[3:0] | 1 | 9 |
| *MUX3_SEL[3:0]*[1] | 2104[7:4] | 1 | 1 |
| *RMT_E* | 2709[3] | 1 | 1 |
| *DIFFA_E* | 210C[4] | 1 | 1 |
| *DIFFB_E* | 210C[5] | 0 | 0 |
| *EQU[2:0]* | 2106[7:5] | 0 or 1 | 0, 1 or 2 |
| CE Code | -- | CE41B016201[2]<br>CE41B016601[3] | |
| Equations | -- | 0, 1 | 0, 1 and 2 |
| Current Sensor Type | -- | 1 Local Shunt and 1 Remote Shunt | 1 Local Shunt and 1 Remote Shunt |
| Applicable Figure | -- | Figure 3 | Figure 5 |

**Notes:**
1. Although not used, set to 1 (the sample data is ignored by the CE)
2. 71M654x with 71M6201 remote sensor (200 Amps)
3. 71M654x with 71M6601 remote sensor (60 Amps)

Teridian updates the CE code periodically. Please contact your local Teridian representative to obtain the latest CE code and the associated settings. The configuration presented in this table is set by the MPU demonstration code during initialization.


Using settings for the I/O RAM Mnemonics listed in Table 1 and Table 2 that do not match those required by the corresponding CE code being used results in undesirable side effects and must not be selected by the MPU. Consult your local Teridian representative to obtain the correct CE code and AFE / MUX settings corresponding to the application.

For a basic single-phase application, the IAP-IAN current input is configured for differential mode, whereas the VA pin is single-ended and is typically connected to the phase voltage via a resistor divider. The IBP-IBN differential input may be optionally used to sense the Neutral current. This configuration implies that the multiplexer applies a total of three inputs to the ADC. For this configuration, the multiplexer sequence is as shown in Figure 6. In this configuration IAP-IAN, IBP-IBN and VA are sampled, the extra conversion time slot (i.e., slot 2) is the optional Neutral current, and the physical current sensor for the Neutral current measurement may be omitted if not required.

For a standard single-phase application with tamper sensor in the neutral path, two current inputs can be configured for differential mode, using the pin pairs IAP-IAN and IBP-IBN. This means that the multiplexer applies a total of three inputs to the ADC. In this application, the system design may use two locally connected current sensors via IAP-IAN and IBP-IBN, as shown in Figure 2, and configured as differential inputs. Alternately, the IAP-IAN pin pair is configured as a differential input and connected to a local current shunt, and IBP-IBN is configured to connect to an isolated 71M6x01 isolated sensor (i.e., $RMT\_E = 1$), as shown in Figure 3. The VA pin is typically connected to the phase voltage via resistor dividers. For this configuration, the multiplexer frame is also as shown in Figure 6 and time slot 2 is unused and ignored by the CE, as the samples corresponding to the remote sensor (IBP-IBN) do not pass through the multiplexer and are stored directly in CE RAM. The remote current sensor channel is sampled during the second half of the multiplexer frame and its timing relationship to the VA voltage is precisely known so that delay compensation can be properly applied.

The 71M6542F adds the ability to sample a second phase voltage (applied at the VB pin), which makes it suitable for meters with two voltage and two current sensors, such as meters implementing Equation 2 for dual-phase operation (P = VA*IA+VB*IB). Figure 7 shows the multiplexer sequence when four inputs are

processed with locally connected sensors, as shown in Figure 3. When using one local and one remote sensor (Figure 5), the multiplexer sequence is also as shown in Figure 7.

For both multiplexer sequences shown in Figure 6 and Figure 7, the frame duration is 13 CK32 cycles (where CK32 = 32768 Hz), therefore, the resulting sample rate is 32768 Hz / 13 = 2520.6 Hz.

Table 3 summarizes the various AFE input configurations.

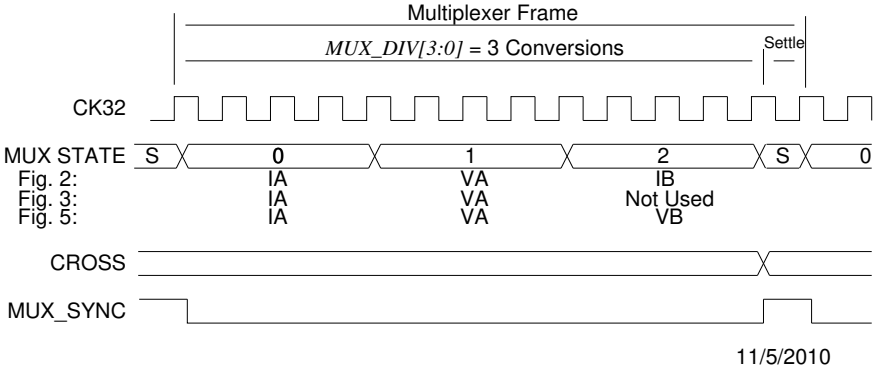


**Figure 6: States in a Multiplexer Frame (*MUX_DIV[3:0]* = 3)**

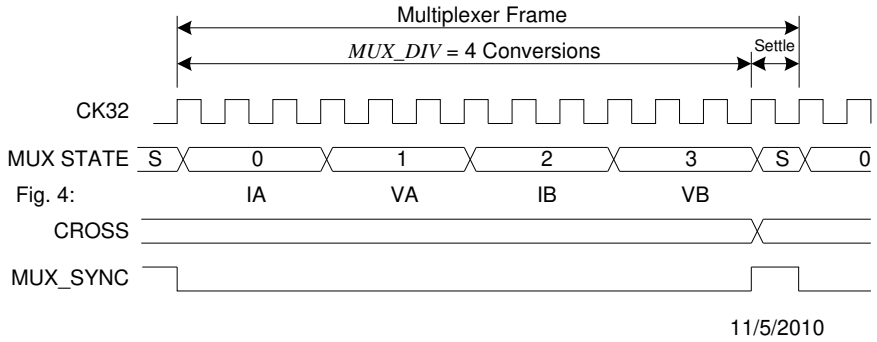


**Figure 7: States in a Multiplexer Frame (*MUX_DIV[3:0]* = 4)**

**Table 3: ADC Input Configuration**

| Pin | ADC Channel | Required Setting | Comment |
|---|---|---|---|
| IAP | ADC0 | *DIFFA_E* = 1 | Differential mode must be selected with *DIFFA_E* = 1 (*I/O RAM 0x210C[4]*). The ADC results are stored in CE RAM location *ADC0* (*CE RAM 0x0*), and *ADC1* (*CE RAM 0x1*) is not disturbed. |
| IAN | ADC1 | | |
| IBP | ADC2 | *DIFFB_E* = 1 or *RMT_E* = 1 | For locally connected sensors (Figure 2 and Figure 4), the differential input must be enabled by setting *DIFFB_E (I/O RAM 0x210C[5]*.<br>For the remote connected sensor (Figure 3 and Figure 5) with a remote shunt sensor, *RMT_E* (*I/O RAM 0x2709[3]*) must be set.<br>In both cases, the ADC results are stored in RAM location *ADC2 (CE RAM 0x2)*, and *ADC3 (CE RAM 0x3)* is not disturbed. |
| IBN | ADC3 | | |
| VA | ADC10 | -- | Single-ended mode only. The ADC result is stored in RAM location *ADC10* (*CE RAM 0xA*). |
| VB | ADC9 | -- | Single-ended mode only (71M6542F only). The ADC result is stored in RAM location *ADC9* (*CE RAM 0x9*). |

Multiplexer advance, FIR initiation and chopping of the ADC reference voltage (using the internal CROSS signal, see 2.2.7 Voltage References) are controlled by the internal MUX_CTRL circuit. Additionally, MUX_CTRL launches each pass of the CE through its code. Conceptually, MUX_CTRL is clocked by CK32, the 32768 Hz clock from the PLL block. The behavior of the MUX_CTRL circuit is governed by:

- *CHOP_E[1:0]* (*I/O RAM 0x2106[3:2]*)
- *MUX_DIV[3:0]* (*I/O RAM 0x2100[7:4]*)
- *FIR_LEN[1:0]* (*I/O RAM 0x210C[2:1]*)
- *ADC_DIV* (*I/O RAM 0x2200[5]*)

The duration of each multiplexer state depends on the number of ADC samples processed by the FIR as determined by the *FIR_LEN[1:0] (I/O RAM 0x210C[2:1]* control field. Each multiplexer state starts on the rising edge of CK32, the 32-kHz clock.

It is recommended that *MUX_DIV[3:0] (I/O RAM 0x2200[2:0])* be set to zero while changing the ADC configuration. Although not required, it minimizes system transients that might be caused by momentary shorts between the ADC inputs, especially when changing the *DIFFn_E* control bits (*I/O RAM 0x210C[5:4]*). After the configuration bits are set, *MUX_DIV[3:0]* should be set to the required value.

Additionally, the ADC can be configured to operate at ½ rate (32768*75=2.46MHz). In this mode, the bias current to the ADC amplifiers is reduced and overall system power is reduced. The *ADC_DIV (I/O RAM 0x2200[5])* bit selects full speed or half speed. At half speed, if *FIR_LEN[1:0]* is set to 01 (288), each conversion requires 4 XTAL cycles, resulting in a 2520Hz sample rate when *MUX_DIV[3:0]* = 3. Note that in order to work with these power-reducing settings, a corresponding CE code is required.

The duration of each time slot in CK32 cycles depends on *FIR_LEN[1:0], ADC_DIV* and *PLL_FAST*:

Time_Slot_Duration (*PLL_FAST* = 1) = (*FIR_LEN[1:0]*+1) * (*ADC_DIV*+1)

Time_Slot_Duration (*PLL_FAST* = 0) = 3*(*FIR_LEN[1:0]*+1) * (*ADC_DIV*+1)

The duration of a multiplexer frame in CK32 cycles is:

MUX_Frame_Duration = 3-2**PLL_FAST* + Time_Slot_Duration * *MUX_DIV[3:0]*

The duration of a multiplexer frame in CK_FIR cycles is:

MUX frame duration (CK_FIR cycles) =

[3-2**PLL_FAST* + Time_Slot_Duration * *MUX_DIV*] * (48+*PLL_FAST**102)

The ADC conversion sequence is programmable through the *MUXx_SEL* control fields (*I/O RAM 0x2100* to *0x2105*). As stated above, there are three ADC time slots in the 71M6541D/F/G and four ADC time slots in the 71M6542F/G, as set by *MUX_DIV[3:0]* (*I/O RAM 0x2100[7:4]*). In the expression *MUXx_SEL[3:0]* = n, '*x*' refers to the multiplexer frame time slot number and n refers to the desired ADC input number or ADC handle (i.e., ADC0 to ADC10, or simply 0 to 10 decimal). Thus, there are a total of 11 valid ADC handles in the 71M654x devices. For example, if *MUX0_SEL[3:0]* = 0, then ADC0, corresponding to the sample from the IAP-IAN input (configured as a differential input), is positioned in the multiplexer frame during time slot 0. See Table 1 and Table 2 for the appropriate *MUXx_SEL[3:0]* settings and other settings applicable to a particular CE code.

Note that when the remote sensor interface is enabled, and even though the samples corresponding to the remote sensor current (IBP-IBN) do not pass through the multiplexer, the *MUX2_SEL[3:0]* and *MUX3_SEL[3:0]* control fields must be written with a valid ADC handle that is not being used. Typically, ADC1 is used for this purpose (see Table 2). In this manner, the ADC1 handle, which is not used in the 71M6541D/F/G or 71M6542F/G, is used as a place holder in the multiplexer frame, in order to generate the correct multiplexer frame sequence and the correct sample rate. The resulting sample data stored in *CE RAM 0x1* is undefined and is ignored by the CE code. Meanwhile, the digital isolation interface takes care of automatically storing the samples for the remote interface current (IBP-IBN) in *CE RAM 0x2*.

✓ Delay compensation and other functions in the CE code require the settings for *MUX_DIV[3:0], MUXx_SEL[3:0], RMT_E, FIR_LEN[1:0], ADC_DIV* and *PLL_FAST* to be fixed for a given CE code. Refer to Table 1 and Table 2 for the settings that are applicable to the 71M6541D/F/G and 71M6542F/G.

Table 4 summarizes the I/O RAM registers used for configuring the multiplexer, signals pins, and ADC. All listed registers are 0 after reset and wake from battery modes, and are readable and writable.

**Table 4: Multiplexer and ADC Configuration Bits**

| Name | Location | Description |
|---|---|---|
| *MUX0_SEL[3:0]* | 2105[3:0] | Selects the ADC input converted during time slot 0. |
| *MUX1_SEL[3:0]* | 2105[7:4] | Selects the ADC input converted during time slot 1. |
| *MUX2_SEL[3:0]* | 2104[3:0] | Selects the ADC input converted during time slot 2. |
| *MUX3_SEL[3:0]* | 2104[7:4] | Selects the ADC input converted during time slot 3. |
| *MUX4_SEL[3:0]* | 2103[3:0] | Selects the ADC input converted during time slot 4. |
| *MUX5_SEL[3:0]* | 2103[7:4] | Selects the ADC input converted during time slot 5. |
| *MUX6_SEL[3:0]* | 2102[3:0] | Selects the ADC input converted during time slot 6. |
| *MUX7_SEL[3:0]* | 2102[7:0] | Selects the ADC input converted during time slot 7. |
| *MUX8_SEL[3:0]* | 2101[3:0] | Selects the ADC input converted during time slot 8. |
| *MUX9_SEL[3:0]* | 2101[7:0] | Selects the ADC input converted during time slot 9. |
| *MUX10_SEL[3:0]* | 2100[3:0] | Selects the ADC input converted during time slot 10. |
| *ADC_DIV* | 2200[5] | Controls the rate of the ADC and FIR clocks. |
| *MUX_DIV[3:0]* | 2100[7:4] | The number of ADC time slots in each multiplexer frame (maximum = 11). |
| *PLL_FAST* | 2200[4] | Controls the speed of the PLL and MCK. |
| *FIR_LEN[1:0]* | 210C[1] | Determines the number of ADC cycles in the ADC decimation FIR filter. |
| *DIFFA_E* | 210C[4] | Enables the differential configuration for analog input pins IAP-IAN. |
| *DIFFB_E* | 210C[5] | Enables the differential configuration for analog input pins IBP-IBN. |
| *RMT_E* | 2709[3] | Enables the remote sensor interface transforming pins IBP-IBN into a digital balanced differential pair for communications with the 71M6x01 sensor. |
| *PRE_E* | 2704[5] | Enables the 8x pre-amplifier. |
| Refer to Table 76 starting on page 111 for more complete details about these I/O RAM locations. | | |

### 2.2.3 Delay Compensation

When measuring the energy of a phase (i.e., Wh and VARh) in a service, the voltage and current for that phase must be sampled at the same instant. Otherwise, the phase difference, Φ, introduces errors.

$$\phi = \frac{t_{delay}}{T} \cdot 360^o = t_{delay} \cdot f \cdot 360^o$$

Where *f* is the frequency of the input signal, T = 1/f and $t_{delay}$ is the sampling delay between current and voltage.

Traditionally, sampling is accomplished by using two A/D converters per phase (one for voltage and the other one for current) controlled to sample simultaneously. Maxim's Teridian Single-Converter Technology, however, exploits the 32-bit signal processing capability of its CE to implement "constant delay" all-pass filters. The all-pass filter corrects for the conversion time difference between the voltage and the corresponding current samples that are obtained with a single multiplexed A/D converter.

The "constant delay" all-pass filter provides a broad-band delay $360^o - \theta$, which is precisely matched to the difference in sample time between the voltage and the current of a given phase. This digital filter does not affect the amplitude of the signal, but provides a precisely controlled phase response.

The recommended ADC multiplexer sequence samples the current first, immediately followed by sampling of the corresponding phase voltage, thus the voltage is delayed by a phase angle Φ relative to

the current. The delay compensation implemented in the CE aligns the voltage samples with their corresponding current samples by first delaying the current samples by one full sample interval (i.e., 360°), then routing the voltage samples through the all-pass filter, thus delaying the voltage samples by 360° - θ, resulting in the residual phase error between the current and its corresponding voltage of θ – Φ. The residual phase error is negligible, and is typically less than ±1.5 milli-degrees at 100Hz, thus it does not contribute to errors in the energy measurements.

When using remote sensors, the CE performs the same delay compensation described above to align each voltage sample with its corresponding current sample. Even though the remote current samples do not pass through the 71M654x multiplexer, their timing relationship to their corresponding voltages is fixed and precisely known, provided that the *MUXn_SEL[3:0]* slot assignment fields are programmed as shown in Table 1 and Table 2.

### 2.2.4 ADC Pre-Amplifier

The ADC pre-amplifier is a low-noise differential amplifier with a fixed gain of 8 available only on the IAP-IAN sensor input pins. A gain of 8 is enabled by setting *PRE_E* = 1 (*I/O RAM 0x2704[5]*). When disabled, the supply current of the pre-amplifier is <10 nA and the gain is unity. With proper settings of the *PRE_E* and *DIFFA_E* (*I/O RAM 0x210C[4]*) bits, the pre-amplifier can be used whether differential mode is selected or not. For best performance, the differential mode is recommended. In order to save power, the bias current of the pre-amplifier and ADC is adjusted according to the *ADC_DIV* control bit (*I/O RAM 0x2200[5]*).

### 2.2.5 A/D Converter (ADC)

A single 2nd order delta-sigma A/D converter digitizes the voltage and current inputs to the device. The resolution of the ADC, including the sign bit, is 21 bits (*FIR_LEN[1:0]* = 1, *I/O RAM 0x210C[2:1]*), or 22 bits (*FIR_LEN[1:0]* = 2). The ADC is clocked by CKADC.

Initiation of each ADC conversion is controlled by MUX_CTRL internal circuit as described above. At the end of each ADC conversion, the FIR filter output data is stored into the CE RAM location determined by the multiplexer selection. FIR data is stored LSB justified, but shifted left 9 bits.

### 2.2.6 FIR Filter

The finite impulse response filter is an integral part of the ADC and it is optimized for use with the multiplexer. The purpose of the FIR filter is to decimate the ADC output to the desired resolution. At the end of each ADC conversion, the output data is stored into the fixed CE RAM location determined by the multiplexer selection as shown in Table 1 and Table 2.

### 2.2.7 Voltage References

A bandgap circuit provides the reference voltage to the ADC. The amplifier within the reference is chopper stabilized, i.e., the chopper circuit can be enabled or disabled by the MPU using the I/O RAM control field *CHOP_E[1:0] (I/O RAM 0x2106[3:2])*. The two bits in the *CHOP_E[1:0]* field enable the MPU to operate the chopper circuit in regular or inverted operation, or in toggling modes (recommended). When the chopper circuit is toggled in between multiplexer cycles, dc offsets on VREF are automatically be averaged out, therefore the chopper circuit should always be configured for one of the toggling modes.

Since the VREF band-gap amplifier is chopper-stabilized, the dc offset voltage, which is the most significant long-term drift mechanism in the voltage references (VREF), is automatically removed by the chopper circuit. Both the 71M654x and the 71M6x01 feature chopper circuits for their respective VREF voltage reference.

The general topology of a chopped amplifier is shown in Figure 8. The CROSS signal is an internal on-chip signal and is not accessible on any pin or register.

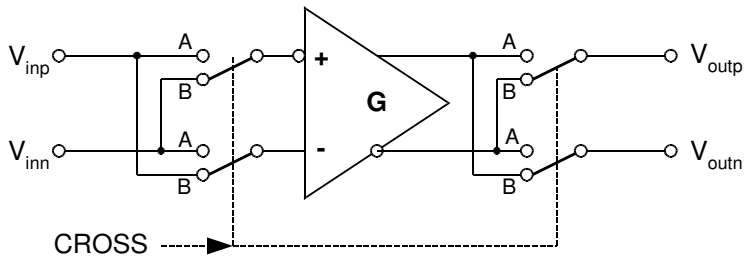


**Figure 8: General Topology of a Chopped Amplifier**

It is assumed that an offset voltage Voff appears at the positive amplifier input. With all switches, as controlled by CROSS (an internal signal), in the A position, the output voltage is:

Voutp – Voutn = G (Vinp + Voff – Vinn) = G (Vinp – Vinn) + G Voff

With all switches set to the B position by applying the inverted CROSS signal, the output voltage is:

Voutn – Voutp = G (Vinn – Vinp + Voff) = G (Vinn – Vinp) + G Voff, or

Voutp – Voutn = G (Vinp – Vinn) - G Voff

Thus, when CROSS is toggled, e.g., after each multiplexer cycle, the offset alternately appears on the output as positive and negative, which results in the offset effectively being eliminated, regardless of its polarity or magnitude.

When CROSS is high, the connection of the amplifier input devices is reversed. This preserves the overall polarity of that amplifier gain; it inverts its input offset. By alternately reversing the connection, the amplifier's offset is averaged to zero. This removes the most significant long-term drift mechanism in the voltage reference. The *CHOP_E[1:0]* (*I/O RAM 0x2106[3:2]*) control field controls the behavior of CROSS. The CROSS signal reverses the amplifier connection in the voltage reference in order to negate the effects of its offset. On the first CK32 rising edge after the last multiplexer state of its sequence, the multiplexer waits one additional CK32 cycle before beginning a new frame. At the beginning of this cycle, the value of CROSS is updated according to the *CHOP_E[1:0]* field. The extra CK32 cycle allows time for the chopped VREF to settle. During this cycle, MUXSYNC is held high. The leading edge of MUXSYNC initiates a pass through the CE program sequence. The beginning of the sequence is the serial readout of the four RTM words.

*CHOP_E[1:0]* has four states: positive, reverse, and two toggle states. In the positive state, *CHOP_E[1:0]* = 01, CROSS is held low. In the reverse state, *CHOP_E[1:0]* = 10, CROSS is held high.

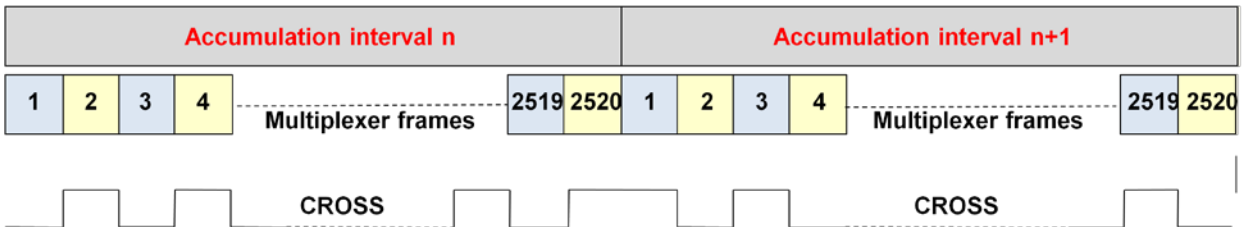


**Figure 9: CROSS Signal with *CHOP_E* = 00**

Figure 9 shows CROSS over two accumulation intervals when *CHOP_E[1:0]* = 00: At the end of the first interval, CROSS is high, at the end of the second interval, CROSS is low. Operation with *CHOP_E[1:0]* = 00 does not require control of the chopping mechanism by the MPU.

In the second toggle state, *CHOP_E[1:0]* = 11, CROSS does not toggle at the end of the last multiplexer cycle in an accumulation interval.

A second, low-power voltage reference is used in the LCD system and for the comparators that support transitions to and from the battery modes.

### 2.2.8 71M6x01 Isolated Sensor Interface (Remote Sensor Interface)

#### 2.2.8.1 General Description

Non-isolating sensors, such as shunt resistors, can be connected to the inputs of the 71M654x via a combination of a pulse transformer and a 71M6x01 IC (a top-level block diagram of this sensor interface is shown in Figure 36). The 71M6x01 receives power directly from the 71M654x via a pulse transformer and does not require a dedicated power supply circuit. The 71M6x01 establishes 2-way communication with the 71M654x, supplying current samples and auxiliary information such as sensor temperature via a serial data stream.

One 71M6x01 Isolated Sensor can be supported by the 71M6541D/F/G and 71M6542F/G. When remote interface IBP-IBN is enabled, the two analog current inputs pins IBP and IBN become a digital balanced differential interface to the remote sensor. See Table 3 for details.

Each 71M6x01 Isolated Sensor consists of the following building blocks:

- Power supply for power pulses received from the 71M654x
- Digital communications interface
- Shunt signal pre-amplifier
- Delta-Sigma ADC Converter with precision bandgap reference (chopping amplifier)
- Temperature sensor
- Fuse system containing part-specific information

During an ordinary multiplexer cycle, the 71M654x internally determines which other channels are enabled with *MUX_DIV[3:0] (I/O RAM 0x2100[7:4])*. At the same time, it decimates the modulator output from the 71M6x01 Isolated Sensors. Each result is written to CE RAM during one of its CE access time slots. See Table 3 for the CE RAM locations of the sampled signals.

#### 2.2.8.2 Communication between 71M654x and 71M6x01 Isolated Sensor

The ADC of the 71M6x01 derives its timing from the power pulses generated by the 71M654x and as a result, operates its ADC slaved to the frequency of the power pulses. The generation of power pulses, as well as the communication protocol between the 71M654x and 71M6x01 Isolated Sensor is automatic and transparent to the user. Details are not covered in this data sheet.

#### 2.2.8.3 Control of the 71M6x01 Isolated Sensor

The 71M654x can read or write certain types of information from each 71M6x01 isolated sensor.

The data to be read is selected by a combination of the *RCMD[4:0]* and *TMUXRn[2:0]*. To perform a read transaction from one of the 71M6x01 devices, the MPU first writes the *TMUXRn[2:0]* field (where n = 2, 4, 6, located at *I/O RAM 0x270A[2:0], 0x270A[6:4]* and *0x2709[2:0],* respectively). Next, the MPU writes *RCMD[4:0]* (*SFR 0xFC[4:0]*) with the desired command and phase selection. When the *RCMD[4:2]* bits have cleared to zero, the transaction has been completed and the requested data is available in *RMT_RD[15:0]* (*I/O RAM 0x2602[7:0]* is the MSB and *0x2603[7:0]* is the LSB). The read parity error bit, *PERR_RD (SFR 0xFC[6])* is also updated during the transaction. If the MPU writes to *RCMD[4:0]* before a previously initiated read transaction is completed, the command is ignored. Therefore, the MPU must wait for *RCMD[4:2]*=0 before proceeding to issue the next remote sensor read command.

The *RCMD[4:0]* field is divided into two sub-fields, *COMMAND=RCMD[4:2]* and *PHASE=RCMD[1:0]*, as shown in Table 5.

**Table 5. *RCMD[4:0]* Bits**

| **Command** *RCMD[4:2]* | | **Phase Selector** *RCMD[1:0]* | | **Associated** *TMUXRn* **Control Field** |
|---|---|---|---|---|
| 000 | Invalid | 00 | Invalid | --- |
| 001 | Command 1 | 01 | IBP-IBN | *TMUXRB [2:0]* |
| 100 | Reserved | | | |
| 101 | Invalid | | | |
| 110 | Reserved | | | |

| | | |
|---|---|---|
| 111 | Reserved | |

**Notes:**
1. Only two codes of *RCMD[4:2]* (*SFR 0xFC[4:2]*) are relevant for normal operation. These are *RCMD[4:2]* = 001 and 010. Codes 000 and 101 are invalid and will be ignored if used. The remaining codes are reserved and must not be used.
2. For the *RCMD[1:0]* control field, codes 01, 10 and 11 are valid and 00 is invalid and must not be used.

Table 6 shows the allowable combinations of values in *RCMD[4:2]* and *TMUXRn[2:0]*, and the corresponding data type and format sent back by the 71M6x01 isolated sensor and how the data is stored in *RMT_RD[15:8]* and *RMT_RD[7:0]*. The MPU selects which of the three phases is read by asserting the proper code in the *RCMD[1:0]* field, as shown in Table 5.

**Table 6: Remote Interface Read Commands**

| *RCMD[4:2]* | *TMUXRn[2:0]* | Read Operation | *RMT_RD* [15:8] | *RMT_RD* [7:0] |
|---|---|---|---|---|
| 001 | 00X | *TRIMT[7:0]*<br>(trim fuse for all 71M6x01) | *TRIMT[7]=RMT_RD[8]* | *TRIMT[6:0]=RMT_RD[7:1]* |
| 010 | 00X | *STEMP[10:0]*<br>(sensed 71M6x01 temperature) | *STEMP[10:8]=RMT_RD[10:8]*<br>*(RMT_RD[15:11] are sign extended)* | *STEMP[7:0]* |
| 010 | 01X | *VSENSE[7:0]*<br>(sensed 71M6x01 supply voltage) | *All zeros* | *VSENSE[7:0]* |
| 010 | 10X | *VERSION[7:0]*<br>(chip version) | *VERSION[7:0]* | *All zeros* |

**Notes:**
1. *TRIMT[7:0]* is the VREF trim value for all 71M6x01 devices. Note that the *TRIMT[7:0]* 8-bit value is formed by *RMT_RD[8]* and *RMT_RD[7:1]*. See the 71M6xxx Data sheet for more information on *TRIMT[7:0]*
2. See the *71M6xxx Data Sheet* for the equation to calculate temperature from the *STEMP[7:0]* value read from the 71M6x01.
3. See the *71M6xxx Data Sheet* for the equation to calculate temperature from the *VSENSE[7:0]* value read from the 71M6x01.

With hardware and trim-related information on each connected 71M6x01 Isolated Sensor available to the 71M6541D/F/G, the MPU can implement temperature compensation of the energy measurement based on the individual temperature characteristics of the 71M6x01 Isolated Sensor. See 4.7 Metrology Temperature Compensation on page 97 for details.

Table 7 shows all I/O RAM registers used for control of the external 71M6x01 Isolated Sensors. See the 71M6xxx Data Sheet for additional details.

**Table 7: I/O RAM Control Bits for Isolated Sensor**

| Name | Address | RST Default | WAKE Default | R/W | Description |
|---|---|---|---|---|---|
| *RCMD[4:0]* | SFR FC[4:0] | 0 | 0 | R/W | When the MPU writes a non-zero value to *RCMD*, the 71M654x issues a command to the corresponding isolated sensor selected with *RCMD[1:0]*. When the command is complete, the 71M654x clears *RCMD[4:2]*. The command code itself is in *RCMD[4:2]*. |
| *PERR_RD*<br>*PERR_WR* | SFR FC[6]<br>SFR FC[5] | 0 | 0 | R/W | The 71M654x sets these bits to indicate that a parity error on the isolated sensor has been detected. Once set, the bits are remembered until they are cleared by the MPU. |
| *CHOPR[1:0]* | 2709[7:6] | 00 | 00 | R/W | The CHOP settings for the isolated sensors.<br>00 – Auto chop. Change every multiplexer frame.<br>01 – Positive<br>10 – Negative<br>11 – Same as 00 |

| Name | Address | RST Default | WAKE Default | R/W | Description |
|---|---|---|---|---|---|
| *TMUXRB[2:0]* | 270A[2:0] | 000 | 000 | R/W | The TMUX bits for control of the isolated sensor. |
| *RMT_RD[15:8]*<br>*RMT_RD[7:0]* | 2602[7:0]<br>2603[7:0] | 0 | 0 | R | The read buffer for 71M6x01 read operations. |
| *RFLY_DIS* | 210C[3] | 0 | 0 | R/W | Controls how the 71M654x drives the 71M6x01 power pulse. When set, the power pulse is driven high and low. When cleared, it is driven high followed by an open circuit flyback interval. |
| *RMTB_E* | 2709[3] | 0 | 0 | R/W | Enables the isolated remote sensor interface and re-configures pins IBP-IBN as a balanced pair digital remote interface. |
| Refer to Table 76 starting on page 111 for more complete details about these I/O RAM locations. | | | | | |

## 2.3 Digital Computation Engine (CE)

The CE, a dedicated 32-bit signal processor, performs the precision computations necessary to accurately measure energy. The CE calculations and processes include:

- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied with the constant sample time).
- Frequency-insensitive delay cancellation on all four channels (to compensate for the delay between samples caused by the multiplexing scheme).
- 90° phase shifter (for VAR calculations).
- Pulse generation.
- Monitoring of the input signal frequency (for frequency and phase information).
- Monitoring of the input signal amplitude (for sag detection).
- Scaling of the processed samples based on calibration coefficients.
- Scaling of samples based on temperature compensation information.

### 2.3.1 CE Program Memory

The CE program resides in flash memory. Common access to flash memory by the CE and MPU is controlled by a memory share circuit. Each CE instruction word is two bytes long. Allocated flash space for the CE program cannot exceed 4096 16-bit words (8 KB). The CE program counter begins a pass through the CE code each time multiplexer state 0 begins. The code pass ends when a HALT instruction is executed. For proper operation, the code pass must be completed before the multiplexer cycle ends.

The CE program must begin on a 1 KB boundary of the flash address. The I/O RAM control field *CE_LCTN[5:0]* (*I/O RAM 0x2109[5:0]*) defines which 1 KB boundary contains the CE code. Thus, the first CE instruction is located at 1024**CE_LCTN[5:0]*.

### 2.3.2 CE Data Memory

The CE and MPU share data memory (RAM). Common access to XRAM by the CE and MPU is controlled by a memory share circuit. The CE can access up to 3 KB of the 3 KB data RAM (XRAM), i.e., from RAM address 0x0000 to 0x0C00.

The XRAM can be accessed by the FIR filter block, the RTM circuit, the CE, and the MPU. Assigned time slots are reserved for FIR and MPU, respectively, to prevent bus contention for XRAM data access by the CE.

The MPU reads and writes the XRAM shared between the CE and MPU as the primary means of data communication between the two processors.

Table 3 shows the CE addresses in XRAM allocated to analog inputs from the AFE.

The CE is aided by support hardware to facilitate implementation of equations, pulse counters, and accumulators. This hardware is controlled through the I/O RAM control field *EQU[2:0],* equation assist *(I/O RAM 0x2106[7:5]*), bit *DIO_PV (I/O RAM 0x2457[6]),* bit *DIO_PW*, pulse count assist (*I/O RAM 0x2457[7]*), and SUM*_SAMPS[12:0]*, accumulation assist (*I/O RAM 0x2107[4:0] and 0x2108[7:0]*).

*SUM_SAMPS[12:0]* supports an accumulation scheme where the incremental energy values from up to *SUM_SAMPS[12:0]* multiplexer frames are added up over one accumulation interval. The integration time for each energy output is, for example, *SUM_SAMPS[12:0]*/2520.6 (with *MUX_DIV[3:0]* = 011, *I/O RAM 0x2100[7:4]* and *FIR_LEN[1:0]* = 10, *I/O RAM 0x210C[2:1]*). CE hardware issues the XFER_BUSY interrupt when the accumulation is complete.

### 2.3.3 CE Communication with the MPU

The CE outputs six signals to the MPU: CE_BUSY, XFER_BUSY, XPULSE, YPULSE, WPULSE and VPULSE. These are connected to the MPU interrupt service. CE_BUSY indicates that the CE is actively processing data. This signal occurs once every multiplexer frame. XFER_BUSY indicates that the CE is updating to the output region of the CE RAM, which occurs whenever an accumulation cycle has been completed. Both, CE_BUSY and XFER_BUSY are cleared when the CE executes a HALT instruction.

XPULSE, YPULSE, VPULSE and WPULSE can be configured to interrupt the MPU and indicate sag failures, zero crossings of the mains voltage, or other significant events. Additionally, these signals can be connected directly to DIO pins to provide direct outputs for the CE. Interrupts associated with these signals always occur on the leading edge (see "External" interrupt source No. 2 in Figure 16).

### 2.3.4 Meter Equations

The 71M6541D/F/G and 71M6542F/G provide hardware assistance to the CE in order to support various meter equations. This assistance is controlled through I/O RAM register *EQU[2:0]* (equation assist). The Compute Engine (CE) firmware for industrial configurations can implement the equations listed in Table 8. *EQU*[2:0] specifies the equation to be used based on the meter configuration and on the number of phases used for metering.

**Table 8: Inputs Selected in Multiplexer Cycles**

| *EQU* | Description | Wh and VARh formula | | | Recommended Multiplexer Sequence |
|---|---|---|---|---|---|
| | | Element 0 | Element 1 | Element 2 | |
| 0 | 1-element, 2-W, 1ϕ with neutral current sense | VA · IA | VA · IB[1] | N/A | IA VA IB[1] |
| 1 | 1-element, 3-W, 1ϕ | VA(IA-IB)/2 | N/A | N/A | IA VA IB |
| 2 † | 2-element, 3-W, 3ϕ Delta | VA · IA | VB · IB | N/A | IA VA IB VB |

Note:
1. Optionally, IB may be used to measure neutral current

† 71M6542F/G only

### 2.3.5 Real-Time Monitor (RTM)

The CE contains a Real-Time Monitor (RTM), which can be programmed to monitor four selectable XRAM locations at full sample rate. The four monitored locations, as selected by the I/O RAM registers *RTM0[9:8], RTM0[7:0], RTM1[9:8], RTM1[7:0], RTM2[9:8], RTM2[7:0], RTM3[9:8],* and *RTM3[7:0]*, are serially output to the TMUXOUT pin via the digital output multiplexer at the beginning of each CE code pass. The RTM can be enabled and disabled with control bit *RTM_E (I/O RAM 0x2106[1])*. The RTM output is clocked by CKTEST. Each RTM word is clocked out in 35 CKCE cycles (1 CKCE cycle is equivalent to 203 ns) and contains a leading flag bit. See Figure 10 for the RTM output format. RTM is low when not in use.

Figure 11 summarizes the timing relationships between the input MUX states, the CE_BUSY signal, and the RTM serial output stream. In this example, *MUX_DIV[3:0]* = 4 *(I/O RAM 0x2100[7:4])* and *FIR_LEN[1:0]* = 10 *(I/O RAM 0x210C[1]),* (384), resulting in 4 ADC conversions. An ADC conversion always consumes an integer number of CK32 clocks. Followed by the conversions is a single CK32 cycle.

Figure 11 also shows that the RTM serial data stream begins transmitting at the beginning of state S. RTM, consisting of 140 CK cycles, always finishes before the next CE code pass starts.