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71M6543FT/71M6543HT/ 71M6543GT/71M6543GHT

Energy Meter ICs

General Description

The 71M6543FT/71M6543HT/71M6543GT/71M6543GHT (71M654xT) are 4th-generation three-phase metering systems-on-chips (SoCs) with a 5MHz, 8051-compatible MPU core, low-power RTC with digital temperature compensation, flash memory, and LCD driver. Our Single Converter Technology® with a 22-bit delta-sigma ADC, seven analog inputs, digital temperature compensation, precision voltage reference, and a 32-bit computation engine (CE) support a wide range of metering applications with very few external components.

The 71M654xT devices support optional interfaces to the Maxim Integrated 71M6x03 series of isolated sensors offering BOM cost reduction, immunity to magnetic tamper, and enhanced reliability. Other features include an SPI interface, advanced power management, ultra-low-power operation in active and battery modes, 5KB shared RAM, and 64KB/128KB flash memory that can be programmed in the field with code and/or data during meter operation and the ability to drive up to six LCD segments per SEG driver pin. High processing and sampling rates combined with differential inputs offer a powerful platform for residential meters.

A complete array of code development tools, demonstration code, and reference designs enable rapid development and certification of meters that meet all ANSI and IEC electricity metering standards worldwide.

The 71M654xT family operates over the industrial temperature range and comes in a 100-pin lead(Pb)-free LQFP package.

Applications

- Three-Phase Residential, Commercial, and Industrial Energy Meters

***Ordering Information* and *Typical Operating Circuit* appear at end of data sheet.**

Single Converter Technology is a registered trademark of Maxim Integrated Products, Inc.

MICROWIRE is a registered trademark of National Semiconductor Corp.

Benefits and Features

- SoC Integration and Unique Isolation Technique Reduces BOM Cost Without Sacrificing Performance
  - 0.1% Typical Accuracy Over 2000:1 Current Range
  - Exceeds IEC 62053/ANSI C12.20 Standards
  - Four-Quadrant Metering
  - 46-64Hz Line Frequency Range with the Same Calibration
  - Phase Compensation (±10°)
  - Independent 32-Bit Compute Engine
  - 64KB Flash, 5KB RAM (71M6543FT/71M6543HT)
  - 128KB Flash, 5KB RAM (71M6543GT/71M6543GHT)
  - Built-In Flash Security
  - SPI Interface with Flash Program Capability
  - Up to Four Pulse Outputs with Pulse Count
  - 8-Bit MPU (80515), Up to 5 MIPS
  - Full-Speed MPU Clock in Brownout Mode
  - LCD Driver Allows Up to 6 Commons/Up to 56 Pins
  - Up to 51 Multifunction DIO Pins
  - Hardware Watchdog Timer (WDT)
  - Two UARTs for IR and AMR
  - IR LED Driver with Modulation
  - I2C/MICROWIRE® EEPROM Interface
- Innovative Isolation Technology (Requires Companion 71M6xxx Sensor, also from Maxim Integrated) Eliminates Current Transformers
  - Four Current Sensor Inputs with Selectable Differential Mode
  - Selectable Gain of 1 or 8 for One Current Input to Support Neutral Current Shunt
  - High-Speed Wh/VARh Pulse Outputs with Programmable Width
- Digital Temperature Compensation Improves System Performance
  - Metrology Compensation
  - Accurate RTC for TOU Functions with Automatic Temperature Compensation for Crystal in All Power Modes
- Power Management Extends Battery Life During Power Outages
  - Three Battery-Backup Modes
    - Brownout Mode (BRN)
    - LCD Mode (LCD)
    - Sleep Mode (SLP)
- Wake-Up on Pin Events and Wake-On Timer
  - 1μA in Sleep Mode

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Absolute Maximum Ratings

(All voltages referenced to GNDA.)

Supplies and Ground Pins

$V_{V3P3SYS}$, V_{V3P3A} ....-0.5V to +4.6V
V_{BAT}, V_{BAT_RTC} ....-0.5V to +4.6V
GNDD ....-0.1V to +0.1V

Analog Output Pins

V_{REF} ....-10mA to +10mA, -0.5V to (V_{V3P3A} + 0.5V)
V_{DD} ....-10mA to +10mA, -0.5V to +3.0V
V_{V3P3D} ....-10mA to +10mA, -0.5V to +4.6V
V_{LCD} ....-10mA to +10mA, -0.5V to +6.0V

Analog Input Pins

IADC0-7, VADC8-10..........................-10mA to +10mA, -0.5V to (V_{V3P3A} + 0.5V)
XIN, XOUT..............................-10mA to +10mA, -0.5V to +3.0V

SEG and SEGDIO Pins

Configured as SEG or COM Drivers. -1mA to +1mA, -0.5V to +6.0V
Configured as Digital Inputs ....-10mA to +10mA, -0.5V to +6.0V
Configured as Digital Outputs ....-10mA to +10mA, -0.5V to (V_{V3P3D} + 0.5V)

Digital Pins

Inputs (PB, RESET, RX, ICE_E, TEST)...........-10mA to +10mA, -0.5V to +6.0V
Outputs (TX).......... -10mA to +10mA, -0.5V to (V_{V3P3D} + 0.5V)

Temperature

Operating Junction Temperature (peak, 100ms).............+140°C
Operating Junction Temperature (continuous)................+125°C
Storage Temperature....................................... -45°C to +140°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow).......................................+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECOMMENDED OPERATING CONDITIONS					
$V_{V3P3SYS}$ and V_{V3P3A} Supply Voltage	Precision metering operation	3.0		3.6	V
V_{BAT}	PLL_FAST = 1	2.65		3.8	V
	PLL_FAST = 0	2.40		3.8	
V_{BAT_RTC}		2.0		3.8	V
Operating Temperature		-40		+85	°C
INPUT LOGIC LEVELS					
Digital High-Level Input Voltage (V_{IH})		2			V
Digital Low-Level Input Voltage (V_{IL})				0.8	V
Input Pullup Current, (I_{IL}) E_RTXT, E_RST, E_TCLK		10		100	µA
Input Pullup Current, (I_{IL}) OPT_RX, OPT_TX		10		100	µA
Input Pullup Current, (I_{IL}) SPI_CSZ (SEGDIO36)		10		100	µA
Input Pullup Current, (I_{IL}) Other Digital Inputs		-1		+1	µA
Input Pulldown Current (I_{IH}), ICE_E, RESET, TEST		10		100	µA
Input Pulldown Current, (I_{IH}) Other Digital Inputs		-1		+1	µA

Electrical Characteristics (continued)

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT LOGIC LEVELS					
Digital High-Level Output Voltage (V_{OH})	I_{LOAD} = 1mA	V_{V3P3D} - 0.4			V
	I_{LOAD} = 15mA (Note 1)	V_{V3P3D} - 0.8			V
Digital Low-Level Output Voltage (V_{OL})	I_{LOAD} = 1mA	0		0.4	V
	I_{LOAD} = 15mA (Note 1)	0		0.8	V
BATTERY MONITOR **Battery Voltage Equation: 3.3 + (BSENSE - BNOM3P3) x 0.0252 + STEMP x 2.79E-5 V**					
Measurement Error	V_{BAT} = 2.0V	-3.5		+3.5	%
	V_{BAT} = 2.5V	-3.5		+3.5	
	V_{BAT} = 3.0V	-3.0		+3.0	
	V_{BAT} = 3.8V	-3.0		+3.0	
Input Impedance		260			kΩ
Passivation Current	I_{BAT}(BCURR = 1) - I_{BAT}(BCURR = 0)	50	100	165	µA
TEMPERATURE MONITOR					
Temperature Measurement Equation			22.15 + STEMP x 0.085 - 0.0023 x STEMP x [($STEMP_{T85P}$ -$STEMP_{T22P}$) /(T_{85P} - T_{22P}) - 12.857]		°C
Temperature Error (Note 1)	T_A = +85°C	-3.2		+3.2	°C
	T_A = 0°C to +70°C	-2.65		+2.65	
	T_A = -20°C	-3.4		+3.4	
	T_A = -40°C	-3.8		+3.8	
V_{BAT_RTC} Charge per Measurement			2		µC
Duration of Temperature Measurement after TEMP_START			22	40	ms
SUPPLY CURRENT					
V_{V3P3A} + $V_{V3P3SYS}$ Supply Current (Note 1)	V_{V3P3A} = $V_{V3P3SYS}$ = 3.3V; MPU_DIV = 3 (614kHz MPU clock); PLL_FAST = 1; PRE_E = 0		7.2	8.5	mA
	PLL_FAST = 0		2.9	3.8	
	PRE_E = 1		7.3	8.7	
	PLL_FAST = 0, PRE_E = 1		3.0	3.9	
Dynamic Current			0.4	0.6	mA/MHz

Electrical Characteristics (continued)

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{BAT} Current	Mission mode		-300		+300	nA
	Brownout mode			2.4	3.2	mA
	LCD mode (external V_{LCD})			0.4	108	nA
	LCD mode (internal V_{LCD} from DAC)			3.0	16	µA
	LCD mode (V_{BAT})			1.4	3.8	µA
	Sleep mode		-300		+300	nA
V_{BAT_RTC} Current	Brownout mode			400	650	nA
	LCD mode			1.8	4.1	µA
	Sleep mode, $T_A \leq 25°C$			0.7	1.7	µA
	Sleep mode, T_A = 85°C (Note 1)			1.5	3.2	µA
Flash Write Current	Maximum flash write rate			7.1	9.3	mA
V_{V3P3D} SWITCH						
On-Resistance	$V_{V3P3SYS}$ to V_{V3P3D}, $I_{V3P3D} \leq 1mA$				11	Ω
	V_{BAT} to V_{V3P3D}, $I_{V3P3D} \leq 1mA$				11	
I_{OH}			9			mA
INTERNAL POWER FAULT COMPARATOR						
Response Time	100mV overdrive, falling		20		200	µs
	100mV overdrive, rising				200	
Falling Threshold, 3.0V Comparator			2.83	2.93	3.03	V
Falling Threshold, 2.8V Comparator			2.71	2.81	2.91	V
Difference between 3.0V and 2.8V comparators			47	136	220	mV
Falling Threshold, 2.25V Comparator			2.14	2.33	2.51	V
Falling Threshold, 2.0V Comparator			1.90	2.07	2.23	V
Difference between 2.25V and 2.0V Comparators			0.15	0.25	0.365	V
Hysteresis	T_A = +22°C	3.0V comparator	13	45	81	mV
		2.8V comparator	17	42	79	
		2.25V comparator	7	33	71	
		2.0V comparator	4	28	83	

Electrical Characteristics (continued)

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
2.5V REGULATOR					
V_{V2P5} Output Voltage	V_{V3P3} = 3.0V to 3.8V, I_{LOAD} = 0mA	2.55	2.65	2.75	V
V_{V2P5} Load Regulation	V_{BAT} = 3.3V, V_{V3P3} = 0V, I_{LOAD} = 0mA to 1mA			40	mV
Dropout Voltage	I_{LOAD} = 5mA			440	mV
	I_{LOAD} = 0mA			200	
PSSR	I_{LOAD} = 0mA		5		mV/V
CRYSTAL OSCILLATOR					
Maximum Output Power to Crystal				1	μW
PLL					
PLL Settling Time	Power-up		3		ms
	PLL_FAST transition, low to high		3		
	PLL_FAST transition, high to low		3		
	Mode transition, sleep to mission		3		
LCD					
V_{LCD} Current	V_{LCD} = 3.3V, LCD frequency = 512Hz, all segments on		8.1		μA
	V_{LCD} = 3.3V, LCD frequency = 256Hz, all segments on		4.6		
	V_{LCD} = 3.3V, all segments off			2.1	
	V_{LCD} = 5.0V, LCD frequency = 512Hz, all segments on		12.0		
	V_{LCD} = 5.0V, LCD frequency = 256Hz, all segments on		4.6		
	V_{LCD} = 5.0V, all segments off			3.0	
V_{REF}					
V_{REF} Output Voltage	T_A = +22°C	1.193	1.195	1.197	V
V_{REF} Output Impedance	I_{LOAD} = -10μA to +10μA			3.2	kΩ
V_{REF} Power Supply Sensitivity	V_{V3P3A} = 3.0V to 3.6V	-1.5		+1.5	mV/V
V_{REF} Temperature Sensitivity (Note 1)		$V_{REFT} = V_{REF22} + (T-22)TC_1 + (T-22)^2 TC_2$			V
	71M6543FT/71M6543GT	TC_1 = 151 - 2.77 x TRIMT			μV/°C
	71M6543HT/71M6543GHT	TC_1 = 33.264 + 0.08 x TRIMT + 1.587 x (TRIMBGB - TRIMBGD)			μV/°C
		TC_2 = -0.528 - 0.00128 x TRIMT			μV/°C²
V_{REF} Error (Note 1)	71M6543FT/71M6543GT (-40°C to +85°C)	-40		+40	ppm/°C
	71M6543HT/71M6543GHT (-40°C to -20°C)	-16		+16	
	71M6543HT/71M6543GHT (-20°C to +85°C)	-10		+10	

Electrical Characteristics (continued)

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ADC					
Recommended Input Range (All Analog Inputs, Relative to V_{V3P3A})		-250		+250	mV Peak
Recommended Input Range, IADC0-IADC1, Preamp Enabled		-31.25		+31.25	mV Peak
Input Impedance	f_{IN} = 65Hz	40		100	kΩ
ADC Gain Error vs. Power Supply	V_{IN} = 200mV peak, 65Hz, V_{V3P3A} = 3.0V to 3.6V	-30		+70	ppm/%
Input Offset Voltage	Differential or single-ended modes	-10		+10	mV
THD	250mV peak, 65Hz, 64k points, Blackman-Harris window, FIR_LEN = 2, ADC_DIV = 1, PLL_FAST = 1, MUX_DIV = 2		-93		dB
	20mV peak, 65Hz, 64k points, Blackman-Harris window, FIR_LEN = 2, ADC_DIV = 1, PLL_FAST = 1, MUX_DIV = 2		-90		
LSB Size	FIR_LEN = 2, ADC_DIV = 1, PLL_FAST = 1, MUX_DIV = 2		151		nV
Digital Full Scale	FIR_LEN = 2, ADC_DIV = 1, PLL_FAST = 1, MUX_DIV = 2		±2,097,152		LSB
PREAMPLIFIER					
Differential Gain		7.88	7.98	8.08	V/V
Gain Variation vs. Temperature	T_A = -40°C to +85°C (Note 1)	-30	-10	+15	ppm/°C
Gain Variation vs. V3P3	V_{V3P3} = 2.97V to 3.63V (Note 1)	-100		+100	ppm/%
Phase Shift	(Note 1)	+10		+22	m°
Preamp Input Current		3	6	9	µA
THD, Preamp + ADC	V_{IN} = 30mV		-88		dB
	V_{IN} = 15mV		-88		
Preamp Input Offset Voltage	IADC0 = IADC1 = V_{V3P3} + 30mV		-0.63		mV
	IADC0 = IADC1 = V_{V3P3} + 15mV		-0.57		
	IADC0 = IADC1 = V_{V3P3}		-0.56		
	IADC0 = IADC1 = V_{V3P3} - 15mV		-0.56		
	IADC0 = IADC1 = V_{V3P3} - 30mV		-0.55		
Phase Shift Over Temperature	(Note 1)	-0.03		+0.03	m°/C

Electrical Characteristics (continued)

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

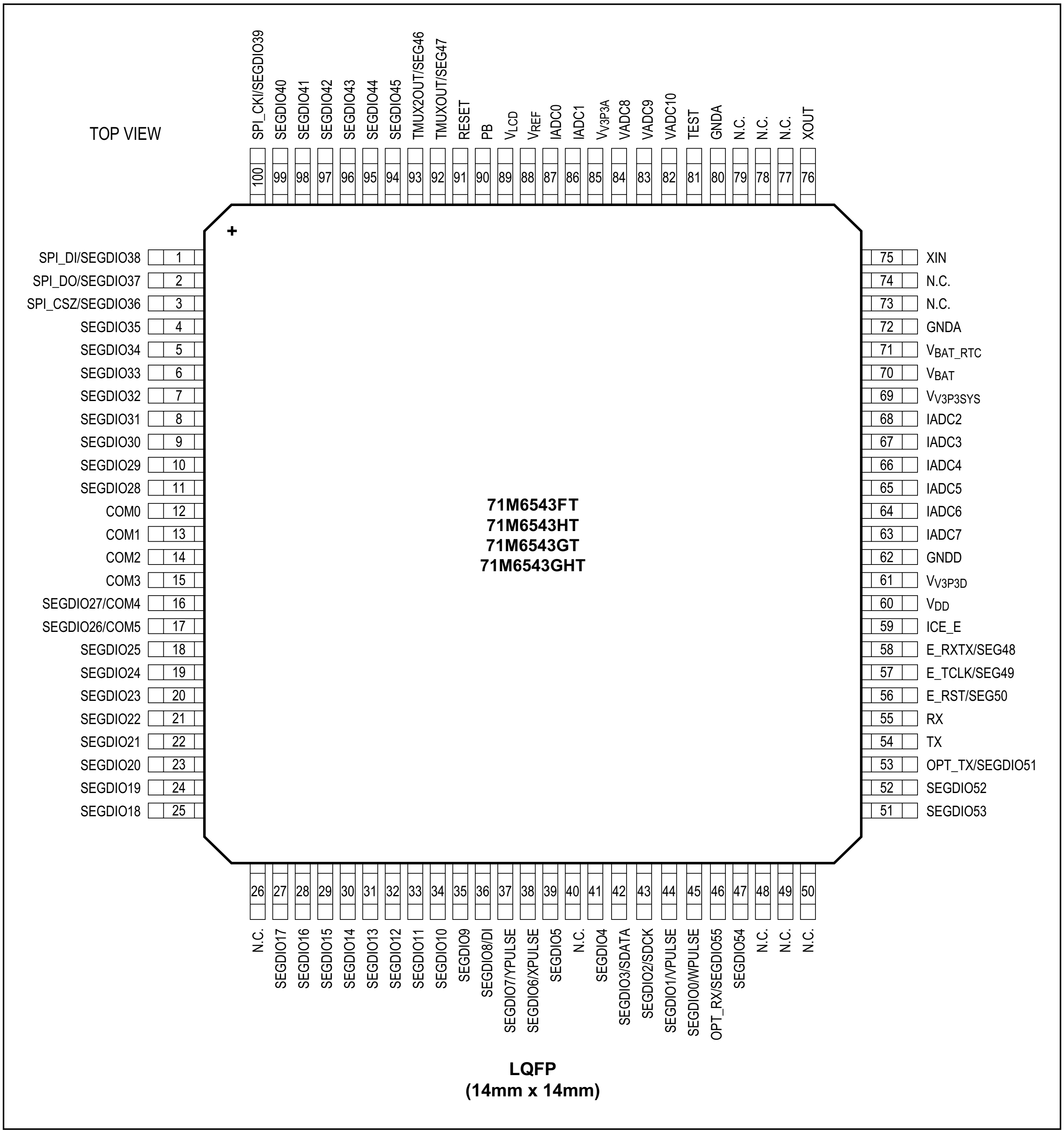
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FLASH MEMORY					
Endurance		20,000			Cycles
Data Retention	T_A = +25°C	100			Years
Byte Writes Between Erase Operations				2	Cycles
Write Time, per byte	Per 2 bytes if using SPI			50	µs
Page Erase Time				22	ms
Mass Erase Time				22	ms
SPI					
Data-to-Clock Setup Time		10			ns
Data Hold Time From Clock		10			ns
Output Delay, Clock to Data				40	ns
CS-to-Clock Setup Time		10			ns
Hold Time, CS to Clock		15			ns
Clock High Period		40			ns
Clock Low Period		40			ns
Clock Frequency (as a multiple of CPU frequency)				2.0	MHz/MHz
Space between SPI Transactions		4.5			CPU Cycles
EEPROM INTERFACE					
I^2C SCL Frequency	MPU clock = 4.9MHz, using interrupts		310		kHz
	MPU clock = 4.9MHz, bit-banging DIO2-DIO3		100		
3-Wire Write Clock Frequency	MPU clock = 4.9MHz, PLL_FAST = 0		160		kHz
	MPU clock = 4.9MHz, PLL_FAST = 1		490		
RESET					
Reset Pulse Width	(Note 1)	5			µs
Reset Pulse Fall Time	(Note 1)			1	µs
INTERNAL CALENDAR					
Year Date Range		2000		2255	Years

Recommended External Components

NAME	FROM	TO	FUNCTION	VALUE	UNITS
C1	V_{V3P3A}	GNDA	Bypass capacitor for 3.3V supply	≥ 0.1 ±20%	µF
C2	V_{V3P3D}	GNDD	Bypass capacitor for 3.3V output	0.1 ±20%	µF
CSYS	$V_{V3P3SYS}$	GNDD	Bypass capacitor for $V_{V3P3SYS}$	≥ 1.0 ±30%	µF
CVDD	V_{DD}	GNDD	Bypass capacitor for V_{DD}	0.1 ±20%	µF
CVLCD	V_{LCD}	GNDD	Bypass capacitor for V_{LCD} pin	≥ 0.1 ±20%	µF
XTAL	XIN	XOUT	32.768 kHz crystal; electrically similar to ECS .327-12.5-17X, Vishay XT26T or Suntsu SCP6–32.768kHz TR (load capacitance 12.5pF)	32.768	kHz
CXS (Note 2)	XIN	GNDA	Load capacitor values for crystal depend on crystal specifications and board parasitics. Nominal values are based on 3pF allowance for the sum of board and chip capacitances.	22 ±10%	pF
CXL (Note 2)	XOUT	GNDA		22 ±10%	pF

Note 1: Parameter not tested in production, guaranteed by design to six-sigma.
Note 2: If the capacitor values of CXS = 15pF and CXL = 10pF have already been installed, then changing the CXL value to 33pF and leaving CXS = 15pF would minimize rework.

Pin Configuration



Pin Descriptions

PIN 100	NAME	TYPE	CIRCUIT	FUNCTION
POWER AND GROUND PINS				
72, 80	GNDA	P	—	Analog Ground. This pin should be connected directly to the ground plane.
62	GNDD	P	—	Digital Ground. This pin should be connected directly to the ground plane.
85	V_{V3P3A}	P	—	Analog Power Supply. A 3.3V power supply should be connected to this pin. V_{V3P3A} must be the same voltage as $V_{V3P3SYS}$.
69	$V_{V3P3SYS}$	P	—	System 3.3V supply. This pin should be connected to a 3.3V power supply.
61	V_{V3P3D}	O	13	Auxiliary Voltage Output of the Chip. In mission mode, this pin is connected to $V_{V3P3SYS}$ by the internal selection switch. In BRN mode, it is internally connected to V_{BAT}. V_{V3P3D} is floating in LCD and sleep mode. A 0.1µF bypass capacitor to ground must be connected to this pin.
60	V_{DD}	O	—	Output of the 2.5V Regulator. This pin is powered in MSN and BRN modes. A 0.1µF bypass capacitor to ground should be connected to this pin.
89	V_{LCD}	O	—	Output of the LCD DAC. A 0.1µF bypass capacitor to ground should be connected to this pin.
70	V_{BAT}	P	12	Battery Backup Pin to Support the Battery Modes (BRN, LCD). A battery or super capacitor is to be connected between V_{BAT} and GNDD. If no battery is used, connect V_{BAT} to $V_{V3P3SYS}$.
71	V_{BAT_RTC}	P	12	RTC and Oscillator Power Supply. A battery or super capacitor is to be connected between V_{BAT} and GNDD. If no battery is used, connect V_{BAT_RTC} to $V_{V3P3SYS}$.
ANALOG PINS				
87, 86	IADC0 IADC1	I	6	Differential or Single-Ended Line Current Sense Inputs. These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of current sensors. Unused pins must be tied to V_{V3P3A}. Pins IADC2-IADC3, IADC4-IADC5 and IADC6-IADC7 may be configured for communication with the remote sensor interface (71M6x03).
68, 67	IADC2 IADC3			
66, 65	IADC4 IADC5			
64, 63	IADC6 IADC7			
84, 83, 82	VADC8 (VA), VADC9 (VB), VADC10 (VC)	I	6	Line Voltage Sense Inputs. These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of resistor-dividers. Unused pins must be tied to V_{V3P3A}.
88	V_{REF}	O	9	Voltage Reference for the ADC. This pin should be left unconnected (floating).
75	XIN	I	8	Crystal Inputs. A 32.768kHz crystal should be connected across these pins. Typically, a 22pF capacitor is also connected from XIN to GNDA and a 22pF capacitor is connected from XOUT to GNDA. It is important to minimize the capacitance between these pins. See the crystal manufacturer data sheet for details. If an external clock is used, a 150mV$_{P-P}$ clock signal should be applied to XIN, and XOUT should be left unconnected.
76	XOUT	O		

Pin Descriptions (continued)

<table>
<tr><th>PIN
100</th><th>NAME</th><th>TYPE</th><th>CIRCUIT</th><th>FUNCTION</th></tr>
<tr><td colspan="5">DIGITAL PINS</td></tr>
<tr><td>12–15</td><td>COM0–COM3</td><td>O</td><td>5</td><td>LCD Common Outputs. These four pins provide the select signals for the LCD display.</td></tr>
<tr><td>45</td><td>SEGDIO0/WPULSE</td><td rowspan="19">I/O</td><td rowspan="19">3, 4, 5</td><td rowspan="19">Multiple-Use Pins. Configurable as either LCD segment driver or DIO. Alternative functions with proper selection of associated I/O RAM registers are:
SEGDIO0 = WPULSE
SEGDIO1 = VPULSE
SEGDIO2 = SDCK
SEGDIO3 = SDATA
SEGDIO6 = XPULSE
SEGDIO7 = YPULSE
SEGDIO8 = DI
SEGDIO16 = RX3
SEGDIO17 = TX3
Unused pins must be configured as outputs or terminated to V3P3/GNDD.</td></tr>
<tr><td>44</td><td>SEGDIO1/VPULSE</td></tr>
<tr><td>43</td><td>SEGDIO2/SDCK</td></tr>
<tr><td>42</td><td>SEGDIO3/SDATA</td></tr>
<tr><td>41</td><td>SEGDIO4</td></tr>
<tr><td>39</td><td>SEGDIO5</td></tr>
<tr><td>38</td><td>SEGDIO6/XPULSE</td></tr>
<tr><td>37</td><td>SEGDIO7/YPULSE</td></tr>
<tr><td>36</td><td>SEGDIO8/DI</td></tr>
<tr><td>35–30</td><td>SEGDIO[9:14]</td></tr>
<tr><td>29–27</td><td>SEGDIO[15:17]</td></tr>
<tr><td>25</td><td>SEGDIO[18]</td></tr>
<tr><td>24–18</td><td>SEGDIO[19:25]</td></tr>
<tr><td>11–4</td><td>SEGDIO[28:35]</td></tr>
<tr><td>95–94</td><td>SEGDIO[44:45]</td></tr>
<tr><td>99–96</td><td>SEGDIO[40:43]</td></tr>
<tr><td>52</td><td>SEGDIO52</td></tr>
<tr><td>51</td><td>SEGDIO53</td></tr>
<tr><td>47</td><td>SEGDIO54</td></tr>
<tr><td>17</td><td>SEGDIO26/COM5</td><td rowspan="2">I/O</td><td rowspan="2">3, 4, 5</td><td rowspan="2">Multiple-Use Pins. Configurable as either LCD segment driver or DIO with alternative function (LCD common drivers).</td></tr>
<tr><td>16</td><td>SEGDIO27/COM4</td></tr>
<tr><td>3</td><td>SPI_CSZ/SEGDIO36</td><td rowspan="4">I/O</td><td rowspan="4">3, 4, 5</td><td rowspan="4">Multiple-Use Pins. Configurable as either LCD segment driver or DIO with alternative function (SPI interface).</td></tr>
<tr><td>2</td><td>SPI_DO/SEGDIO37</td></tr>
<tr><td>1</td><td>SPI_DI/SEGDIO38</td></tr>
<tr><td>100</td><td>SPI_CKI/SEGDIO39</td></tr>
<tr><td>53</td><td>OPT_TX/SEGDIO51</td><td rowspan="2">I/O</td><td rowspan="2">3, 4, 5</td><td rowspan="2">Multiple-Use Pins, configurable as either LCD segment driver or DIO with alternative function (optical port/UART1)</td></tr>
<tr><td>46</td><td>OPT_RX/SEGDIO55</td></tr>
<tr><td>58</td><td>E_RXTX/SEG48</td><td rowspan="2">I/O</td><td rowspan="2">1, 4, 5</td><td rowspan="2">Multiuse Pins. Configurable as either emulator port pins (when ICE_E pulled high) or LCD segment drivers (when ICE_E tied to GND).</td></tr>
<tr><td>56</td><td>E_RST/SEG50</td></tr>
<tr><td>57</td><td>E_TCLK/SEG49</td><td>O</td><td>4, 5</td><td></td></tr>
<tr><td>59</td><td>ICE_E</td><td>I</td><td>2</td><td>ICE Enable. When zero, E_RST, E_TCLK, and E_RXTX become SEG50, SEG49, and SEG48, respectively. For production units, this pin should be pulled to GND to disable the emulator port.</td></tr>
<tr><td>92</td><td>TMUXOUT/SEG47</td><td rowspan="2">O</td><td rowspan="2">4, 5</td><td rowspan="2">Multiple-Use Pins. Configurable as either multiplexer/clock output or LCD segment driver using the I/O RAM registers.</td></tr>
<tr><td>93</td><td>TMUX2OUT/SEG46</td></tr>
<tr><td>91</td><td>RESET</td><td>I</td><td>2</td><td>Chip Reset. This input pin is used to reset the chip into a known state. For normal operation, this pin is pulled low. To reset the chip, this pin should be pulled high. This pin has an internal 30FA (nominal) current source pulldown. No external reset circuitry is necessary.</td></tr>
</table>

Pin Descriptions (continued)

PIN	NAME	TYPE	CIRCUIT	FUNCTION
100				
55	RX	I	3	UART0 Input. If this pin is unused it must be terminated to V_{V3P3D} or GNDD.
54	TX	O	4	UART0 Output
81	TEST	I	7	Enables Production Test. This pin must be grounded in normal operation.
90	PB	I	3	Pushbutton Input. This pin must be at GNDD when not active or unused. A rising edge sets the WF_PB flag. It also causes the part to wake up if it is in SLP or LCD mode. PB does not have an internal pullup or pulldown resistor.
26, 40, 48, 49, 50, 73, 74, 77, 78, 79, 84	N.C.	N.C.	—	No Connection. Do not connect these pins.

I = Input, O = Output, P = Power

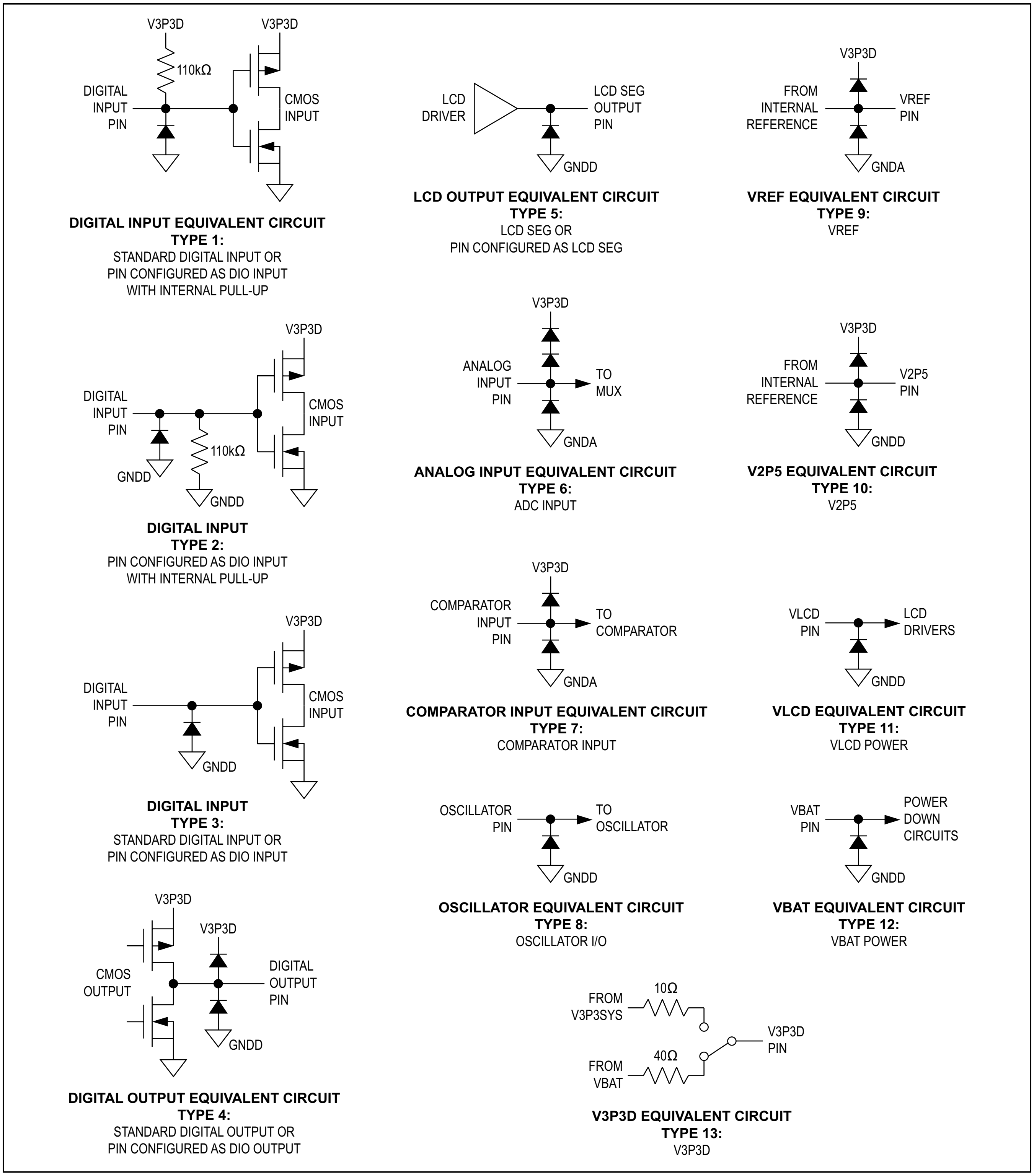
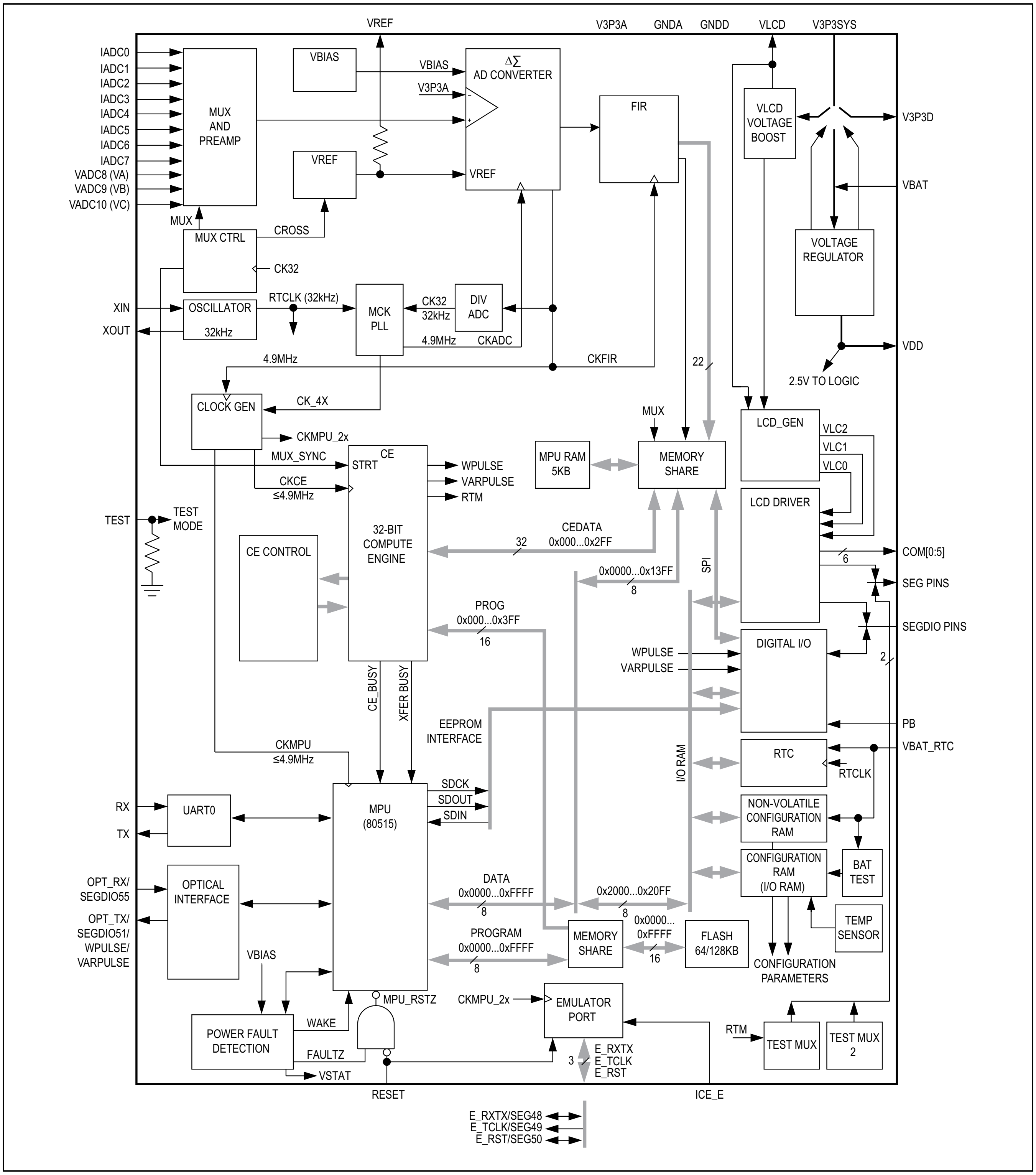


Figure 1. I/O Equivalent Circuits

Block Diagram



Hardware Description

The 71M6543FT/HT/GT/GHT single-chip energy meter ICs integrate all primary functional blocks required to implement a solid-state residential electricity meter. Included on the chip are the following:

- An analog front-end (AFE) featuring a 22-bit second-order sigma-delta ADC
- An independent 32-bit digital computation engine (CE) to implement DSP functions
- An 8051-compatible microprocessor (MPU) which executes one instruction per clock cycle (80515)
- A precision voltage reference (V_{REF})
- A temperature sensor for digital temperature compensation:
  - Metrology digital temperature compensation (MPU)
  - Automatic RTC digital temperature compensation operational in all power states
- LCD drivers
- RAM and flash memory
- A real-time clock (RTC)
- A variety of I/O pins
- A power-failure interrupt
- A zero-crossing interrupt
- Selectable current sensor interfaces for locally-connected sensors as well as isolated sensors (i.e., using the 71M6x03 companion IC with a shunt resistor sensor)
- Resistive shunt and current transformers are supported

Resistive shunts and current transformer (CT) current sensors are supported. Resistive shunt current sensors may be connected directly to the 71M654xT device or isolated using a companion 71M6x03 isolator IC in order to implement a variety of metering configurations. An inexpensive, small pulse transformer is used to isolate the 71M6x03 isolated sensor from the 71M654xT. The 71M654xT performs digital communications bidirectionally with the 71M6x03 and also provides power to the 71M6x03 through the isolating pulse transformer. Isolated (remote) shunt current sensors are connected to the differential input of the 71M6x03. Included on the 71M6x03 companion isolator chip are:

- Digital isolation communications interface
- An analog front-end (AFE)
- A precision voltage reference (V_{REF})
- A temperature sensor (for digital temperature compensation)
- A fully differential shunt resistor sensor input
- A preamplifier to optimize shunt current sensor performance
- Isolated power circuitry obtains dc power from pulses sent by the 71M654xT

In a typical application, the 32-bit compute engine (CE) of the 71M654xT sequentially processes the samples from the voltage inputs on analog input pins and from the external 71M6x03 isolated sensors and performs calculations to measure active energy (Wh) and reactive energy (VARh), as well as A^2h, and V^2h for four-quadrant metering. These measurements are then accessed by the MPU, processed further and output using the peripheral devices available to the MPU.

In addition to advanced measurement functions, the clock function allows the 71M6543FT/HT/GT/GHT to record time-of-use (TOU) metering information for multi-rate applications and to time-stamp tamper or other events. Measurements can be displayed on 3.3V LCDs commonly used in low-temperature environments. Flexible mapping of LCD display segments facilitate integration of existing custom LCDs. Design trade-off between the number of LCD segments and DIO pins can be implemented in software to accommodate various requirements.

In addition to the temperature-trimmed ultra-precision voltage reference, the on-chip digital temperature compensation mechanism includes a temperature sensor and associated controls for correction of unwanted temperature effects on measurement and RTC accuracy, e.g., to meet the requirements of ANSI and IEC standards. Temperature-dependent external components such as crystal oscillator, resistive shunts, current transformers (CTs) and their corresponding signal conditioning circuits can be characterized and their correction factors can be programmed to produce electricity meters with exceptional accuracy over the industrial temperature range.

One of the two internal UARTs is adapted to support an Infrared LED with internal drive and sense configuration and can also function as a standard UART. The optical output can be modulated at 38kHz. This flexibility makes it possible to implement AMR meters with an IR interface. A block diagram of the IC is shown in Figure 1.

Analog Front-End (AFE)

The AFE functions as a data acquisition system, controlled by the MPU. When used with locally connected sensors, as shown in Figure 2, the analog input signals (IADC0-IADC7, VADC8-VADC10) are multiplexed to the ADC input and sampled by the ADC.

The ADC output is decimated by the FIR filter and stored in CE RAM where it can be accessed and processed by the CE.

When remote isolated sensors are connected to the 71M6543FT/HT/GT/GHT using 71M6x03 remote sensor interfaces, the input multiplexer is bypassed. Instead, the extracted modulator bit stream is passed directly to a dedicated decimation filter. The output of the decimation filter is then directly stored in the appropriate CE RAM location without making use of a multiplexer cycle.

Signal Input Pins

The 71M6543FT/HT/GT/GHT features eleven ADC inputs.

IADC0-IADC7 are intended for use as current sensor inputs. These eight current sensor inputs can be configured as four single-ended inputs, or (more frequently) can be paired to form four differential inputs. For best performance, it is recommended to configure the current sensor inputs as differential inputs. The first differential input (IADC0-IADC1) features a preamplifier with a selectable gain of 1 or 8, and is intended for direct connection to a shunt resistor sensor, and can also be used with a current transformer (CT). The remaining differential pairs may be

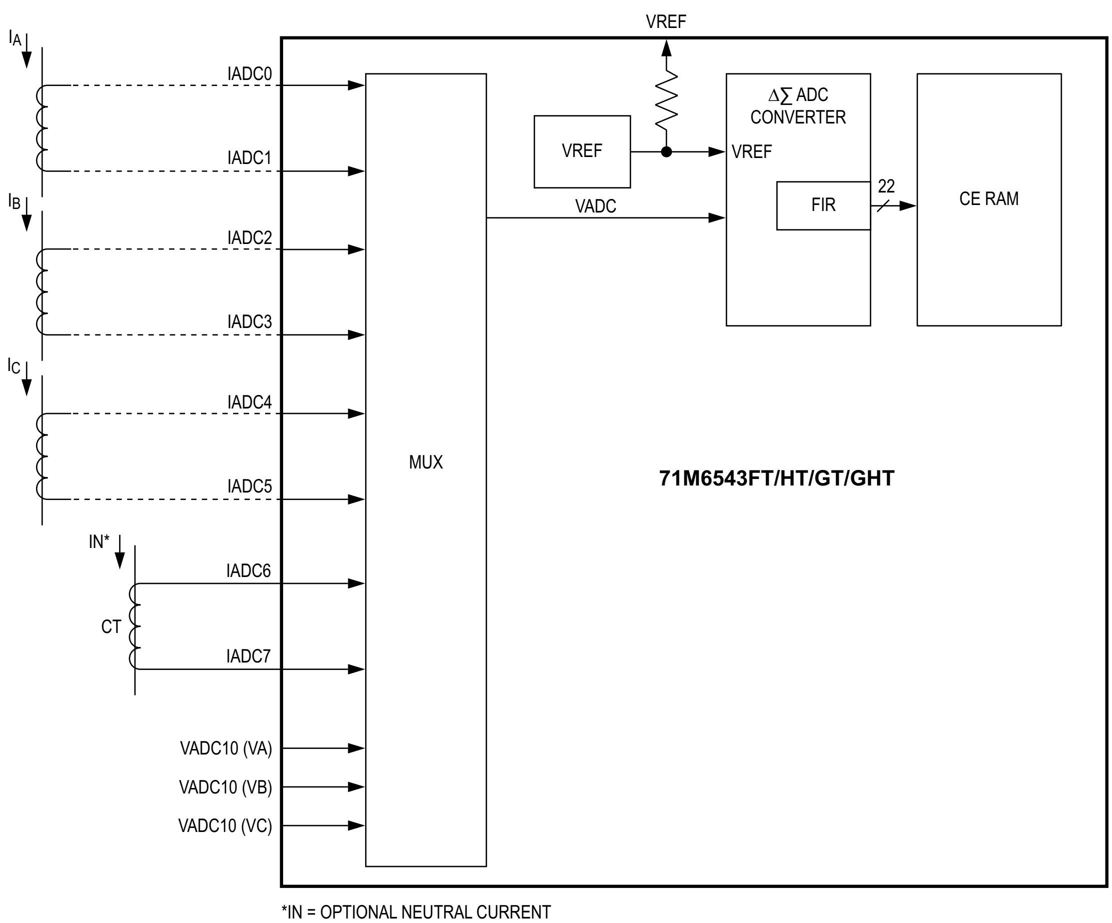


Figure 2. 71M6543FT/HT/GT/GHT Operating with Local Sensors

used with CTs, or may be enabled to interface to a remote 71M6x03 isolated current sensor providing isolation for a shunt resistor sensor using a low cost pulse transformer.

The remaining inputs (VADC8-VADC10) are single-ended and sense line voltage. These single-ended inputs are referenced to the V_{V3P3A} pin.

All analog signal input pins measure voltage. In the case of shunt current sensors, currents are sensed as a voltage drop in the shunt resistor sensor. Referring to Figure 2, shunt sensors can be connected directly to the 71M654xT (referred to as a 'local' shunt sensor) or connected via an isolated 71M6x03 (referred to as a 'remote' shunt sensor) (Figure 3). In the case of current transformers, the current is measured as a voltage across a burden resistor that is connected to the secondary winding of the CT. Meanwhile, line voltages are sensed through resistive voltage dividers.

Pins IADC0-IADC1 can be programmed individually to be differential or single-ended. For most applications IADC0-IADC1 are configured as a differential input to work with a shunt or CT directly interfaced to the IADC0-IADC1 differential input with the appropriate external signal conditioning components.

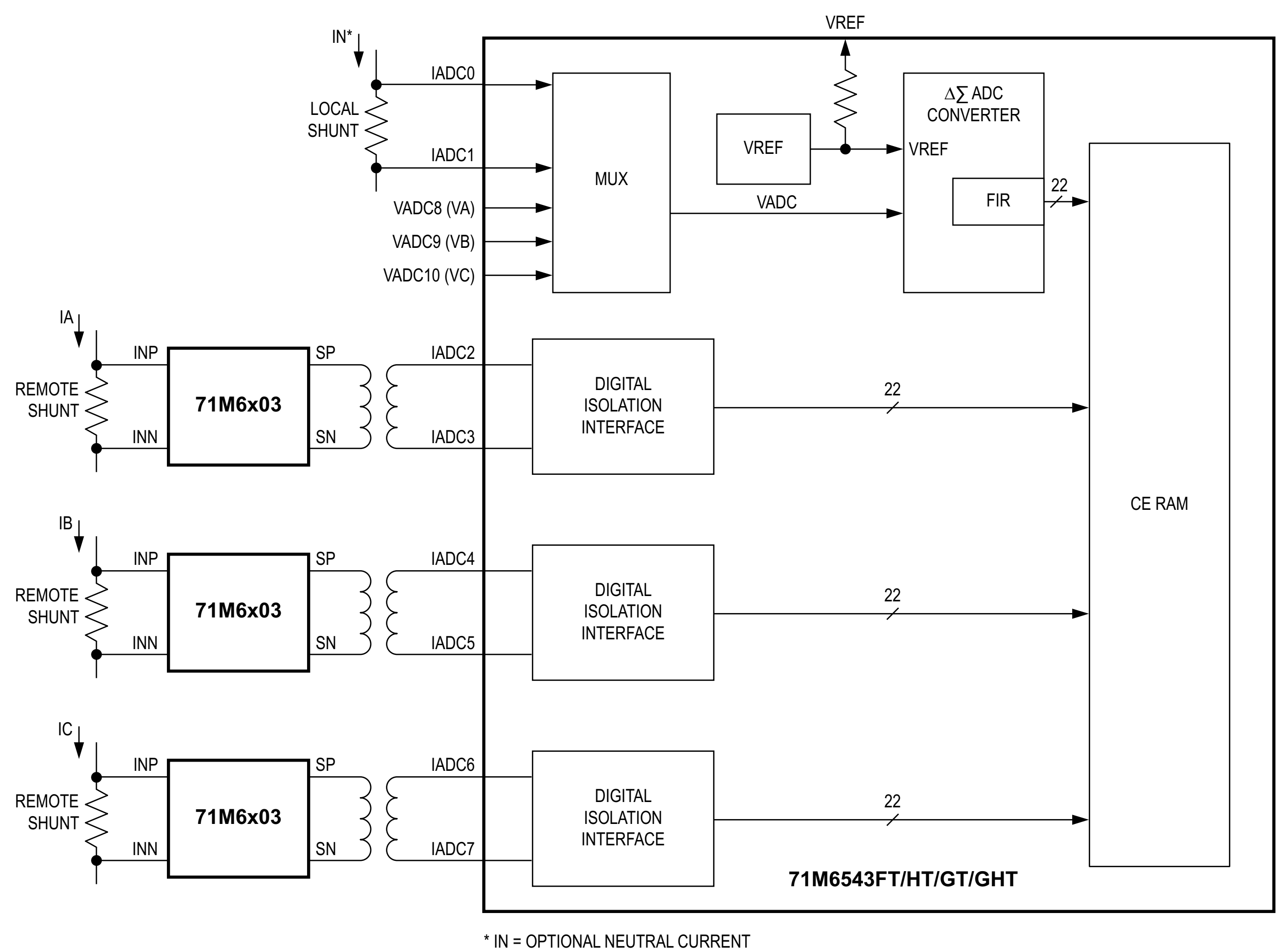


Figure 3. 71M6543FT/HT/GT/GHT Operating with Remote Sensor for Neutral Current

The performance of the IADC0-IADC1 pins can be enhanced by enabling a preamplifier with a fixed gain of 8. When the PRE_E bit = 1, IADC0-IADC1 become the inputs to the 8x preamplifier, and the output of this amplifier is supplied to the multiplexer. The 8x amplification is useful when current sensors with low sensitivity, such as shunt resistors, are used. With PRE_E set, the IADC0-IADC1 input signal amplitude is restricted to 31.25 mV peak.

When shunt resistors are used as current sense elements on all current inputs, the IADC0-IADC1 pins are configured for differential mode to interface to a local shunt by setting the DIFFA_E control bit. Meanwhile, the IADC2-IADC7 pins are re-configured as digital balanced pair to communicate with a 71M6x03 isolated sensor interface by setting the RMT_E control bit. The 71M6x03 communicates with the 71M654xT using a bidirectional digital data stream through an isolating low-cost pulse transformer. The 71M654xT also supplies power to the 71M6x03 through the isolating transformer.

When using current transformers the IADC2-IADC7 pins are configured as local analog inputs (RMT_E = 0). The IADC0-IADC1 pins cannot be configured as a remote sensor interface.

Input Multiplexer

When operating with local sensors, the input multiplexer sequentially applies the input signals from the analog input pins to the input of the ADC. One complete sampling sequence is called a multiplexer frame. The multiplexer of the 71M6543FT/HT/GT/GHT can select up to seven input signals (three voltage inputs and four current inputs) per multiplexer frame. The multiplexer always starts at state 1 and proceeds until as many states as determined by MUX_DIV[3:0] have been converted.

The 71M6543FT/HT/GT/GHT requires CE code that is written for the specific application. Moreover, each CE code requires specific AFE and MUX settings in order to function properly. Contact Maxim Integrated for specific information about alternative CE codes.

For a polyphase configuration with neutral current sensing using shunt resistor current sensors and the 71M6xx3 isolated sensors, as shown in Figure 3, the IADC0-IADC1 input must be configured as a differential input, to be connected to a local shunt. The local shunt connected to the IADC0-IADC1 input is used to sense the Neutral current. The voltage sensors (VADC8-VADC10) are also directly connected to the 71M6543FT/HT/GT/GHT and are also routed though the multiplexer. Meanwhile, the IADC2-IADC7 current inputs are configured as remote sensor digital interfaces and the corresponding samples are not routed through the multiplexer.

For a polyphase configuration with optional neutral current sensing using Current Transformer (CTs) sensors, all four current sensor inputs must be configured as differential inputs. IADC2-IADC3 is connected to phase A, IADC4-IADC5 is connected to phase B, and IADC6-IADC7 is connected to phase C. The IADC0-IADC1 current sensor input is optionally used to sense the Neutral current for anti-tampering purposes. The voltage sensors (VADC8-VADC10), typically resistive dividers, are directly connected to the 71M6543FT/HT/GT/GHT. No 71M6xx3 isolated sensors are used in this configuration and all signals are routed though the multiplexer.

The multiplexer sequence shown in Figure 4 corresponds to the configuration shown in Figure 3. The frame duration is 13 CK32 cycles (where CK32 = 32,768Hz), therefore, the resulting sample rate is 32,768 Hz/13 = 2,520.6Hz.

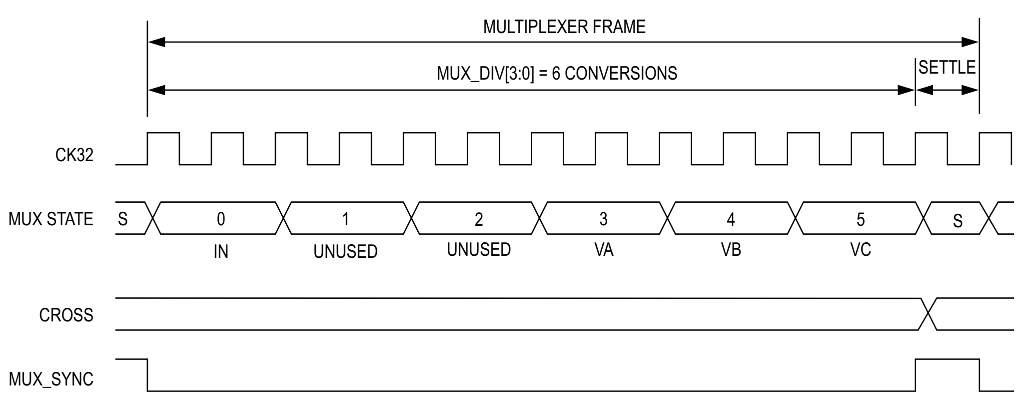


Figure 4. Multiplexer Sequence with Neutral Channel and Remote Sensors

Note that Figure 4 only shows the currents that pass through the 71M6543FT/HT/GT/GHT multiplexer, and does not show the currents that are copied directly into CE RAM from the remote sensors (see Figure 3), which are sampled during the second half of the multiplexer frame. The two unused conversion slots shown are necessary to produce the desired 2,520.6Hz sample rate.

The multiplexer sequence shown in Figure 5 corresponds to the CT configuration shown in Figure 2. Since in this case all current sensors are locally connected to the 71M6543FT/HT/GT/GHT, all currents are routed through the multiplexer, as seen in Figure 2. For this multiplexer sequence, the frame duration is 15 CK32 cycles (where CK32 = 32,768Hz), therefore, the resulting sample rate is 32,768 Hz/15 = 2,184.5Hz.

Delay Compensation

When measuring the energy of a phase (i.e., Wh and VARh) in a service, the voltage and current for that phase must be sampled at the same instant. Otherwise, the phase difference, Φ, introduces errors.

$$\varphi = \frac{t_{delay}}{T} \cdot 360^\circ = t_{delay} \cdot f \cdot 360^\circ$$

Where f is the frequency of the input signal, T = 1/f and t_{delay} is the sampling delay between current and voltage.

Traditionally, sampling is accomplished by using two A/D converters per phase (one for voltage and the other one for current) controlled to sample simultaneously. Our Single Converter Technology, however, exploits the 32-bit signal processing capability of its CE to implement "constant delay" allpass filters. The allpass filter corrects for the conversion time difference between the voltage and the corresponding current samples that are obtained with a single multiplexed A/D converter.

The "constant delay" allpass filter provides a broad-band delay 360° – θ, which is precisely matched to the difference in sample time between the voltage and the current of a given phase. This digital filter does not affect the amplitude of the signal, but provides a precisely controlled phase response.

The recommended ADC multiplexer sequence samples the current first, immediately followed by sampling of the corresponding phase voltage, thus the voltage is delayed by a phase angle Φ relative to the current. The delay compensation implemented in the CE aligns the voltage samples with their corresponding current samples by first delaying the current samples by one full sample interval (i.e., 360°), then routing the voltage samples through the allpass filter, thus delaying the voltage samples by 360o - θ, resulting in the residual phase error between the current and its corresponding voltage of B – Φ. The residual phase error is negligible, and is typically less than ±1.5 milli-degrees at 100Hz, thus it does not contribute to errors in the energy measurements.

When using remote sensors, the CE performs the same delay compensation described above to align each voltage sample with its corresponding current sample. Even though the remote current samples do not pass through the 71M654xT multiplexer, their timing relationship to their corresponding voltages is fixed and precisely known.

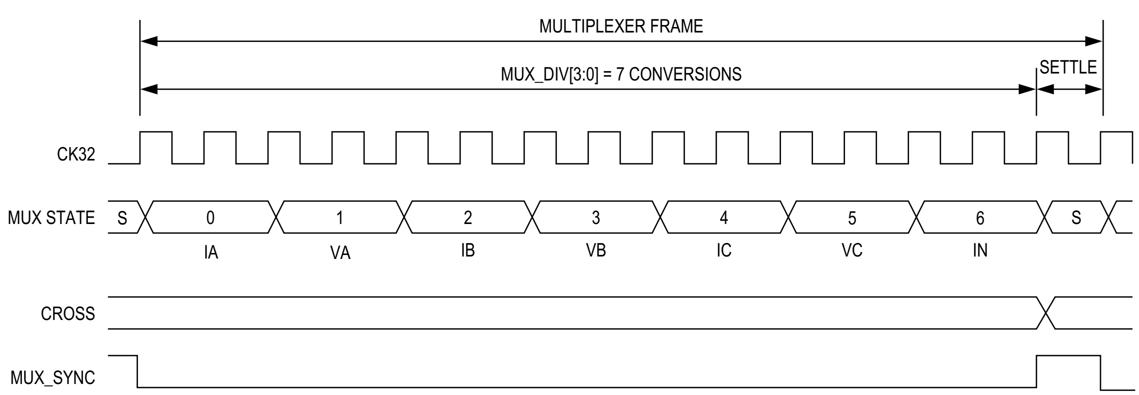


Figure 5. Multiplexer Sequence with Neutral Channel and Current Transformers

Table 1. ADC Input Configuration

PIN	REQUIRED SETTING	COMMENT
IADC0 IADC1	DIFFx_E = 1	Differential mode must be selected with DIFFx_E = 1. The ADC results are stored in ADC0 and ADC1 is not disturbed.
IADC2 IADC3	DIFFx_E = 1 or RMT_E = 1	For locally connected sensors the differential input must be enabled. For the remote sensor RMT_E must be set. ADC results are stored in ADC2 and ADC3 is not disturbed.
IADC4 IADC5	DIFFx_E = 1 or RMT_E = 1	For locally connected sensors the differential input must be enabled. For the remote sensor RMT_E must be set. ADC results are stored in ADC4 and ADC5 is not disturbed.
IADC6 IADC7	DIFFx_E = 1 or RMT_E = 1	For locally connected sensors the differential input must be enabled. For the remote sensor RMT_E must be set. ADC results are stored in ADC6 and ADC7 is not disturbed.
VADC8	—	Phase A voltage. Single ended mode only. ADC result stored in ADC8.
VADC9	—	Phase B voltage. Single ended mode only. ADC result stored in ADC9.
VADC10	—	Phase A voltage. Single ended mode only. ADC result stored in ADC10.

ADC Preamplifier

The ADC preamplifier is a low-noise differential amplifier with a fixed gain of 8 available only on the IADC0-IADC1 sensor input pins. A gain of 8 is enabled by setting PRE_E = 1. When disabled, the supply current of the preamplifier is < 10 nA and the gain is unity. With proper settings of the PRE_E and DIFFA_E (I/O RAM 0x210C[4]) bits, the preamplifier can be used whether or not differential mode is selected. For best performance, the differential mode is recommended. In order to save power, the bias current of the preamplifier and ADC is adjusted according to the ADC_DIV control bit (I/O RAM 0x2200[5]).

Analog-to-Digital Converter (ADC)

A single 2nd-order delta-sigma ADC digitizes the voltage and current inputs to the device. The resolution of the ADC, including the sign bit, is 21 bits (FIR_LEN[1:0] = 1), or 22 bits (FIR_LEN[1:0] = 2).

Initiation of each ADC conversion is controlled by MUX_CTRL internal circuit. At the end of each ADC conversion, the FIR filter output data is stored into the CE RAM location determined by the multiplexer selection. FIR data is stored LSB justified, but shifted left 9 bits.

FIR Filter

The finite impulse response filter is an integral part of the ADC and it is optimized for use with the multiplexer. The purpose of the FIR filter is to decimate the ADC output to the desired resolution. At the end of each ADC conversion, the output data is stored into the fixed CE RAM location determined by the multiplexer selection.

Voltage References

A bandgap circuit provides the reference voltage to the ADC. The V_{REF} band-gap amplifier is chopper-stabilized to remove the dc offset voltage. This offset voltage is the most significant long-term drift mechanism in voltage reference circuits.

Isolated Sensor Interface

Nonisolating sensors, such as shunt resistors, can be connected to the inputs of the 71M654x via a combination of a pulse transformer and a 71M6x03 isolated sensor interface. The 71M6x03 receives power directly from the 71M654xT through a pulse transformer and does not require a dedicated power supply circuit. The 71M6x03 establishes 2-way communication with the 71M654xT, supplying current samples and auxiliary information such as sensor temperature via a serial data stream.

Up to three 71M6x03 isolated sensors can be supported by the 71M6543FT/HT/GT/GHT. When a remote sensor interface is enabled, the two analog current inputs become reconfigured as a digital remote sensor interface. Each 71M6x03 isolated sensor consists of the following building blocks:

- Power supply for power pulses received from the 71M654xT
- Digital communications interface
- Shunt signal preamplifier
- Delta-sigma ADC converter with precision bandgap reference (chopping amplifier)
- Temperature sensor
- Fuse system containing part-specific information