Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

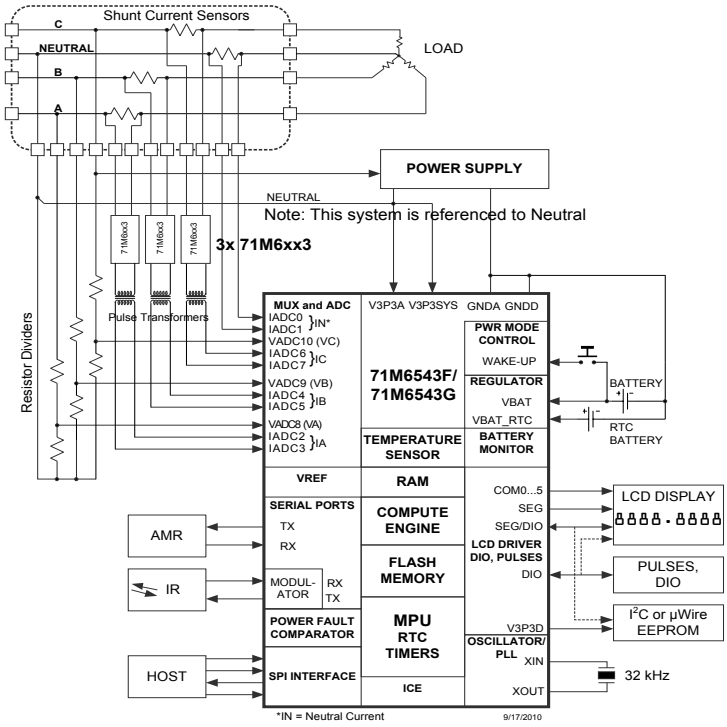
71M6543F/71M6543G Energy Meter ICs

GENERAL DESCRIPTION

The 71M6543F/71M6543G are 4th-generation polyphase metering systems-on-chips (SoCs) with a 5MHz 8051-compatible MPU core, low-power real-time clock (RTC) with digital temperature compensation, flash memory, and LCD driver. Our Single Converter Technology® with a 22-bit delta-sigma ADC, seven analog inputs, digital metrology temperature compensation, precision voltage reference, and a 32-bit computation engine (CE) supports a wide range of metering applications with very few external components.

The 71M6543F/71M6543G support optional interfaces to the 71M6xx3 series of isolated sensors that offer BOM cost reduction, immunity to magnetic tamper, and enhanced reliability. The ICs feature ultra-low-power operation in active and battery modes, 5KB shared RAM, and 64KB (71M6543F) or 128KB (71M6543G) of flash memory, which can be programmed with code and/or data during meter operation.

A complete array of code development tools, demonstration code, and reference designs enable rapid development and certification of meters that meet all ANSI and IEC electricity metering standards worldwide.



Single Converter Technology is a registered trademark of Maxim Integrated Products, Inc.
MICROWIRE is a registered trademark of National Semiconductor Corp.

FEATURES

- 0.1% Typical Accuracy Over 2000:1 Current Range
- Exceeds IEC 62053/ANSI C12.20 Standards
- Seven Sensor Inputs with Neutral Current Measurement, Differential Mode Selectable for Current Inputs
- Selectable Gain of 1 or 8 for One Current Input to Support Shunts
- High-Speed Wh/VARh Pulse Outputs with Programmable Width
- 64KB Flash, 5KB RAM (71M6543F)
- 128KB Flash, 5KB RAM (71M6543G)
- Up to Four Pulse Outputs with Pulse Count
- Four-Quadrant Metering, Phase Sequencing
- Digital Temperature Compensation:
  - Metrology Compensation
  - Accurate RTC for TOU Functions with Automatic Temperature Compensation for Crystal in All Power Modes
- Independent 32-Bit Compute Engine
- 46-64Hz Line Frequency Range with the Same Calibration
- Phase Compensation (±7°)
- Three Battery-Backup Modes:
  - Brownout Mode
  - LCD Mode
  - Sleep Mode
- Wake-Up on Pin Events and Wake-on-Timer
- 1µA in Sleep Mode
- Flash Security
- In-System Program Update
- 8-Bit MPU (80515), Up to 5MIPS
- Full-Speed MPU Clock in Brownout Mode
- LCD Driver:
  - 6 Common Segment Drivers
  - Up to 56 Selectable Pins
- Up to 51 Multifunction DIO Pins
- Hardware Watchdog Timer (WDT)
- I^2C/MICROWIRE® EEPROM Interface
- SPI Interface with Flash Program Capability
- Two UARTs for IR and AMR
- IR LED Driver with Modulation
- Industrial Temperature Range
- 100-Pin Lead-Free LQFP Package

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-5375; Rev 2; 10/13

Table of Contents

Figures

Tables

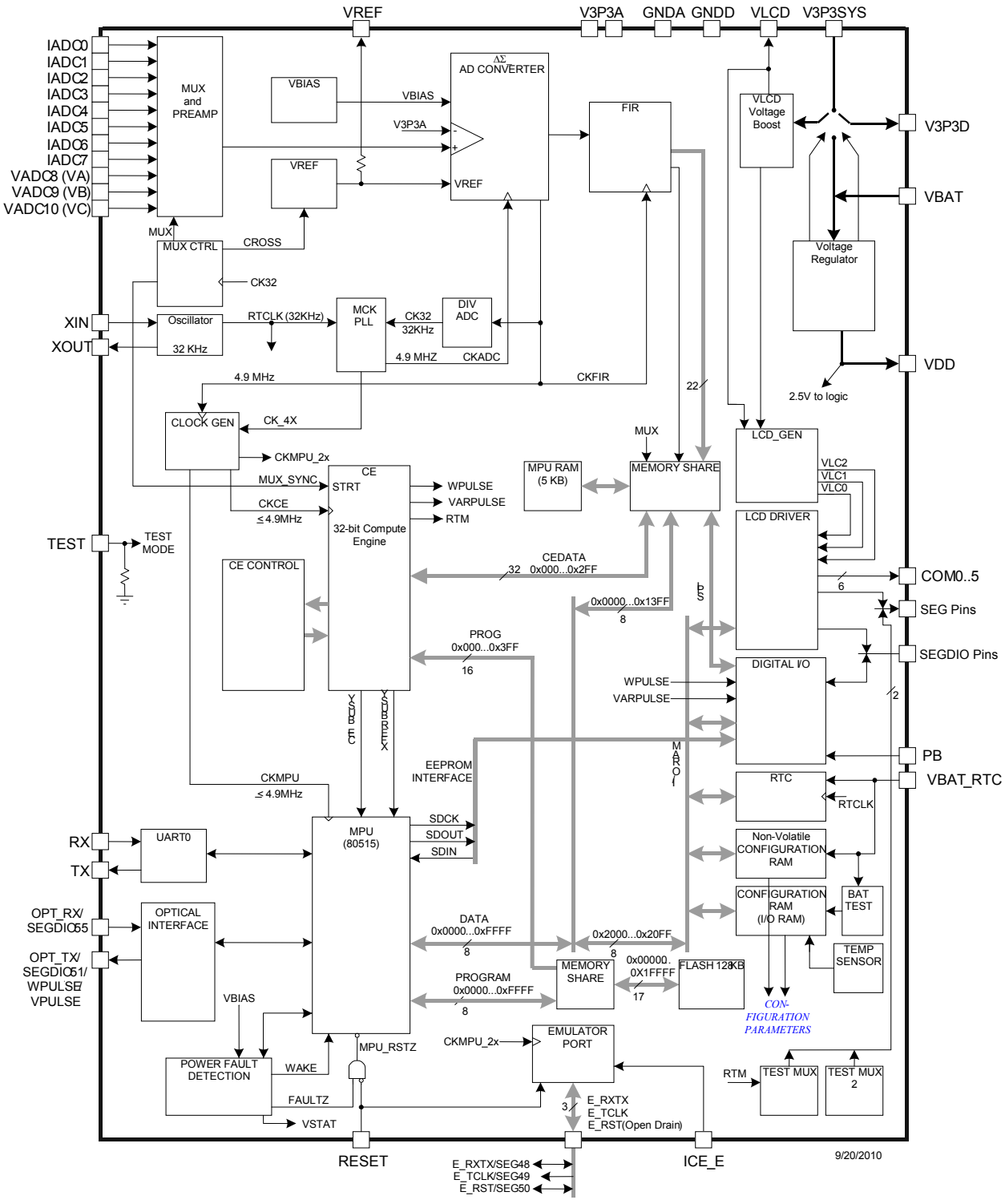


Figure 1: IC Functional Block Diagram

1 Introduction

This data sheet covers the 71M6543F (64KB) and 71M6543G (128KB) 4th-generation polyphase energy measurement system-on-chips (SoCs). The term “71M6543” is used when discussing a device feature or behavior that is applicable to all four part numbers. The specific part numbers are used when discussing those features that apply only to specific part numbers. This data sheet also covers details about the companion 71M6xx3 isolated current sensor device.

This document covers the use of the 71M6543 in conjunction with the 71M6xx3 isolated current sensor. The 71M6543 and 71M6xx3 ICs make it possible to use one non-isolated and three additional isolated shunt current sensors to create polyphase energy meters using inexpensive shunt resistors, while achieving unprecedented performance with this type of sensor technology. The 71M6543 SoCs also support Current Transformers (CT).

To facilitate document navigation, hyperlinks are often used to reference figures, tables and section headings that are located in other parts of the document. All hyperlinks in this document are highlighted in blue. Hyperlinks are used extensively to increase the level of detail and clarity provided within each section by referencing other relevant parts of the document. To further facilitate document navigation, this document is published as a PDF document with bookmarks enabled.

The reader is also encouraged to obtain and review the documents listed in 8 Related Information on page 152 of this document.

2 Hardware Description

2.1 Hardware Overview

The 71M6543 single-chip energy meter integrates all primary functional blocks required to implement a solid-state electricity meter. Included on the chip are:

- An analog front-end (AFE) featuring a 22-bit second-order sigma-delta ADC
- An independent 32-bit digital computation engine (CE) to implement DSP functions
- An 8051-compatible microprocessor (MPU) which executes one instruction per clock cycle (80515)
- A precision voltage reference (VREF)
- A temperature sensor for digital temperature compensation of:
  - Metrology (MPU)
  - Automatic RTC in all power states
  - MPU assisted RTC compensation
- LCD Driver
- RAM and Flash memory
- A real time clock (RTC)
- A variety of I/O pins
- A power failure interrupt
- A zero-crossing interrupt
- Selectable current sensor interfaces for locally-connected sensors as well as isolated sensors (i.e., using the 71M6xx3 companion IC with a shunt resistor sensor)
- Resistive Shunt and Current Transformers are supported

In order to implement a polyphase meter with or without neutral current sensing, one resistive shunt current sensor may be connected directly (non-isolated) to the 71M6543 device, while up to three additional current shunts are isolated using a companion 71M6xx3 isolated sensor IC. An inexpensive, small size pulse transformer is used to electrically isolate the 71M6xx3 remote sensor from the 71M6543. The 71M6543 performs digital communications bi-directionally with the 71M6xx3 and also provides power to the 71M6xx3 through the isolating pulse transformer. Isolated (remote) shunt current sensors are connected to the differential input of the 71M6xx3. The 71M6543 may also be used with Current Transformers; in this case the 71M6xx3 isolated sensors are not required. Included on the 71M6xx3 companion isolator chip are:

- Digital isolation communications interface
- An analog front-end (AFE) featuring a 22-bit second-order sigma-delta ADC
- A precision voltage reference (VREF)
- A temperature sensor (for current-sensing digital temperature compensation)
- A fully differential shunt resistor sensor input
- A pre-amplifier to optimize shunt current sensor performance
- Isolated power circuitry obtains dc power from pulses sent by the 71M6543

In a typical application, the 32-bit compute engine (CE) of the 71M6543 sequentially processes the samples from the voltage inputs on analog input pins and performs calculations to measure active energy (Wh) and reactive energy (VARh), as well as A^2h, and V^2h for four-quadrant metering. These measurements are then accessed by the MPU, processed further and output using the peripheral devices available to the MPU.

In addition to advanced measurement functions, the real time clock (RTC) function allows the 71M6543 to record time of use (TOU) metering information for multi-rate applications and to time-stamp tamper or other events. An automatic RTC temperature compensation circuit operates in all power states including when the MPU is halted, and continues to compensate using back-up battery power during power outages.

Measurements can be displayed on 3.3 V LCDs commonly used in low-temperature environments. The integrated charge pump and temperature sensor can be used by the MPU to enhance 3.3 V LCD performance at cold temperatures. The on-chip charge pump may also drive 5 V LCDs. Flexible mapping of LCD display segments facilitates the integration of existing custom LCDs. Design trade-off between the

number of LCD segments and DIO pins can be implemented in software to accommodate various requirements.

In addition to the temperature-trimmed ultra-precision voltage reference, the on-chip digital temperature compensation mechanism includes a temperature sensor and associated controls for correction of unwanted temperature effects on metrology and RTC accuracy (i.e., to meet the requirements of ANSI and IEC standards). Temperature-dependent external components such as the crystal oscillator, current transformers (CTs), Current Shunts and their corresponding signal conditioning circuits can be characterized and their correction factors can be programmed to produce electricity meters with exceptional accuracy over the industrial temperature range.

One of the two internal UARTs is adapted to support an Infrared LED with internal drive and sense configuration and can also function as a standard UART. The optical output can be modulated at 38 kHz. This flexibility makes it possible to implement AMR meters with an IR interface. A block diagram of the IC is shown in Figure 1.

2.2 Analog Front-End (AFE)

The AFE functions as a data acquisition system, controlled by the MPU. The 71M6543 AFE may also be augmented by isolated 71M6xx3 sensors in order to support low-cost current shunt sensors. Figure 2, and Figure 3 show the two most common configurations; other configurations are possible. Sensors that are connected directly to the 71M6543 (i.e., IADC0-IADC1, VADC8, VADC9 and VADC10) are multiplexed into the single second-order sigma-delta ADC input for sampling in the 71M6543. The 71M6543 ADC output is decimated by the FIR filter and stored in CE RAM where it can be accessed and processed by the CE.

Shunt current sensors that are isolated by using a 71M6xx3 device, are sampled by a second-order sigma delta ADC in the 71M6xx3 and the signal samples are transferred over the digital isolation interface through the low-cost isolation pulse transformer.

Figure 2 shows the 71M6543 using shunt current sensors and the 71M6xx3 isolated sensor devices. Figure 2 supports neutral current measurement with a local shunt connected to the IADC0-IADC1 input plus three remote (isolated) shunt sensors. As seen in Figure 2, when a remote isolated shunt sensor is connected via the 71M6xx3, the samples associated with this current channel are not routed to the multiplexer, and are instead transferred digitally to the 71M6543 via the isolation interface and are directly stored in CE RAM. The *MUX_SELn[3:0]* I/O RAM control fields allow the MPU to configure the AFE for the desired multiplexer sampling sequence. Refer to Table 1 and Table 2 for the appropriate CE code and the corresponding AFE settings.

See Figure 31 for the meter wiring configuration corresponding to Figure 2.

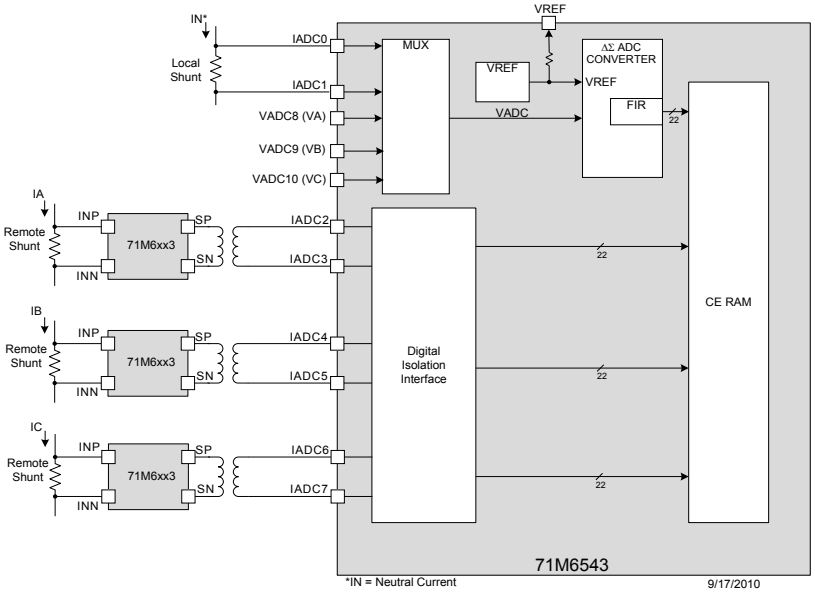


Figure 2: AFE Block Diagram (Shunts: One-Local, Three-Remotes)

The 71M6543 AFE can also be directly interfaced to Current Transformers (CTs), as seen in Figure 3. In this case, all voltage and current channels are multiplexed into a single second-order sigma-delta ADC in the 71M6543 and the 71M6xx3 remote isolated sensors are not used. The fourth CT and the measurement of Neutral current via the IADC0-IADC1 current channel are optional.

See Figure 32 for the meter wiring configuration corresponding to Figure 3.

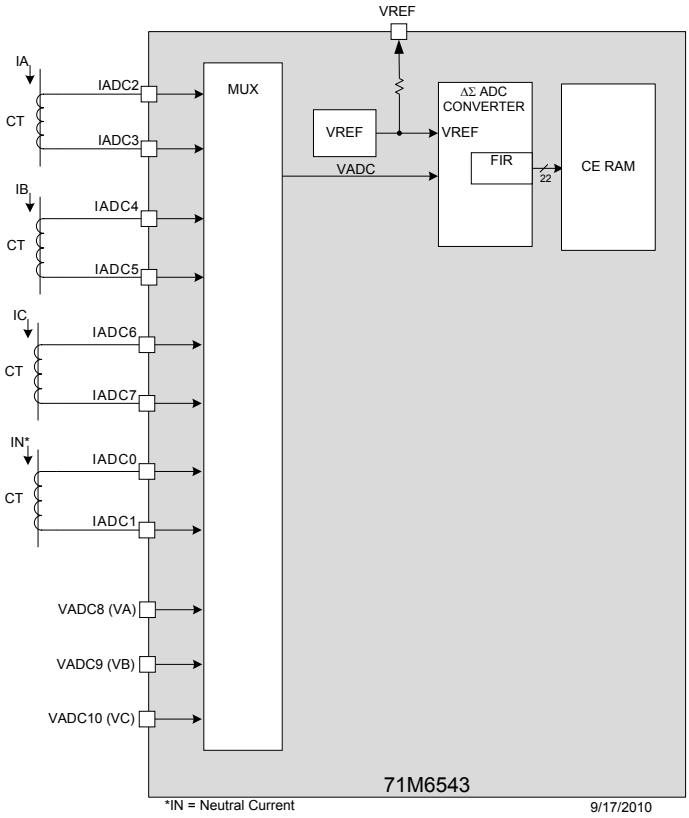


Figure 3. AFE Block Diagram (Four CTs)

2.2.1 Signal Input Pins

The 71M6543 features eleven ADC input pins.

IADC0 through IADC7 are intended for use as current sensor inputs. These eight current sensor inputs can be configured as four single-ended inputs, or can be paired to form four differential inputs. For best performance, it is recommended to configure the current sensor inputs as differential inputs (i.e., IADC0-IADC1, IADC2-IADC3, IADC4-IADC5 and IADC6-IADC7). The first differential input (IADC0-IADC1) features a pre-amplifier with a selectable gain of 1 or 8, and is intended for direct connection to a shunt resistor sensor, and can also be used with a Current Transformer (CT). The three remaining differential pairs (i.e., IADC2-IADC3, IADC4-IADC5 and IADC6-IADC7) may be used with CTs, or may be enabled to interface to a remote 71M6xx3 isolated current sensor providing isolation for a shunt resistor sensor using a low cost pulse transformer.

The remaining three inputs VADC8 (VA), VADC9 (VB) and VADC10 (VC) are single-ended, and are intended for sensing each of the phase voltages in a polyphase meter application. These three single-ended inputs are referenced to the V3P3A pin.

All ADC input pins measure voltage. In the case of shunt current sensors, currents are sensed as a voltage drop in the shunt resistor sensor. In the case of Current Transformers (CT), the current is measured as a voltage across a burden resistor that is connected to the secondary of the CT. Meanwhile, line voltages are sensed through resistive voltage dividers. The VADC8 (VA), VADC9 (VB) and VADC10 (VC) pins are single-ended and their common return is the V3P3A pin. See Figure 27, Figure 28, Figure 29 and Figure 30 for detailed connections for each type of sensor. Also refer to the 71M6543 Demonstration Board schematic and bill of materials for typical component values used in these and other circuits.

Pins IADC0-IADC1 can be programmed individually to be differential or single-ended as determined by the *DIFF0_E* (*I/O RAM 0x210C[4]*) control bit. However, for most applications, IADC0-IADC1 are configured as a differential input to work with a resistive shunt or CT directly interfaced to the IADC0-IADC1 differential input with the appropriate external signal conditioning components.

The performance of the IADC0-IADC1 pins can be enhanced by enabling a pre-amplifier with a fixed gain of 8, using the I/O RAM control bit *PRE_E (I/O RAM 0x2704[5])*. When *PRE_E* = 1, IADC0-IADC1 become the inputs to the 8x pre-amplifier, and the output of this amplifier is supplied to the multiplexer. The 8x amplification is useful when current sensors with low sensitivity, such as shunt resistors, are used. With *PRE_E* set, the IADC0-IADC1 input signal amplitude is restricted to 31.25 mV peak. When *PRE_E* = 0 (Gain = 1), the IADC0-IADC1 input signal is restricted to 250 mV peak.

For the 71M6543 application utilizing shunt resistor sensors (Figure 2), the IADC0-IADC1 pins are configured for differential mode to interface to a local shunt by setting the *DIFF0_E* control bit. Meanwhile, the IADC2-IADC3 , IADC4-IADC5 and IADC6-IADC7 pins are re-configured as digital remote sensor interface designed to communicate with a 71M6xx3 isolated sensor by setting the *RMTx_E* control bits (*I/O RAM 0x2709[5:3]*). The 71M6xx3 communicates with the 71M6543 using a bi-directional digital data stream through an isolating pulse transformer. The 71M6543 also supplies power to the 71M6xx3 through the isolating transformer. This type of interface is further described at the end of this chapter. See 2.2.8 71M6xx3 Isolated Sensor Interface.

For use with Current Transformers (CTs), as shown in Figure 3, the *RMTx_E* control bits are reset, so that IADC2-IADC3, IADC4-IADC5 and IADC6-IADC7 are configured as local analog inputs. The IADC0-IADC1 pins cannot be configured as a remote sensor interface.

2.2.2 Input Multiplexer

When operating with locally connected sensors, the input multiplexer sequentially applies the input signals from the analog input pins to the input of the ADC (see Figure 3), according to the sampling sequence determined by the eleven *MUXn_SEL[3:0]* control fields. One complete sampling sequence is called a multiplexer frame. The multiplexer of the 71M6543 can select up to eleven input signals when the current sensor inputs are configured for single-ended mode. When the current sensor inputs are configured in differential mode (recommended for best performance), the number of input signals is seven (i.e., IADC0-IADC1, IADC2-IADC3, IADC4-IADC5, IADC6-IADC7, VADC8, VADC9 and VADC10) per multiplexer frame. The number of slots in the multiplexer frame is controlled by the I/O RAM control field *MUX_DIV[3:0] (I/O RAM 0x2100[7:4])* (see Figure 4). The multiplexer always starts at state 0 and proceeds until the number of sensor channels determined by the *MUX_DIV[3:0]* field setting have been converted.

The 71M6543 requires a unique CE code that is written for the specific meter configuration. Moreover, each CE code requires specific AFE and MUX settings in order to function properly. Table 1 provides the CE code and settings corresponding to the 1-Local / 3-Remote sensor configuration shown in Figure 2. Table 2 provides the CE code and settings corresponding to the CT configuration shown in Figure 3.

Table 1. Required CE Code and Settings for 1-Local / 3-Remotes

I/O RAM Mnemonic	I/O RAM Location	I/O RAM Setting	Comments
FIR_LEN[1:0]	210C[2:1]	1	288 cycles
ADC_DIV	2200[5]	0	Fast
PLL_FAST	2200[4]	1	19.66 MHz
MUX_DIV[3:0]	2100[7:4]	6	See note 1
MUX0_SEL[3:0]	2105[3:0]	0	Slot 0 is IADC**0**-IADC1 (IN)
MUX1_SEL[3:0]	2105[7:4]	1	Unused (See note 2)
MUX2_SEL[3:0]	2104[3:0]	1	Unused (See note 2)
MUX3_SEL[3:0]	2104[7:4]	8	Slot 3 is VADC**8** (VA)
MUX4_SEL[3:0]	2103[3:0]	9	Slot 4 is VADC**9** (VB)
MUX5_SEL[3:0]	2103[7:4]	A	Slot 5 is VADC**10** (VC)
MUX6_SEL[3:0]	2102[3:0]	0	Slots not enabled
MUX7_SEL[3:0]	2102[7:4]	0	
MUX8_SEL[3:0]	2101[3:0]	0	
MUX9_SEL[3:0]	2101[7:4]	0	
MUX10_SEL[3:0]	2100[3:0]	0	
RMT2_E	2709[3]	1	Enable Remote IADC2-IADC3 (IA)
RMT4_E	2709[4]	1	Enable Remote IADC4-IADC5 (IB)
RMT6_E	2709[5]	1	Enable Remote IADC6-IADC7 (IC)
DIFF0_E	210C[4]	1	Differential IADC0-IADC1 (IN)
DIFF2_E	210C[5]	0	See note 3
DIFF4_E	210C[6]	0	See note 3
DIFF6_E	210C[7]	0	See note 3
PRE_E	2704[5]	1	IADC0-IADC1 Gain = 8
EQU[2:0]	2106[7:5]	5	IA*VA + IB*VB + IC*VC
CE Codes (See note 4)	ce43b016603 (use with 71M6603) ce43b016103 (use with 71M6103) ce43b016113 (use with 71M6113) ce43b016203 (use with 71M6203)		
Equation(s)	5		
Current Sensor Type	1 Local Shunt and 3 Remote Shunts		
Applicable Figures	Figure 2, Figure 4 and Figure 31		

Notes:

1. *MUX_DIV[3:0]* must be set to 0 while writing the other RAM locations in this table.
2. Each unused slot must be assigned to a valid (0 to A), but unused ADC handle.
3. This channel is remote (71M6xx3), hence *DIFFx_E* is irrelevant.
4. Must use the CE code that corresponds to the specific 71M6xx3 device used.

Maxim updates the CE code periodically. Contact your local Maxim representative to obtain the latest CE code and the associated settings.

Table 2. Required CE Code and Settings for CT Sensors

I/O RAM Mnemonic	I/O RAM Location	I/O RAM Setting (Hex)	Comments
FIR_LEN[1:0]	210C[2:1]	1	288 cycles
ADC_DIV	2200[5]	0	Fast
PLL_FAST	2200[4]	1	19.66 MHz
MUX_DIV[3:0]	2100[7:4]	7	See note 1
MUX0_SEL[3:0]	2105[3:0]	2	Slot 0 is IADC**2**-IADC3 (IA)
MUX1_SEL[3:0]	2105[7:4]	8	Slot 1 is VADC**8** (VA)
MUX2_SEL[3:0]	2104[3:0]	4	Slot 2 is IADC**4**-IADC5 (IB)
MUX3_SEL[3:0]	2104[7:4]	9	Slot 3 is VADC**9** (VB)
MUX4_SEL[3:0]	2103[3:0]	6	Slot 4 is IADC**6**-IADC7 (IC)
MUX5_SEL[3:0]	2103[7:4]	A	Slot 5 is VADC**10** (VC)
MUX6_SEL[3:0]	2102[3:0]	0	Slot 6 is IADC0-IADC1 (IN – See note 2)
MUX7_SEL[3:0]	2102[7:4]	0	Slots not enabled
MUX8_SEL[3:0]	2101[3:0]	0	
MUX9_SEL[3:0]	2101[7:4]	0	
MUX10_SEL[3:0]	2100[3:0]	0	
RMT2_E	2709[3]	0	Local Sensor IADC2-IADC3
RMT4_E	2709[4]	0	Local Sensor IADC4-IADC5
RMT6_E	2709[5]	0	Local Sensor IADC6-IADC7
DIFF0_E	210C[4]	1	Differential IADC0-IADC1
DIFF2_E	210C[5]	1	Differential IADC2-IADC3
DIFF4_E	210C[6]	1	Differential IADC4-IADC5
DIFF6_E	210C[7]	1	Differential IADC6-IADC7
PRE_E	2704[5]	0	IADC0-IADC1 Gain = 1
EQU[2:0]	2106[7:5]	5	IA*VA + IB*VB + IC*VC
CE Code	ce43a02		
Equation(s)	5		
Current Sensor Type	4 Current Transformers (CTs)		
Applicable Figures	Figure 3, Figure 4 and Figure 32		

Notes:

1. *MUX_DIV[3:0]* must be set to 0 while writing the other RAM locations in this table.
2. IN is the optional Neutral Current.

Maxim updates the CE code periodically. Contact your local Maxim representative to obtain the latest CE code and the associated settings.

Using settings for the I/O RAM Mnemonics listed in Table 1 and Table 2 that do not match those required by the corresponding CE code being used may result in undesirable side effects and must not be selected by the MPU. Consult your local Maxim representative to obtain the correct CE code and AFE / MUX settings corresponding to the application.

For a polyphase configuration with neutral current sensing using shunt resistor current sensors and the 71M6xx3 isolated sensors, as shown in Figure 2, the IADC0-IADC1 input must be configured as a differential input, to be connected to a local shunt (see Figure 30 for the shunt connection details). The local shunt connected to the IADC0-IADC1 input is used to sense the Neutral current. The voltage sensors (VADC8, VADC9 and VADC10) are also directly connected to the 71M6543 (see Figure 27 for the connection details) and are also routed though the multiplexer, as seen in Figure 2. Meanwhile, the IADC2-IADC3, IADC4-IADC5 and IADC6-IADC7 current inputs are configured as remote sensor digital interfaces and the corresponding samples are not routed through the multiplexer. For this configuration, the multiplexer sequence is as shown in Figure 4.

For a polyphase configuration with optional neutral current sensing using Current Transformer (CTs) sensors, as shown in Figure 3, all four current sensor inputs must be configured as a differential inputs, to be connected to their corresponding CTs (see Figure 29 for the differential CT connection details). The IADC0-IADC1 current sensor input is optionally used to sense the Neutral current for anti-tampering purposes. The voltage sensors (VADC8, VADC9 and VADC10) are directly connected to the 71M6543 (see Figure 27 for the voltage sensor connection details). No 71M6xx3 isolated sensors are used in this configuration and all sensors are routed though the multiplexer, as seen in Figure 3. For this configuration, the multiplexer sequence is as shown in Figure 5.

The multiplexer sequence shown in Figure 4 corresponds to the configuration shown in Figure 2. The frame duration is 13 CK32 cycles (where CK32 = 32,768 Hz), therefore, the resulting sample rate is 32,768 Hz / 13 = 2,520.6 Hz. Note that Figure 4 only shows the currents that pass through the 71M6543 multiplexer, and does not show the currents that are copied directly into CE RAM from the remote sensors (see Figure 2), which are sampled during the second half of the multiplexer frame. The two unused conversion slots shown are necessary to produce the desired 2,520.6 Hz sample rate.

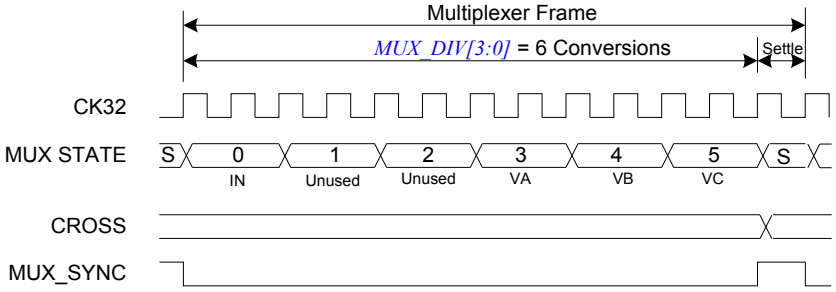


Figure 4: States in a Multiplexer Frame (*MUX_DIV[3:0]* = 6)

The multiplexer sequence shown in Figure 5 corresponds to the CT configuration shown in Figure 3. Since in this case all current sensors are locally connected to the 71M6543, all currents are routed through the multiplexer, as seen in Figure 3. For this multiplexer sequence, the frame duration is 15 CK32 cycles (where CK32 = 32,768 Hz), therefore, the resulting sample rate is 32,768 Hz / 15 = 2,184.5 Hz.

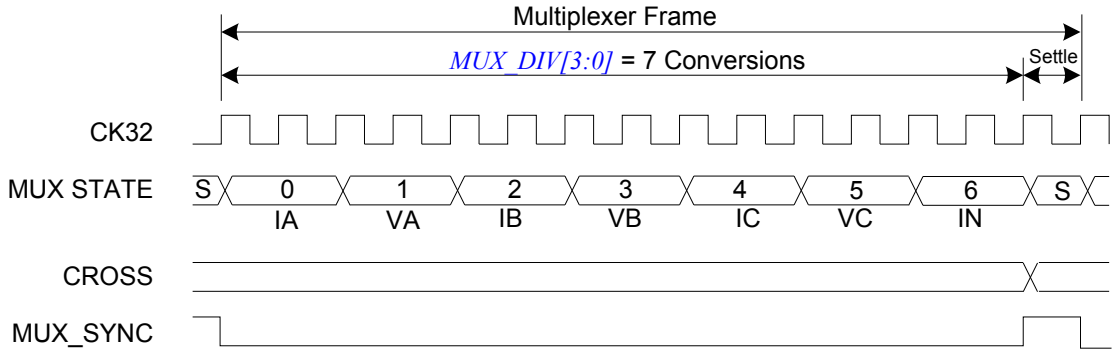


Figure 5: States in a Multiplexer Frame (*MUX_DIV[3:0]* = 7)

Multiplexer advance, FIR initiation and chopping of the ADC reference voltage (using the internal CROSS signal, see 2.2.7 Voltage References) are controlled by the internal MUX_CTRL circuit. Additionally, MUX_CTRL launches each pass of the CE through its code. MUX_CTRL is clocked by CK32, the 32768 Hz clock from the PLL block. The behavior of the MUX_CTRL circuit is governed by:

- *CHOP_E[1:0]* (*I/O RAM 0x2106[3:2]*)
- *MUX_DIV[3:0]* (*I/O RAM 0x2100[7:4]*)
- *FIR_LEN[1:0]* (*I/O RAM 0x210C[2:1]*)
- *ADC_DIV* (*I/O RAM 0x2200[5]*)

The duration of each multiplexer state depends on the number of ADC samples processed by the FIR as determined by the *FIR_LEN[1:0] (I/O RAM 0x210C[2:1]* control field. Each multiplexer state starts on the rising edge of CK32, the 32-kHz clock.

It is required that *MUX_DIV[3:0] (I/O RAM 0x2100[7:4])* be set to zero while changing the ADC configuration to minimize system transients. After all configuration bits are set, *MUX_DIV[3:0]* should be set to the required value.

The duration of each time slot in CK32 cycles depends on *FIR_LEN[1:0], ADC_DIV* and *PLL_FAST*:

Time_Slot_Duration = (3-2**PLL_FAST*)*(*FIR_LEN[1:0]*+1) * (*ADC_DIV*+1)

The duration of a multiplexer frame in CK32 cycles is:

MUX_Frame_Duration = 3-2**PLL_FAST* + Time_Slot_Duration * *MUX_DIV[3:0]*

The duration of a multiplexer frame in CK_FIR cycles is:

MUX frame duration (CK_FIR cycles) =

[3-2**PLL_FAST* + Time_Slot_Duration * *MUX_DIV*] * (48+*PLL_FAST**102)

The ADC conversion sequence is programmable through the *MUXn_SEL* control fields (*I/O RAM 0x2100* to *0x2105*). As stated above, there are up to eleven ADC time slots in the 71M6543, as set by *MUX_DIV[3:0]* (*I/O RAM 0x2100[7:4]*). In the expression *MUXn_SEL[3:0]* = x, 'n' refers to the multiplexer frame time slot number and 'x' refers to the desired ADC input number or ADC handle (i.e., IADC0 to VADC10, or simply 0 to 10 decimal). Thus, there are a total of 11 valid ADC handles in the 71M6543 devices. For example, if *MUX0_SEL[3:0]* = 0, then IADC0, corresponding to the sample from the IADC0-IADC1 input (configured as a differential input), is positioned in the multiplexer frame during time slot 0. See Table 1 and Table 2 for the appropriate *MUXn_SEL[3:0]* settings and other settings applicable to a particular meter configuration and CE code.

Note that when the remote sensor interface is enabled, the samples corresponding to the remote sensor currents do not pass through the 71M6543 multiplexer. The sampling of the remote current sensors occurs in the second half of the multiplexer frame. The VA, VB and VC voltages are assigned the last three slots in the frame. With this slot assignment for VA, VB and VC, the sampling of the corresponding remote sensor currents bears a precise timing relationship to their corresponding phase voltages, and delay compensation is accurately performed (see 2.2.3 Delay Compensation on page 19).

Also when using remote sensors, it is necessary to introduce unused slots to realize the number of slots specified by the *MUX_DIV[3:0]* (*I/O RAM 0x2100[7:4]*) field setting (see Figure 4 and Figure 5). The *MUXn_SEL[3:0]* control fields for these unused ("dummy") slots must be written with a valid ADC handle (i.e., 0 to 10 decimal) that is not otherwise being used. In this manner, the unused ADC handle, is used as a "dummy" place holder in the multiplexer frame, and the correct duration multiplexer frame sequence is generated and also the desired sample rate. The resulting sample data stored in the CE RAM location corresponding to the "dummy" ADC handle is ignored by the CE code. Meanwhile, the digital isolation interface takes care of automatically storing the samples for the remote current sensors in the appropriate CE RAM locations.

Delay compensation and other functions in the CE code require the settings for *MUX_DIV[3:0], MUXn_SEL[3:0], RMT_E, FIR_LEN[1:0], ADC_DIV* and *PLL_FAST* to be fixed for a given CE code. Refer to Table 1 and Table 2 for the settings that are applicable to the 71M6543.

Table 3 summarizes the I/O RAM registers used for configuring the multiplexer, signals pins, and ADC. All listed registers are 0 after reset and wake from battery modes, and are readable and writable.

Table 3: Multiplexer and ADC Configuration Bits

Name	Location	Description
MUX0_SEL[3:0]	2105[3:0]	Selects the ADC input converted during time slot 0.
MUX1_SEL[3:0]	2105[7:4]	Selects the ADC input converted during time slot 1.
MUX2_SEL[3:0]	2104[3:0]	Selects the ADC input converted during time slot 2.
MUX3_SEL[3:0]	2104[7:4]	Selects the ADC input converted during time slot 3.
MUX4_SEL[3:0]	2103[3:0]	Selects the ADC input converted during time slot 4.
MUX5_SEL[3:0]	2103[7:4]	Selects the ADC input converted during time slot 5.
MUX6_SEL[3:0]	2102[3:0]	Selects the ADC input converted during time slot 6.
MUX7_SEL[3:0]	2102[7:0]	Selects the ADC input converted during time slot 7.
MUX8_SEL[3:0]	2101[3:0]	Selects the ADC input converted during time slot 8.
MUX9_SEL[3:0]	2101[7:0]	Selects the ADC input converted during time slot 9.
MUX10_SEL[3:0]	2100[3:0]	Selects the ADC input converted during time slot 10.
ADC_DIV	2200[5]	Controls the rate of the ADC and FIR clocks.
MUX_DIV[3:0]	2100[7:4]	The number of ADC time slots in each multiplexer frame (maximum = 11).
PLL_FAST	2200[4]	Controls the speed of the PLL and MCK.
FIR_LEN[1:0]	210C[2:1]	Determines the number of ADC cycles in the ADC decimation FIR filter.
DIFF0_E	210C[4]	Enables the differential configuration for analog input pins IADC0-IADC1 .
DIFF2_E	210C[5]	Enables the differential configuration for analog input pins IADC2-IADC3 .
DIFF4_E	210C[6]	Enables the differential configuration for analog input pins IADC4-IADC5 .
DIFF6_E	210C[7]	Enables the differential configuration for analog input pins IADC6-IADC7 .
RMT2_E	2709[3]	Enables the remote sensor interface transforming pins IADC2-IADC3 into a digital interface for communications with a 71M6xx3 sensor.
RMT4_E	2709[4]	Enables the remote sensor interface transforming pins IADC4-IADC5 into a digital interface for communications with a 71M6xx3 sensor.
RMT6_E	2709[5]	Enables the remote sensor interface transforming pins IADC6-IADC7 into a digital interface for communications with a 71M6xx3 sensor.
PRE_E	2704[5]	Enables the 8x pre-amplifier.
Refer to Table 70 starting on page 102 for more complete details about these I/O RAM locations.		

2.2.3 Delay Compensation

When measuring the energy of a phase (i.e., Wh and VARh) in a service, the voltage and current for that phase must be sampled at the same instant. Otherwise, the phase difference, Φ, introduces errors.

$$\phi = \frac{t_{delay}}{T} \cdot 360^o = t_{delay} \cdot f \cdot 360^o$$

Where *f* is the frequency of the input signal, T = 1/f and t_{delay} is the sampling delay between current and voltage.

Traditionally, sampling is accomplished by using two A/D converters per phase (one for voltage and the other one for current) controlled to sample simultaneously. Maxim's Single Converter Technology, however, exploits the 32-bit signal processing capability of its CE to implement "constant delay" all-pass filters. The all-pass filter corrects for the conversion time difference between the voltage and the corresponding current samples that are obtained with a single multiplexed A/D converter.

The "constant delay" all-pass filter provides a broad-band delay 360^o - θ, which is precisely matched to the difference in sample time between the voltage and the current of a given phase. This digital filter does not affect the amplitude of the signal, but provides a precisely controlled phase response.

The recommended ADC multiplexer sequence samples the current first, immediately followed by sampling of the corresponding phase voltage, thus the voltage is delayed by a phase angle Φ relative to the current. The delay compensation implemented in the CE aligns the voltage samples with their corresponding current samples by first delaying the current samples by one full sample interval (i.e., 360^{o}), then routing the voltage samples through the all-pass filter, thus delaying the voltage samples by 360^{o} - θ, resulting in the residual phase error between the current and its corresponding voltage of θ – Φ. The residual phase error is negligible, and is typically less than ±1.5 milli-degrees at 100Hz, thus it does not contribute to errors in the energy measurements.

When using remote sensors, the CE performs the same delay compensation described above to align each voltage sample with its corresponding current sample. Even though the remote current samples do not pass through the 71M6543 multiplexer, their timing relationship to their corresponding voltages is fixed and precisely known, provided that the *MUXn_SEL[3:0]* slot assignment fields are programmed as shown in Table 1. Note that these slot assignments result in VA, VB and VC occupying multiplexer slots 3, 4 and 5, respectively (see Figure 4).

2.2.4 ADC Pre-Amplifier

The ADC pre-amplifier is a low-noise differential amplifier with a fixed gain of 8 available only on the IADC0-IADC1 sensor input pins. A gain of 8 is enabled by setting *PRE_E* = 1 (*I/O RAM 0x2704[5]*). When disabled, the supply current of the pre-amplifier is <10 nA and the gain is unity. With proper settings of the *PRE_E* and *DIFF0_E* (*I/O RAM 0x210C[4]*) bits, the pre-amplifier can be used whether differential mode is selected or not. For best performance, the differential mode is recommended. In order to save power, the bias current of the pre-amplifier and ADC is adjusted according to the *ADC_DIV* control bit (*I/O RAM 0x2200[5]*).

2.2.5 A/D Converter (ADC)

A single 2^{nd} order sigma-delta A/D converter digitizes the voltage and current inputs to the device. The resolution of the ADC, including the sign bit, is 21 bits (*FIR_LEN[1:0]* = 01, *I/O RAM 0x210C[2:1]*), or 22 bits (*FIR_LEN[1:0]* = 10). The ADC is clocked by CKADC.

Initiation of each ADC conversion is controlled by the internal MUX_CTRL circuit as described earlier. At the end of each ADC conversion, the FIR filter output data is stored into the CE RAM location determined by the multiplexer selection.

2.2.6 FIR Filter

The finite impulse response filter is an integral part of the ADC and it is optimized for use with the multiplexer. The purpose of the FIR filter is to decimate the ADC output to the desired resolution. At the end of each ADC conversion, the output data is stored into the fixed CE RAM location determined by the multiplexer selection stored in the *MUXn_SEL[3:0]* fields. FIR data is stored after being shifted left by 9 bits.

2.2.7 Voltage References

A bandgap circuit provides the reference voltage to the ADC. The amplifier within the reference is chopper stabilized, i.e., the chopper circuit can be enabled or disabled by the MPU using the I/O RAM control field *CHOP_E[1:0] (I/O RAM 0x2106[3:2])*. The two bits in the *CHOP_E[1:0]* field enable the MPU to operate the chopper circuit in regular or inverted operation, or in toggling modes (recommended). When the chopper circuit is toggled in between multiplexer cycles, dc offsets on VREF are automatically be averaged out, therefore the chopper circuit should always be configured for one of the toggling modes.

Since the VREF band-gap amplifier is chopper-stabilized, the dc offset voltage, which is the most significant long-term drift mechanism in the voltage references (VREF), is automatically removed by the chopper circuit. Both the 71M6543 and the 71M6xx3 feature chopper circuits for their respective VREF voltage reference.

The general topology of a chopped amplifier is shown in Figure 6. The CROSS signal is an internal on-chip signal and is not accessible on any pin or register.

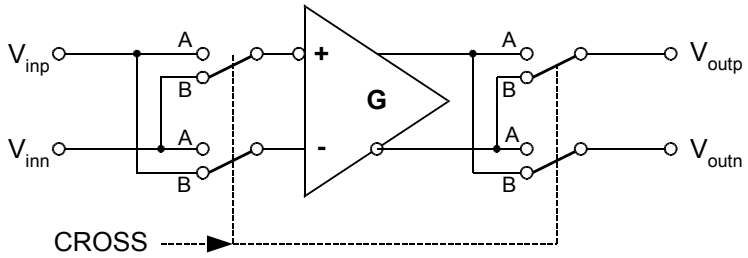


Figure 6: General Topology of a Chopped Amplifier

It is assumed that an offset voltage Voff appears at the positive amplifier input. With all switches, as controlled by CROSS (an internal signal), in the A position, the output voltage is:

Voutp – Voutn = G (Vinp + Voff – Vinn) = G (Vinp – Vinn) + G Voff

With all switches set to the B position by applying the inverted CROSS signal, the output voltage is:

Voutn – Voutp = G (Vinn – Vinp + Voff) = G (Vinn – Vinp) + G Voff, or
Voutp – Voutn = G (Vinp – Vinn) - G Voff

Thus, when CROSS is toggled, e.g., after each multiplexer cycle, the offset alternately appears on the output as positive and negative, which results in the offset effectively being eliminated, regardless of its polarity or magnitude.

When CROSS is high, the connection of the amplifier input devices is reversed. This preserves the overall polarity of that amplifier gain; it inverts its input offset. By alternately reversing the connection, the amplifier's offset is averaged to zero. This removes the most significant long-term drift mechanism in the voltage reference. The *CHOP_E[1:0]* (*I/O RAM 0x2106[3:2]*) control field controls the behavior of CROSS. On the first CK32 rising edge after the last multiplexer state of its sequence, the multiplexer waits one additional CK32 cycle before beginning a new frame. At the beginning of this cycle, the value of CROSS is updated according to the *CHOP_E[1:0]* field. The extra CK32 cycle allows time for the chopped VREF to settle. During this cycle, MUXSYNC is held high. The leading edge of MUXSYNC initiates a pass through the CE program sequence.

CHOP_E[1:0] has four states: positive, reverse, and two toggle states. In the positive state, *CHOP_E[1:0]* = 01, CROSS is held low. In the reverse state, *CHOP_E[1:0]* = 10, CROSS is held high. The two automatic toggling states are selected by setting CHOP_E=11 or CHOP_E=00.

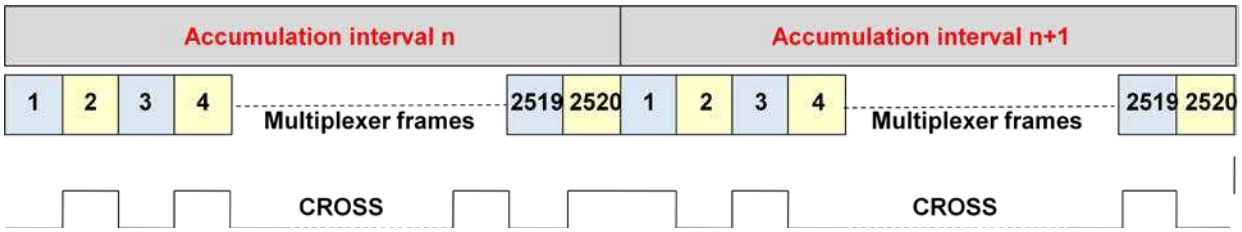


Figure 7: CROSS Signal with *CHOP_E* = 00

Figure 7 shows CROSS over two accumulation intervals when *CHOP_E[1:0]* = 00: At the end of the first interval, CROSS is high, at the end of the second interval, CROSS is low. Operation with *CHOP_E[1:0]* = 00 does not require control of the chopping mechanism by the MPU.

In the second toggle state, *CHOP_E[1:0]* = 11, CROSS does not toggle at the end of the last multiplexer cycle in an accumulation interval.

2.2.8 71M6xx3 Isolated Sensor Interface

2.2.8.1 General Description

Non-isolating sensors, such as shunt resistors, can be connected to the inputs of the 71M6543 via a combination of a pulse transformer and a 71M6xx3 IC (a top-level block diagram of this sensor interface is shown in Figure 31). The 71M6xx3 receives power directly from the 71M6543 via a pulse transformer and does not require a dedicated power supply circuit. The 71M6xx3 establishes 2-way communication with the 71M6543, supplying current samples and auxiliary information such as sensor temperature via a serial data stream.

Up to three 71M6xx3 Isolated Sensors can be supported by the 71M6543. When a remote sensor interface is enabled, the two analog current inputs become re-configured as a digital remote sensor interface. For example, when control bit *RMT2_E* = 1, the IADC2-IADC3 analog pins are re-configured as the digital interface pins to the remote sensor.

Each 71M6xx3 Isolated Sensor consists of the following building blocks:

- Power supply that derives power from pulses received from the 71M6543
- Bi-directional digital communications interface
- Shunt signal pre-amplifier
- 22-bit 2nd Order Sigma-Delta ADC Converter with precision bandgap reference (chopping amplifier)
- Temperature sensor (for digitally compensating VREF)
- Fuse system containing part-specific information

During an ordinary multiplexer cycle, the 71M6543 internally determines which other channels are enabled with *MUX_DIV[3:0] (I/O RAM 0x2100[7:4])*. At the same time, it decimates the modulator output from the 71M6xx3 Isolated Sensors. Each result is written to CE RAM during one of its CE access time slots.

2.2.8.2 Communication between 71M6543 and 71M6xx3 Isolated Sensor

The ADC of the 71M6xx3 derives its timing from the power pulses generated by the 71M6543 and as a result, operates its ADC slaved to the frequency of the power pulses. The generation of power pulses, as well as the communication protocol between the 71M6543 and 71M6xx3 Isolated Sensor, is automatic and transparent to the user. Details are not covered in this data sheet.

2.2.8.3 Control of the 71M6xx3 Isolated Sensor

The 71M6543 can read or write certain types of information from each 71M6xx3 remote sensor.

The data to be read is selected by a combination of the *RCMD[4:0]* and *TMUXRn[2:0]*. To perform a read transaction from one of the 71M6xx3 devices, the MPU first writes the *TMUXRn[2:0]* field (where n = 2, 4, 6, located at *I/O RAM 0x270A[2:0], 0x270A[6:4] and 0x2709[2:0],* respectively). Next, the MPU writes *RCMD[4:0]* (*SFR 0xFC[4:0]*) with the desired command and phase selection. When the *RCMD[4:2]* bits have cleared to zero, the transaction has been completed and the requested data is available in *RMT_RD[15:0]* (*I/O RAM 0x2602[7:0]* is the MSB and *0x2603[7:0]* is the LSB). The read parity error bit, *PERR_RD (SFR 0xFC[6])* is also updated during the transaction. If the MPU writes to *RCMD[4:0]* before a previously initiated read transaction is completed, the command is ignored. Therefore, the MPU must wait for *RCMD[4:2]*=0 before proceeding to issue the next remote sensor read command.

If the CE is running (*CE_E*=1), the MPU must write *RCMD[4:0]* immediately after a CE_BUSY rising edge. *RCMD[4:0]* must be written before the next rising edge of MUX_SYNC. Failure to do this can cause incorrect data to be read.

The *RCMD[4:0]* field is divided into two sub-fields, *COMMAND=RCMD[4:2]* and *PHASE=RCMD[1:0]*, as shown in Table 4.

.

Table 4. *RCMD[4:0]* Bits

Command *RCMD[4:2]*		**Phase Selector** *RCMD[1:0]*		**Associated** *TMUXRn* **Control Field**
000	Invalid	00	Invalid	---
001	Command 1	01	IADC**2**-IADC3	*TMUXR**2**[2:0]*
010	Command 2	10	IADC**4**-IADC5	*TMUXR**4**[2:0]*
011	Reserved	11	IADC**6**-IADC7	*TMUXR**6**[2:0]*
100	Reserved			
101	Invalid			
110	Reserved			
111	Reserved			

Notes:
1. Only two codes of *RCMD[4:2]* (*SFR 0xFC[4:2]*) are relevant for normal operation. These are *RCMD[4:2]* = 001 and 010. Codes 000 and 101 are invalid and will be ignored if used. The remaining codes are reserved and must not be used.
2. For the *RCMD[1:0]* control field, codes 01, 10 and 11 are valid and 00 is invalid and must not be used.
3. The specific phase (A, B or C) associated with each *TMUXRn[2:0]* field, is determined by how the IADCn input pins are connected in the meter design.

Table 5 shows the allowable combinations of values in *RCMD[4:2]* and *TMUXRn[2:0]*, and the corresponding data type and format sent back by the 71M6xx3 remote sensor and how the data is stored in *RMT_RD[15:8]* and *RMT_RD[7:0]*. The MPU selects which of the three phases is read by asserting the proper code in the *RCMD[1:0]* field, as shown in Table 4.

.

Table 5: Remote Interface Read Commands

RCMD[4:2]	***TMUXRn[2:0]***	**Read Operation**	***RMT_RD* [15:8]**	***RMT_RD* [7:0]**
001	00X	*TRIMT[7:0]* (trim fuse for all 71M6xx3)	*TRIMT[7]=RMT_RD[8]*	*TRIMT[6:0]=RMT_RD[7:1]*
001	11X	*TRIMBGB[7:0]* and *TRIMBGD[7:0]* (additional trim fuses for 71M6113 and 71M6203 only)	*TRIMBGB[7:0]*	*TRIMBGD[7:0]*
010	00X	*STEMP[10:0]* (sensed 71M6xx3 temperature)	*STEMP[10:8]=RMT_RD[10:8]* *(RMT_RD[15:11] are sign extended)*	*STEMP[7:0]*
010	01X	*VSENSE[7:0]* (sensed 71M6xx3 supply voltage)	*All zeros*	*VSENSE[7:0]*
010	10X	*VERSION[7:0]* (chip version)	*VERSION[7:0]*	*All zeros*

Notes:
1. *TRIMT[7:0]* is the VREF trim value for all 71M6xx3 devices. Note that the *TRIMT[7:0]* 8-bit value is formed by *RMT_RD[8]* and *RMT_RD[7:1]*. See the 71M6xxx Data Sheet for the equations related to *TRIMT[7:0]* and the corresponding temperature coefficient.
2. *TRIMBGB[7:0]* and *TRIMBGD[7:0]* are trim values used for characterizing the 71M6113 (0.5%) and 71M6203 (0.1%) over temperature. See the 71M6xxx Data sheet for the equations related to *TRIMBGB[7:0]* and *TRIMBGD[7:0]* and the corresponding temperature coefficients.
3. See 2.5.6 71M6xx3 Temperature Sensor on page 56.
4. See 2.5.8 71M6xx3 VCC Monitor on page 56.

With hardware and trim-related information on each connected 71M6xx3 Isolated Sensor available to the 71M6543, the MPU can implement temperature compensation of the energy measurement based on the individual temperature characteristics of the 71M6xx3 Isolated Sensors. See 4.5 Metrology Temperature Compensation for details.

Table 6 shows all I/O RAM registers used for control of the external 71M6xx3 Isolated Sensors. See the 71M6xx3 Data Sheet for additional details.

Table 6: I/O RAM Control Bits for Isolated Sensor

Name	Address	RST Default	WAKE Default	R/W	Description
RCMD[4:0]	SFR FC[4:0]	0	0	R/W	When the MPU writes a non-zero value to *RCMD*, the 71M6543 issues a command to the corresponding isolated sensor selected with *RCMD[1:0]*. When the command is complete, the 71M6543 clears *RCMD[4:2]*. The command code itself is in *RCMD[4:2]*.
PERR_RD *PERR_WR*	SFR FC[6] SFR FC[5]	0	0	R/W	The 71M6543 sets these bits to indicate that a parity error on the isolated sensor has been detected. Once set, the bits are remembered until they are cleared by the MPU.
CHOPR[1:0]	2709[7:6]	00	00	R/W	The CHOP settings for the isolated sensors. 00 – Auto chop. Change every multiplexer frame. 01 – Positive 10 – Negative 11 – Same as 00
TMUXR2[2:0]	270A[2:0]	000	000	R/W	The TMUX bits for control of the isolated sensor.
TMUXR4[2:0]	270A[6:4]	000	000	R/W	The TMUX bits for control of the isolated sensor.
TMUXR6[2:0]	2709[2:0]	000	000	R/W	The TMUX bits for control of the isolated sensor.
RMT_RD[15:8] *RMT_RD[7:0]*	2602[7:0] 2603[7:0]	0	0	R	The read buffer for 71M6xx3 read operations.
RFLY_DIS	210C[3]	0	0	R/W	Controls how the 71M6543 drives the 71M6xx3 power pulse. When set, the power pulse is driven high and low. When cleared, it is driven high followed by an open circuit fly-back interval.
RMT2_E	2709[3]	0	0	R/W	Enables the isolated remote sensor interface and re-configures pins IADC2-IADC3 as a balanced pair digital remote interface.
RMT4_E	2709[4]	0	0	R/W	Enables the isolated remote sensor interface and re-configures pins IADC4-IADC5 as a balanced pair digital remote interface.
RMT6_E	2709[5]	0	0	R/W	Enables the isolated remote sensor interface and re-configures pins IADC6-IADC7 as a balanced pair digital remote interface.
Refer to Table 70 starting on page 102 for more complete details about these I/O RAM locations.					

2.3 Digital Computation Engine (CE)

The CE, a dedicated 32-bit signal processor, performs the precision computations necessary to accurately measure energy. The CE calculations and processes include:

- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied by the constant sample time).
- Frequency-insensitive delay cancellation on all channels (to compensate for the delay between samples caused by the multiplexing scheme).
- 90° phase shifter (for VAR calculations).
- Pulse generation.
- Monitoring of the input signal frequency (for frequency and phase information).
- Monitoring of the input signal amplitude (for sag detection).
- Scaling of the processed samples based on calibration coefficients.
- Scaling of samples based on temperature compensation information.

2.3.1 CE Program Memory

The CE program resides in flash memory. Common access to flash memory by the CE and MPU is controlled by a memory share circuit. Each CE instruction word is two bytes long. Allocated flash space for the CE program cannot exceed 4096 16-bit words (8 KB). The CE program counter begins a pass through the CE code each time multiplexer state 0 begins. The code pass ends when a HALT instruction is executed. For proper operation, the code pass must be completed before the multiplexer cycle ends.

The CE program must begin on a 1 KB boundary of the flash address. The I/O RAM control field *CE_LCTN[6/5:0]* (*I/O RAM 0x2109[6/5:0]*) on the 71M6543F and *CE_LCTN[6:0]* (*I/O RAM 0x2109[6:0]*) on the 71M6543G defines which 1 KB boundary contains the CE code. Thus, the first CE instruction is located at 1024**CE_LCTN[5:0]* on the 71M6543F and 1024**CE_LCTN[6:0]* on the 71M6543G.

2.3.2 CE Data Memory

The CE and MPU share data memory (RAM). Common access to XRAM by the CE and MPU is controlled by a memory share circuit. The CE can access up to 3 KB of the 5 KB data RAM (XRAM), i.e. from RAM address 0x0000 to 0x0C00.

The XRAM can be accessed by the FIR filter block, the RTM circuit, the CE, and the MPU. Assigned time slots are reserved for FIR and MPU, respectively, to prevent bus contention for XRAM data access by the CE.

The MPU reads and writes the XRAM shared between the CE and MPU as the primary means of data communication between the two processors.

The CE is aided by support hardware to facilitate implementation of equations, pulse counters, and accumulators. This hardware is controlled through I/O RAM field *EQU[2:0]* (equation assist, *I/O RAM 0x2106[7:5]*), bit *DIO_PV (I/O RAM 0x2457[6]),* bit *DIO_PW* (pulse count assist, *I/O RAM 0x2457[7]*), and *SUM_SAMPS[12:0]* (accumulation assist, *I/O RAM 0x2107[4:0]* and *0x2108[7:0]*).

The integration time for each energy output, when using standard CE code, is *SUM_SAMPS[12:0]* /2184.53 (with *MUX_DIV[3:0]* = 7, *I/O RAM 0x2100[7:4]*). CE hardware issues the XFER_BUSY interrupt when the accumulation is complete.

2.3.3 CE Communication with the MPU

The CE outputs six signals to the MPU: CE_BUSY, XFER_BUSY, XPULSE, YPULSE, WPULSE and VPULSE. These are connected to the MPU interrupt service. CE_BUSY indicates that the CE is actively processing data. This signal occurs once every multiplexer frame. XFER_BUSY indicates that the CE is updating to the output region of the CE RAM, which occurs whenever an accumulation cycle has been completed. Both, CE_BUSY and XFER_BUSY are cleared when the CE executes a HALT instruction.

XPULSE and YPULSE can be configured to interrupt the MPU and indicate zero crossings of the mains voltage, sag failures, or other significant events. Additionally, these signals can be connected directly to DIO pins to provide direct outputs from the CE. Interrupts associated with these signals always occur on the leading edge.