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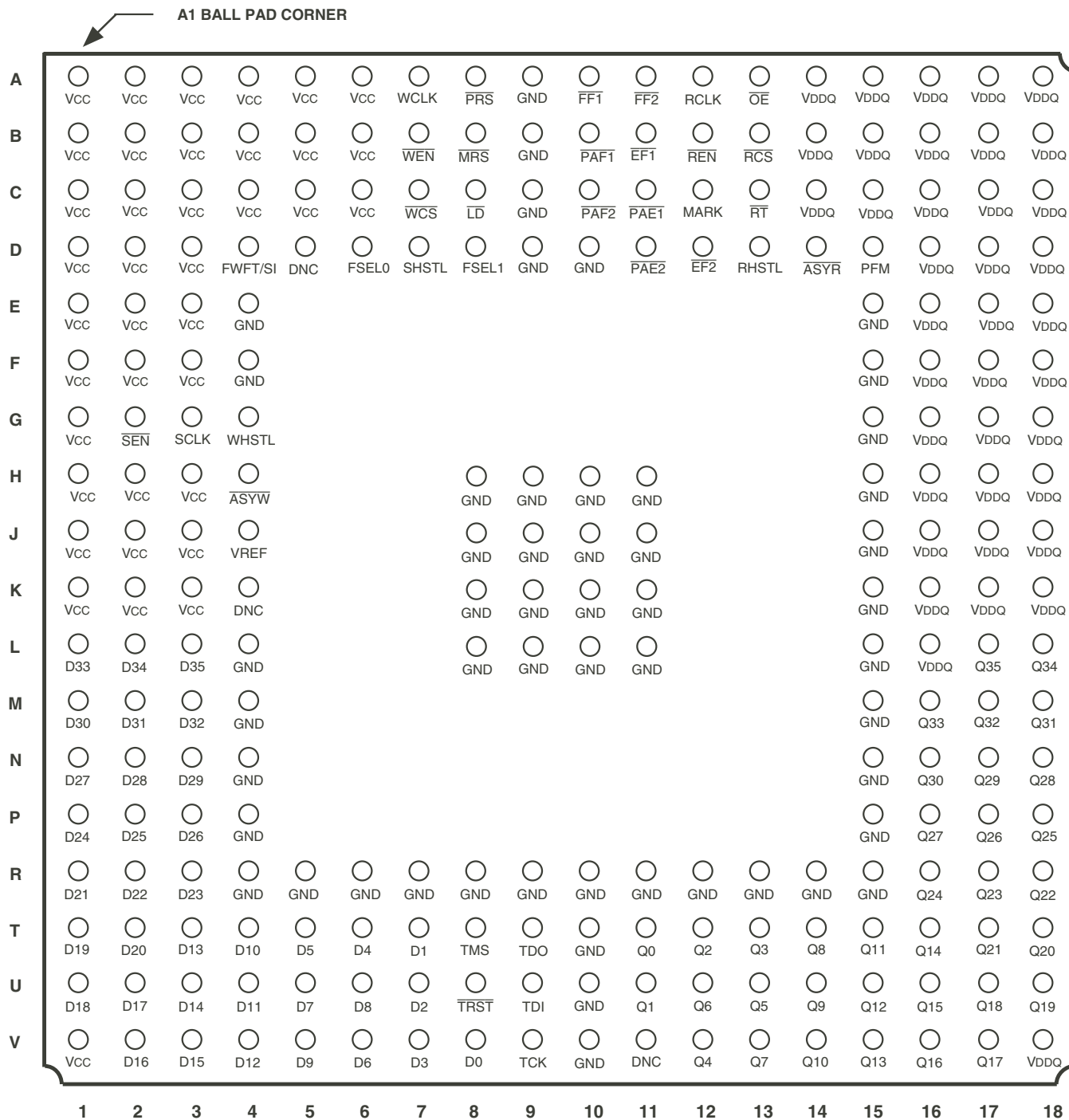
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PIN CONFIGURATION



6723 drw02

NOTE:
1. DNC - Do Not Connect.

PBGA: 1mm pitch, 19mm x 19mm (BB240, order code: BB)
TOP VIEW

DESCRIPTION:

The IDT72T36135M is an exceptionally deep, extremely high speed, CMOS First-In-First-Out (FIFO) memory with clocked read and write controls and a wide extended x36 bus to allow ample data flow. These FIFOs offer several key user benefits:

- High density offering of 18 Mbit
- 200MHz R/W Clocks supporting 7.2Gbps of data throughput
- User selectable MARK location for retransmit
- User selectable I/O structure for HSTL or LVTTTL
- Asynchronous/Synchronous translation on the read or write ports
- The first word data latency period, from the time the first word is written to an empty FIFO to the time it can be read, is fixed and short.

TeraSync FIFOs are particularly appropriate for network, video, telecommunications, data communications and other applications that need to buffer large amounts of data at very high performance.

The input port can be selected as either a Synchronous (clocked) interface, or Asynchronous interface. During Synchronous operation the input port is controlled by a Write Clock (WCLK) input and a Write Enable (\overline{WEN}) input. Data present on the Dn data inputs is written into the FIFO on every rising edge of WCLK when \overline{WEN} is asserted. During Asynchronous operation only the WR input is used to write data into the FIFO. Data is written on a rising edge of WR, the \overline{WEN} input should be tied to its active state, (LOW).

The input port can be selected for either 2.5V LVTTTL or HSTL operation, this operation is selected by the state of the WHSTL input during a master reset. A Write Chip Select input (\overline{WCS}) is provided for use when the write port is in both LVTTTL and HSTL modes. During operation the \overline{WCS} input can be used to disable write port inputs (data only).

The output port can be selected as either a Synchronous (clocked) interface, or Asynchronous interface. During Synchronous operation the output port is controlled by a Read Clock (RCLK) input and Read Enable (\overline{REN}) input. Data is read from the FIFO on every rising edge of RCLK when \overline{REN} is asserted. During Asynchronous operation only the RD input is used to read data from the FIFO. Data is read on a rising edge of RD, the \overline{REN} input should be tied to its active state, LOW. When Asynchronous operation is selected on the output port the FIFO must be configured for Standard IDT mode, also the \overline{RCS} should be tied LOW and the \overline{OE} input used to provide three-state control of the outputs, Qn.

The output port can be selected for either 2.5V LVTTTL or HSTL operation, this operation is selected by the state of the RHSTL input during a master reset.

An Output Enable (\overline{OE}) input is provided for three-state control of the outputs. A Read Chip Select (\overline{RCS}) input is also provided, the \overline{RCS} input is synchronized to the read clock, and also provides three-state control of the Qn data outputs. When \overline{RCS} is disabled, the data outputs will be high impedance. During Asynchronous operation of the output port, \overline{RCS} should be enabled, held LOW.

The frequencies of both the RCLK and the WCLK signals may vary from 0 to fMAX with complete independence. There are no restrictions on the frequency of the one clock input with respect to the other.

There are two possible timing modes of operation with these devices: IDT Standard mode and First Word Fall Through (FWFT) mode.

In *IDT Standard mode*, the first word written to an empty FIFO will not appear on the data output lines unless a specific read operation is performed. A read operation, which consists of activating \overline{REN} and enabling a rising RCLK edge, will shift the word from internal memory to the data output lines.

In *FWFT mode*, the first word written to an empty FIFO is clocked directly to the data output lines after three transitions of the RCLK signal. A \overline{REN} does not have to be asserted for accessing the first word. However, subsequent words written to the FIFO do require a LOW on \overline{REN} for access. The state of the FWFT/SI input during Master Reset determines the timing mode in use.

For applications requiring more data storage capacity than a single FIFO can provide, the FWFT timing mode permits depth expansion by chaining FIFOs in series (i.e. the data outputs of one FIFO are connected to the corresponding data inputs of the next). No external logic is required.

The 18M-bit TeraSync FIFO has 8 flag pins, $\overline{EF}/\overline{OR}[1:2]$ (Empty Flag or Output Ready), $\overline{FF}/\overline{IR}[1:2]$ (Full Flag or Input Ready), $\overline{PAE}[1:2]$ (Programmable Almost-Empty flag) and $\overline{PAF}[1:2]$ (Programmable Almost-Full flag). The $\overline{EF}[1:2]$ and $\overline{FF}[1:2]$ functions are selected in IDT Standard mode. The $\overline{IR}[1:2]$ and $\overline{OR}[1:2]$ functions are selected in FWFT mode. $\overline{PAE}[1:2]$ and $\overline{PAF}[1:2]$ are always available for use, irrespective of timing mode. Each flag has a double because the 18M FIFO was designed as a Multi-chip Module, so each set of flags supports its respective internal 9M FIFO. Some extra external gating logic will have to be used to accurately read each flag output. This will be covered in the flagging section of the datasheet.

$\overline{PAE}[1:2]$ and $\overline{PAF}[1:2]$ can be programmed independently to switch at any point in memory. Programmable offsets determine the flag switching threshold and can be loaded by two methods: parallel or serial. Eight default offset settings are also provided, so that $\overline{PAE}[1:2]$ can be set to switch at a predefined number of locations from the empty boundary and the $\overline{PAF}[1:2]$ threshold can also be set at similar predefined values from the full boundary. The default offset values are set during Master Reset by the state of the FSEL0, FSEL1, and \overline{LD} pins.

For serial programming, \overline{SEN} together with \overline{LD} on each rising edge of SCLK, are used to load the offset registers via the Serial Input (SI). For parallel programming, \overline{WEN} together with \overline{LD} on each rising edge of WCLK, are used to load the offset registers via Dn. \overline{REN} together with \overline{LD} on each rising edge of RCLK can be used to read the offsets in parallel from Qn regardless of whether serial or parallel offset loading has been selected.

During Master Reset (\overline{MRS}) the following events occur: the read and write pointers are set to the first location of the FIFO. The FWFT pin selects IDT Standard mode or FWFT mode.

The Partial Reset (\overline{PRS}) also sets the read and write pointers to the first location of the memory. However, the timing mode, programmable flag programming method, and default or programmed offset settings existing before Partial Reset remain unchanged. The flags are updated according to the timing mode and offsets in effect. \overline{PRS} is useful for resetting a device in mid-operation, when reprogramming programmable flags would be undesirable.

It is also possible to select the timing mode of the $\overline{PAE}[1:2]$ (Programmable Almost-Empty flag) and $\overline{PAF}[1:2]$ (Programmable Almost-Full flag) outputs. The timing modes can be set to be either asynchronous or synchronous for the $\overline{PAE}[1:2]$ and $\overline{PAF}[1:2]$ flags.

If asynchronous $\overline{PAE}/\overline{PAF}[1:2]$ configuration is selected, the $\overline{PAE}[1:2]$ is asserted LOW on the LOW-to-HIGH transition of RCLK. $\overline{PAE}[1:2]$ is reset to HIGH on the LOW-to-HIGH transition of WCLK. Similarly, the $\overline{PAF}[1:2]$ is asserted LOW on the LOW-to-HIGH transition of WCLK and $\overline{PAF}[1:2]$ is reset to HIGH on the LOW-to-HIGH transition of RCLK.

If synchronous $\overline{PAE}/\overline{PAF}[1:2]$ configuration is selected, the $\overline{PAE}[1:2]$ is asserted and updated on the rising edge of RCLK only and not WCLK. Similarly, $\overline{PAF}[1:2]$ is asserted and updated on the rising edge of WCLK only and not RCLK. The mode desired is configured during Master Reset by the state of the Programmable Flag Mode (PFM) pin.

This device includes a Retransmit from Mark feature that utilizes two control inputs, MARK and \overline{RT} (Retransmit). If the MARK input is enabled with respect to the RCLK, the memory location being read at that point will be marked. Any subsequent retransmit operation, \overline{RT} goes LOW, will reset the read pointer to this 'marked' location.

If, at any time, the FIFO is not actively performing an operation, the chip will automatically power down. Once in the power down state, the standby supply current consumption is minimized. Initiating any operation (by activating control

DESCRIPTION (CONTINUED)

inputs) will immediately take the device out of the power down state.

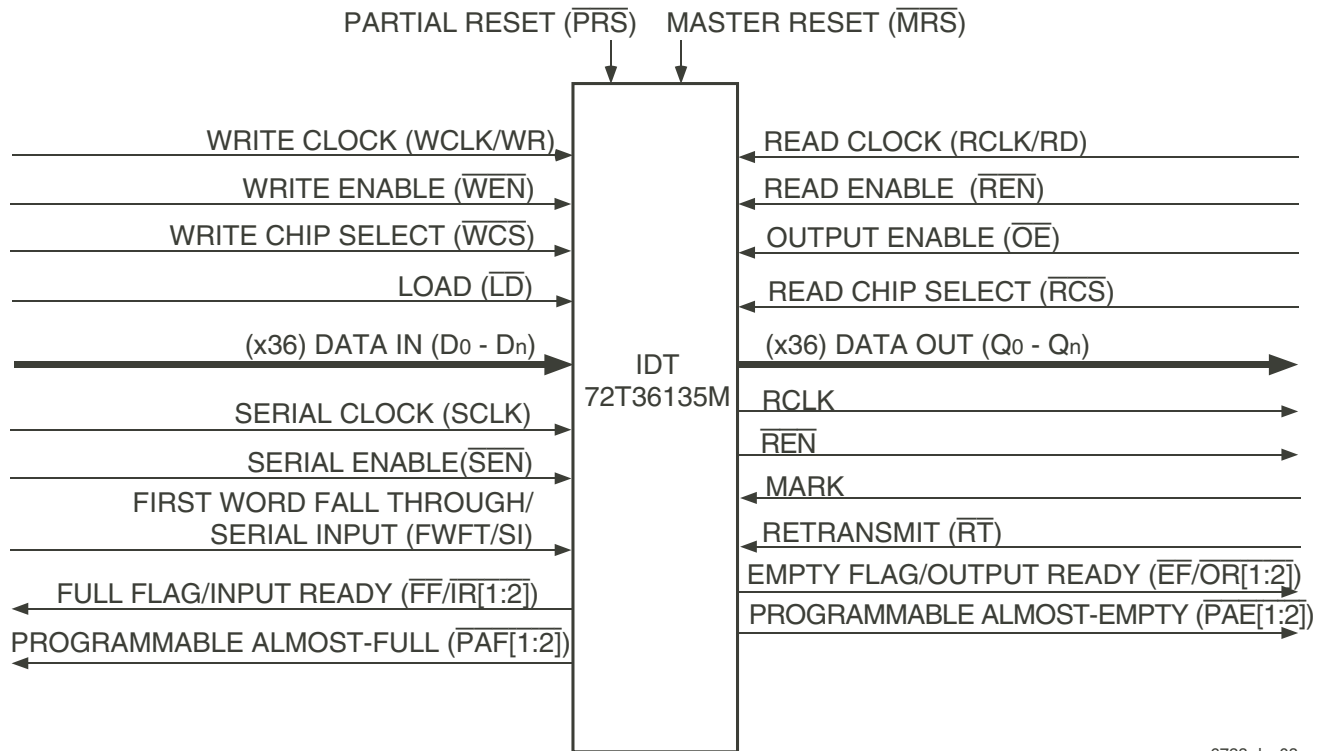
Both an Asynchronous Output Enable pin (\overline{OE}) and Synchronous Read Chip Select pin (\overline{RCS}) are provided on the FIFO. The Synchronous Read Chip Select is synchronized to the RCLK. Both the output enable and read chip select control the output buffer of the FIFO, causing the buffer to be either HIGH impedance or LOW impedance.

A JTAG test port is provided, here the FIFO has fully functional Boundary Scan feature, compliant with IEEE 1449.1 Standard Test Access Port and Boundary Scan Architecture. Special consideration should be taken into

account for JTAG testing since the device is a MCM. Please see JTAG section for further details.

The TeraSync FIFO has the capability of operating its ports (write and/or read) in either LVTTTL or HSTL mode, each ports selection independent of the other. The write port selection is made via WHSTL and the read port selection via RHSTL. An additional input HSTL is also provided, this allows the user to select HSTL operation for other pins on the device (not associated with the write or read ports).

The IDT72T36135M is fabricated using high speed submicron CMOS technology.



6723 drw03

Figure 1. Single Device Configuration Signal Flow Diagram

PIN DESCRIPTION

| Symbol | Name | I/O TYPE | Description |
|--------------------------------------------------|-----------------------------------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $\overline{\text{ASYR}}^{(1)}$ | Asynchronous Read Port | LVTTL INPUT | A HIGH on this input during Master Reset will select Synchronous read operation for the output port. A LOW will select Asynchronous operation. If Asynchronous is selected the FIFO must operate in IDT Standard mode. |
| $\overline{\text{ASYW}}^{(1)}$ | Asynchronous Write Port | LVTTL INPUT | A HIGH on this input during Master Reset will select Synchronous write operation for the input port. A LOW will select Asynchronous operation. |
| D0–D35 | Data Inputs | HSTL-LVTTL INPUT | Data inputs for a 36-bit bus. |
| $\overline{\text{EF}}/\overline{\text{OR}}[1:2]$ | Empty Flag/ Output Ready | HSTL-LVTTL OUTPUT | In the IDT Standard mode, the $\overline{\text{EF}}[1:2]$ function is selected. $\overline{\text{EF}}[1:2]$ indicates whether or not the FIFO memory is empty. In FWFT mode, the $\overline{\text{OR}}[1:2]$ function is selected. $\overline{\text{OR}}[1:2]$ indicates whether or not there is valid data available at the outputs. Please see Flagging section for external gating instructions of these flags. |
| $\overline{\text{FF}}/\overline{\text{IR}}[1:2]$ | Full Flag/ Input Ready | HSTL-LVTTL OUTPUT | In the IDT Standard mode, the $\overline{\text{FF}}[1:2]$ function is selected. $\overline{\text{FF}}[1:2]$ indicates whether or not the FIFO memory is full. In the FWFT mode, the $\overline{\text{IR}}[1:2]$ function is selected. $\overline{\text{IR}}[1:2]$ indicates whether or not there is space available for writing to the FIFO memory. Please see Flagging section for external gating instructions of these flags. |
| FSEL0 ⁽¹⁾ | Flag Select Bit 0 | LVTTL INPUT | During Master Reset, this input along with FSEL 1 and the $\overline{\text{LD}}$ pin, will select the default offset values for the programmable flags PAE[1:2] and PAF[1:2]. There are up to eight possible settings available. |
| FSEL1 ⁽¹⁾ | Flag Select Bit 1 | LVTTL INPUT | During Master Reset, this input along with FSEL0 and the $\overline{\text{LD}}$ pin will select the default offset values for the programmable flags PAE[1:2] and PAF[1:2]. There are up to eight possible settings available. |
| FWFT/SI | First Word Fall Through/Serial In | HSTL-LVTTL INPUT | During Master Reset, selects First Word Fall Through or IDT Standard mode. After Master Reset, this pin functions as a serial input for loading offset registers. If Asynchronous operation of the read port has been selected then the FIFO must be set-up in IDT Standard mode. |
| $\overline{\text{LD}}$ | Load | HSTL-LVTTL INPUT | This is a dual purpose pin. During Master Reset, the state of the $\overline{\text{LD}}$ input along with FSEL0 and FSEL1, determines one of eight default offset values for the PAE[1:2] and PAF[1:2] flags, along with the method by which these offset registers can be programmed, parallel or serial (see Table 1). After Master Reset, this pin enables writing to and reading from the offset registers. |
| MARK | Mark for Retransmit | HSTL-LVTTL INPUT | When this pin is asserted the current location of the read pointer will be marked. Any subsequent Retransmit operation will reset the read pointer to this position. |
| $\overline{\text{MRS}}$ | Master Reset | HSTL-LVTTL INPUT | $\overline{\text{MRS}}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During Master Reset, the FIFO is configured for either FWFT or IDT Standard mode, Synchronous/Asynchronous operation of the read or write port, one of eight programmable flag default settings, serial or parallel programming of the offset settings, zero latency timing mode, and synchronous versus asynchronous programmable flag timing modes. |
| $\overline{\text{OE}}$ | Output Enable | HSTL-LVTTL INPUT | $\overline{\text{OE}}$ provides Asynchronous three-state control of the data outputs, Qn. During a Master or Partial Reset the $\overline{\text{OE}}$ input is the only input that provide High-Impedance control of the data outputs. |
| $\overline{\text{PAE}}[1:2]$ | Programmable Almost-Empty Flag | HSTL-LVTTL OUTPUT | $\overline{\text{PAE}}[1:2]$ goes LOW if the number of words in the FIFO memory is less than offset n, which is stored in the Empty Offset register. $\overline{\text{PAE}}[1:2]$ goes HIGH if the number of words in the FIFO memory is greater than or equal to offset n. Please see Flagging section for external gating instructions of these flags. |
| $\overline{\text{PAF}}[1:2]$ | Programmable Almost-Full Flag | HSTL-LVTTL OUTPUT | $\overline{\text{PAF}}[1:2]$ goes HIGH if the number of free locations in the FIFO memory is more than offset m, which is stored in the Full Offset register. $\overline{\text{PAF}}[1:2]$ goes LOW if the number of free locations in the FIFO memory is less than or equal to m. Please see Flagging section for external gating instructions of these flags. |
| PFM ⁽¹⁾ | Programmable Flag Mode | LVTTL INPUT | During Master Reset, a LOW on PFM will select Asynchronous Programmable flag timing mode. A HIGH on PFM will select Synchronous Programmable flag timing mode. |
| $\overline{\text{PRS}}$ | Partial Reset | HSTL-LVTTL INPUT | $\overline{\text{PRS}}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During Partial Reset, the existing mode (IDT or FWFT), programming method (serial or parallel), and programmable flag settings are all retained. |
| Q0–Q35 | Data Outputs | HSTL-LVTTL OUTPUT | Data outputs for an 36-bit bus. |
| RCLK/RD | Read Clock/ Read Strobe | HSTL-LVTTL INPUT | If Synchronous operation of the read port has been selected, when enabled by $\overline{\text{REN}}$, the rising edge of RCLK reads data from the FIFO memory and offsets from the programmable registers. If LD is LOW, the values loaded into the offset registers is output on a rising edge of RCLK. If Asynchronous operation of the read |

PIN DESCRIPTION (CONTINUED)

| Symbol | Name | I/O TYPE | Description |
|----------------------------------|------------------------------|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RCLK/ RD | Read Clock/ Read Strobe | HSTL-LVTTL INPUT | port has been selected, a rising edge on RD reads data from the FIFO in an Asynchronous manner. \overline{REN} should be tied LOW. |
| \overline{RCS} | Read Chip Select | HSTL-LVTTL INPUT | \overline{RCS} provides synchronous control of the read port and output impedance of Qn, synchronous to RCLK. During a Master Reset or Partial Reset the \overline{RCS} input is don't care, if \overline{OE} is LOW the data outputs will be Low-Impedance regardless of \overline{RCS} . |
| \overline{REN} | Read Enable | HSTL-LVTTL INPUT | If Synchronous operation of the read port has been selected, \overline{REN} enables RCLK for reading data from the FIFO memory and offset registers. If Asynchronous operation of the read port has been selected, the \overline{REN} input should be tied LOW. |
| RHSTL ⁽¹⁾ | Read Port HSTL Select | LVTTL INPUT | This pin is used to select HSTL or 2.5v LVTTL outputs for the FIFO. If HSTL inputs are required, this input must be tied HIGH. Otherwise it should be tied LOW. |
| \overline{RT} | Retransmit | HSTL-LVTTL INPUT | \overline{RT} asserted on the rising edge of RCLK initializes the READ pointer to zero, sets the $\overline{EF}[1:2]$ flag to LOW ($\overline{OR}[1:2]$ to HIGH in FWFT mode) and doesn't disturb the write pointer, programming method, existing timing mode or programmable flag settings. If a mark has been set via the MARK input pin, then the read pointer will jump to the 'mark' location. |
| SCLK | Serial Clock | HSTL-LVTTL INPUT | A rising edge on SCLK will clock the serial data present on the SI input into the offset registers providing that \overline{SEN} is enabled. |
| \overline{SEN} | Serial Enable | HSTL-LVTTL INPUT | \overline{SEN} enables serial loading of programmable flag offsets. |
| SHSTL | System HSTL Select | LVTTL INPUT | All inputs not associated with the write or read port can be selected for HSTL operation via the SHSTL input. |
| TCK ⁽²⁾ | JTAG Clock | HSTL-LVTTL INPUT | Clock input for JTAG function. TMS and TDI are sampled on the rising edge of TCK. Data is output on TDO on the falling edge. |
| \overline{TRST} ⁽²⁾ | JTAG Reset | HSTL-LVTTL INPUT | \overline{TRST} is an asynchronous reset pin for the JTAG controller. |
| TMS | JTAG Mode Select | HSTL-LVTTL INPUT | TMS is a serial input pin. Bits are serially loaded on the rising edge of TCK, which selects 1 of 5 modes of operation for the JTAG boundary scan. |
| TDI | Test Data Input | HSTL-LVTTL INPUT | During JTAG boundary scan operation test data is serially loaded via TDI on the rising edge of TCK. This is also the data for the Instruction Register, ID Register and Bypass Register. |
| TDO | Test Data Output | HSTL-LVTTL OUTPUT | During JTAG boundary scan operation test data is serially output via TDO on the falling edge of TCK. This output is in High-Z except when shifting, while in SHIFT-DR and SHIFT-IR controller states. |
| \overline{WEN} | Write Enable | HSTL-LVTTL INPUT | When Synchronous operation of the write port has been selected, \overline{WEN} enables WCLK for writing data into the FIFO memory and offset registers. If Asynchronous operation of the write port has been selected, the \overline{WEN} input should be tied LOW. |
| \overline{WCS} | Write Chip Select | HSTL-LVTTL INPUT | This pin disables the write port data inputs when the device write port is configured for HSTL mode. This provides added power savings. |
| WCLK/ WR | Write Clock/ Write Strobe | HSTL-LVTTL INPUT | If Synchronous operation of the write port has been selected, when enabled by \overline{WEN} , the rising edge of WCLK writes data into the FIFO. If Asynchronous operation of the write port has been selected, WR writes data into the FIFO on a rising edge in an Asynchronous manner, (\overline{WEN} should be tied to its active state). |
| WHSTL ⁽¹⁾ | Write Port HSTL Select | LVTTL INPUT | This pin is used to select HSTL or 2.5V LVTTL inputs for the FIFO. If HSTL inputs are required, this input must be tied HIGH. Otherwise it should be tied LOW. |
| Vcc | +2.5v Supply | Power | These are Vcc supply inputs and must be connected to the 2.5V supply rail. |
| GND | Ground Pin | GND | These are Ground pins and must be connected to the GND rail. |
| Vref | Reference Voltage | I | This is a Voltage Reference input and must be connected to a voltage level determined from the table, "Recommended DC Operating Conditions". This provides the reference voltage when using HSTL class inputs. If HSTL class inputs are not being used, this pin should be tied LOW. |
| VDDQ | O/P Rail Voltage | I | This pin should be tied to the desired voltage rail for providing power to the output drivers. |

NOTES:

1. Inputs should not change state after Master Reset.
2. If the JTAG feature is not being used, TCK and \overline{TRST} should be tied LOW.

ABSOLUTE MAXIMUM RATINGS

| Symbol | Rating | Commercial | Unit |
|--------|--------------------------------------|-----------------------------|------|
| VTERM | Terminal Voltage with respect to GND | -0.5 to +3.6 ⁽²⁾ | V |
| TSTG | Storage Temperature | -55 to +125 | °C |
| IOUT | DC Output Current | -50 to +50 | mA |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Compliant with JEDEC JESD8-5. VCC terminal only.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|----------------------|--------------------------|------------|-------------------|------|
| CIN ^(2,3) | Input Capacitance | VIN = 0V | 15 ⁽³⁾ | pF |
| COU ^(1,2) | Output Capacitance | VOUT = 0V | 10.5 | pF |

NOTES:

- With output deselected, ($\overline{OE} \geq V_{IH}$).
- Characterized values, not currently tested.
- CIN for Vref is 40pF.

RECOMMENDED DC OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---------------------|----------------------------------|----------|------|----------|------|
| VCC | Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| GND | Supply Voltage | 0 | 0 | 0 | V |
| VIH | Input High Voltage — LVTTTL | 1.7 | — | 3.45 | V |
| | | VREF+0.2 | — | VDDQ+0.3 | V |
| | | VREF+0.2 | — | VDDQ+0.3 | V |
| VIL | Input Low Voltage — LVTTTL | -0.3 | — | 0.7 | V |
| | | -0.3 | — | VREF-0.2 | V |
| | | -0.3 | — | VREF-0.2 | V |
| VREF ⁽¹⁾ | Voltage Reference Input — eHSTL | 0.8 | 0.9 | 1.0 | V |
| | | 0.68 | 0.75 | 0.9 | V |
| TA | Operating Temperature Commercial | 0 | — | 70 | °C |
| TA | Operating Temperature Industrial | -40 | — | 85 | °C |

NOTE:

- VREF is only required for HSTL or eHSTL inputs. VREF should be tied LOW for LVTTTL operation.
- Outputs are not 3.3V tolerant.

DC ELECTRICAL CHARACTERISTICS

(Commercial: $V_{CC} = 2.5V \pm 0.125V$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$; Industrial: $V_{CC} = 2.5V \pm 0.125V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$)

| Symbol | Parameter | Min. | Max. | Unit |
|-----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------|----------------------|----------------|
| I _{LI} | Input Leakage Current | -10 | 10 | μA |
| I _{LO} | Output Leakage Current | -10 | 10 | μA |
| V _{OH} ⁽⁵⁾ | Output Logic "1" Voltage, I _{OH} = -8 mA @V _{DDQ} = 2.5V ± 0.125V (LVTTTL) I _{OH} = -8 mA @V _{DDQ} = 1.8V ± 0.1V (eHSTL) I _{OH} = -8 mA @V _{DDQ} = 1.5V ± 0.1V (HSTL) | V _{DDQ} -0.4 V _{DDQ} -0.4 V _{DDQ} -0.4 | — — — | V V V |
| V _{OL} | Output Logic "0" Voltage, I _{OL} = 8 mA @V _{DDQ} = 2.5V ± 0.125V (LVTTTL) I _{OL} = 8 mA @V _{DDQ} = 1.8V ± 0.1V (eHSTL) I _{OL} = 8 mA @V _{DDQ} = 1.5V ± 0.1V (HSTL) | — — — | 0.4V 0.4V 0.4V | V V V |
| I _{CC1} ^(1,2) | Active V _{CC} Current (V _{CC} = 2.5V) I/O = LVTTTL I/O = HSTL I/O = eHSTL | — — — | 120 180 180 | mA mA mA |
| I _{CC2} ⁽¹⁾ | Standby V _{CC} Current (V _{CC} = 2.5V) I/O = LVTTTL I/O = HSTL I/O = eHSTL | — — — | 40 140 140 | mA mA mA |

NOTES:

- Both WCLK and RCLK toggling at 20MHz. Data inputs toggling at 10MHz. \overline{WCS} = HIGH, \overline{REN} or \overline{RCS} = HIGH.
- For the IDT72T36135M, typical ICC1 calculation (with data outputs in Low-Impedance):
- For all devices, typical IDDQ calculation:
 - with data outputs in High-Impedance: $IDDQ$ (mA) = 0.15 x fs, fs = WCLK = RCLK frequency (in MHz)
 - with data outputs in Low-Impedance: $IDDQ$ (mA) = (CL x V_{DDQ} x fs x N)/2000
 - fs = WCLK = RCLK frequency (in MHz), V_{DDQ} = 2.5V for LVTTTL; 1.5V for HSTL; 1.8V for eHSTL, CL = capacitive load (pf), t_A = 25°C, N = Number of outputs switching.
- Total Power consumed: $PT = (V_{CC} \times I_{CC}) + V_{DDQ} \times I_{DDQ}$.
- Outputs are not 3.3V tolerant.

AC ELECTRICAL CHARACTERISTICS⁽¹⁾ — SYNCHRONOUS TIMING

(Commercial: V_{CC} = 2.5V ± 5%, T_A = 0°C to +70°C; Industrial: V_{CC} = 2.5V ± 5%, T_A = -40°C to +85°C)

| Symbol | Parameter | Commercial | | Com'l & Ind'l | | Unit |
|--------------------|-----------------------------------------------------------|----------------|------|----------------|------|------|
| | | IDT72T36135ML5 | | IDT72T36135ML6 | | |
| | | Min. | Max. | Min. | Max. | |
| f _c | Clock Cycle Frequency (Synchronous) | — | 200 | — | 166 | MHz |
| t _A | Data Access Time | 0.6 | 3.6 | 0.6 | 3.8 | ns |
| t _{CLK} | Clock Cycle Time | 5 | — | 6 | — | ns |
| t _{CLKH} | Clock High Time | 2.5 | — | 3.0 | — | ns |
| t _{CLKL} | Clock Low Time | 2.5 | — | 3.0 | — | ns |
| t _{DS} | Data Setup Time | 1.5 | — | 2.0 | — | ns |
| t _{DH} | Data Hold Time | 0.5 | — | 0.5 | — | ns |
| t _{ENS} | Enable Setup Time | 1.5 | — | 2.0 | — | ns |
| t _{ENH} | Enable Hold Time | 0.5 | — | 0.5 | — | ns |
| t _{LDS} | Load Setup Time | 1.5 | — | 2.0 | — | ns |
| t _{L DH} | Load Hold Time | 0.5 | — | 0.5 | — | ns |
| t _{WCSS} | WCS setup time | 1.5 | — | 2.0 | — | ns |
| t _{WCSH} | WCS hold time | 0.5 | — | 0.5 | — | ns |
| f _s | Clock Cycle Frequency (SCLK) | — | 10 | — | 10 | MHz |
| t _{SCLK} | Serial Clock Cycle | 100 | — | 100 | — | ns |
| t _{SCKH} | Serial Clock High | 45 | — | 45 | — | ns |
| t _{SCKL} | Serial Clock Low | 45 | — | 45 | — | ns |
| t _{SDS} | Serial Data In Setup | 15 | — | 15 | — | ns |
| t _{SDH} | Serial Data In Hold | 5 | — | 5 | — | ns |
| t _{SENS} | Serial Enable Setup | 5 | — | 5 | — | ns |
| t _{SENH} | Serial Enable Hold | 5 | — | 5 | — | ns |
| t _{RS} | Reset Pulse Width ⁽³⁾ | 10 | — | 10 | — | ns |
| t _{RSS} | Reset Setup Time | 15 | — | 15 | — | ns |
| t _{HRSS} | HSTL Reset Setup Time | 4 | — | 4 | — | μs |
| t _{RSR} | Reset Recovery Time | 10 | — | 10 | — | ns |
| t _{RSF} | Reset to Flag and Output Time | — | 15 | — | 15 | ns |
| t _{WFF} | Write Clock to FF[1:2] or IR[1:2] | — | 3.6 | — | 3.7 | ns |
| t _{REF} | Read Clock to EF[1:2] or OR[1:2] | — | 3.6 | — | 3.7 | ns |
| t _{PAFS} | Write Clock to Synchronous PAF[1:2] | — | 3.6 | — | 3.7 | ns |
| t _{PAES} | Read Clock to Synchronous PAE[1:2] | — | 3.6 | — | 3.7 | ns |
| t _{RCSLZ} | RCLK to Active from High-Z ⁽³⁾ | — | 3.6 | — | 3.7 | ns |
| t _{RCSHZ} | RCLK to High-Z ⁽³⁾ | — | 3.6 | — | 3.7 | ns |
| t _{SKEW1} | Skew time between RCLK and WCLK for EF[1:2] and FF[1:2] | — | 4 | — | 5 | ns |
| t _{SKEW2} | Skew time between RCLK and WCLK for PAE[1:2] and PAF[1:2] | — | 5 | — | 6 | ns |

NOTES:

1. All AC timings apply to both Standard IDT mode and First Word Fall Through mode.
2. Pulse widths less than minimum values are not allowed.
3. Values guaranteed by design, not currently tested.
4. Industrial temperature range product for 6ns speed grade is available as a standard device. All other speed grades are available by special order.

AC ELECTRICAL CHARACTERISTICS — ASYNCHRONOUS TIMING

(Commercial: VCC = 2.5V ± 5%, TA = 0°C to +70°C; Industrial: VCC = 2.5V ± 5%, TA = -40°C to +85°C)

| Symbol | Parameter | Commercial | | Com'l & Ind'l | | Unit |
|--------|------------------------------------------------------|----------------|------|----------------|------|------|
| | | IDT72T36135ML5 | | IDT72T36135ML6 | | |
| | | Min. | Max. | Min. | Max. | |
| fA | Cycle Frequency (Asynchronous) | — | 83 | — | 66 | MHz |
| tAA | Data Access Time | 0.6 | 10 | 0.6 | 12 | ns |
| tCYC | Cycle Time | 12 | — | 15 | — | ns |
| tCYH | Cycle HIGH Time | 5 | — | 7 | — | ns |
| tCYL | Cycle LOW Time | 5 | — | 7 | — | ns |
| tRPE | Read Pulse after $\overline{EF}[1:2]$ HIGH | 10 | — | 12 | — | ns |
| tFFA | Clock to Asynchronous $\overline{FF}[1:2]$ | — | 10 | — | 12 | ns |
| tEFA | Clock to Asynchronous $\overline{EF}[1:2]$ | — | 10 | — | 12 | ns |
| tPAFA | Clock to Asynchronous Programmable Almost-Full Flag | — | 10 | — | 12 | ns |
| tPAEA | Clock to Asynchronous Programmable Almost-Empty Flag | — | 10 | — | 12 | ns |
| tOLZ | Output Enable to Output in Low Z ⁽³⁾ | 0 | — | 0 | — | ns |
| tOE | Output Enable to Output Valid | — | 3.6 | — | 3.8 | ns |
| tOHZ | Output Enable to Output in High Z ⁽³⁾ | — | 3.6 | — | 3.8 | ns |
| tHF | Clock to \overline{HF} | — | 10 | — | 12 | ns |

NOTES:

1. All AC timings apply to both Standard IDT mode and First Word Fall Through mode.
2. Industrial temperature range product for 6ns speed grade is available as a standard device. All other speed grades are available by special order.
3. Values guaranteed by design, not currently tested.

HSTL

1.5V AC TEST CONDITIONS

| | |
|-------------------------------|---------------------|
| Input Pulse Levels | 0.25 to 1.25V |
| Input Rise/Fall Times | 0.4ns |
| Input Timing Reference Levels | 0.75 |
| Output Reference Levels | V _{DDQ} /2 |

NOTE:

- V_{DDQ} = 1.5V±.

AC TEST LOADS

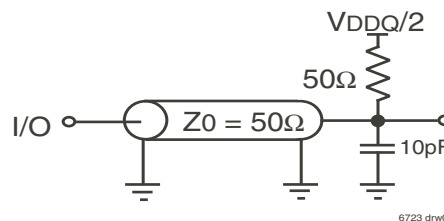


Figure 2a. AC Test Load

EXTENDED HSTL

1.8V AC TEST CONDITIONS

| | |
|-------------------------------|---------------------|
| Input Pulse Levels | 0.4 to 1.4V |
| Input Rise/Fall Times | 0.4ns |
| Input Timing Reference Levels | 0.9 |
| Output Reference Levels | V _{DDQ} /2 |

NOTE:

- V_{DDQ} = 1.8V±.

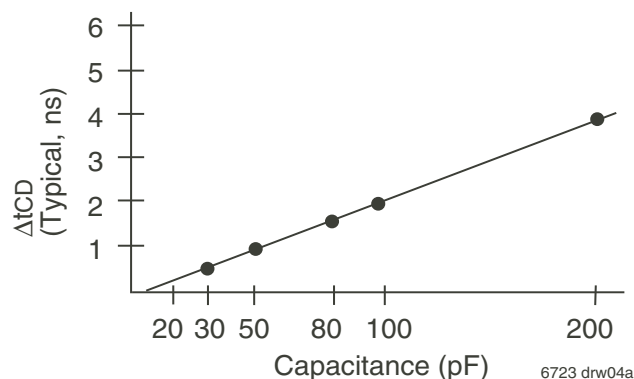


Figure 2b. Lumped Capacitive Load, Typical Derating

2.5V LVTTTL

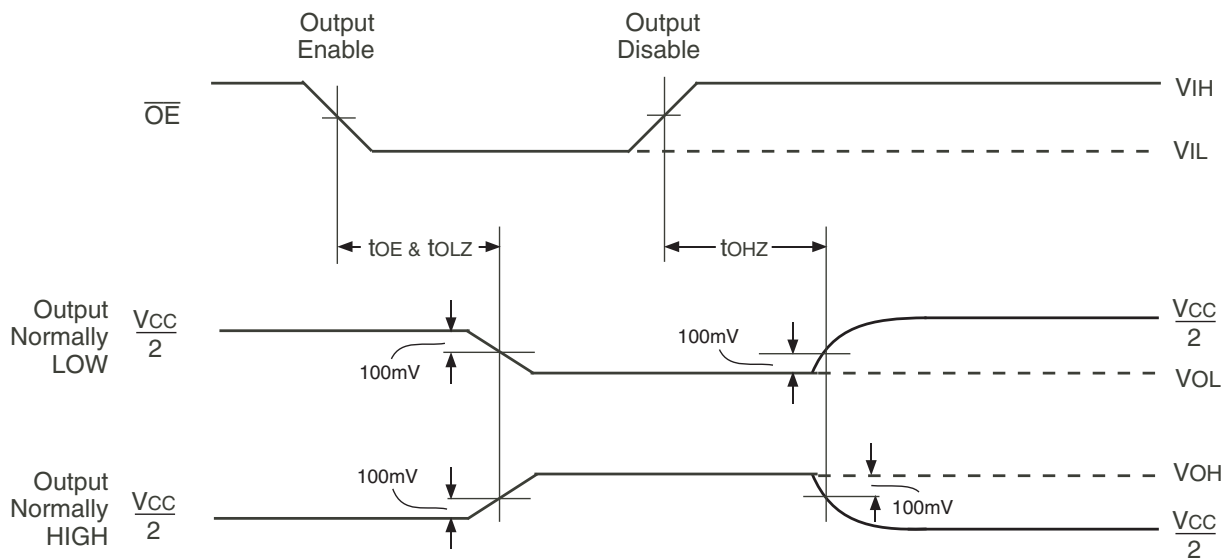
2.5V AC TEST CONDITIONS

| | |
|-------------------------------|---------------------|
| Input Pulse Levels | GND to 2.5V |
| Input Rise/Fall Times | 1ns |
| Input Timing Reference Levels | V _{CC} /2 |
| Output Reference Levels | V _{DDQ} /2 |

NOTE:

- For LVTTTL V_{CC} = V_{DDQ}.

OUTPUT ENABLE & DISABLE TIMING

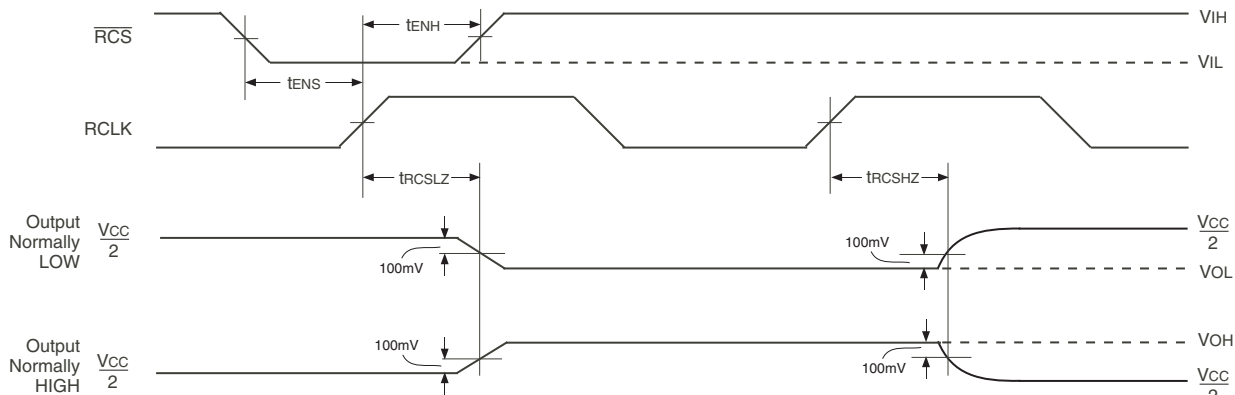


6723 drw05

NOTES:

1. \overline{REN} is HIGH.
2. \overline{RCS} is LOW.

READ CHIP SELECT ENABLE & DISABLE TIMING



6723 drw06

NOTES:

1. \overline{REN} is HIGH.
2. \overline{OE} is LOW.

FUNCTIONAL DESCRIPTION

TIMING MODES: IDT STANDARD vs FIRST WORD FALL THROUGH (FWFT) MODE

The IDT72T36135M support two different timing modes of operation: IDT Standard mode or First Word Fall Through (FWFT) mode. The selection of which mode will operate is determined during Master Reset, by the state of the FWFT/SI input.

If, at the time of Master Reset, FWFT/SI is LOW, then IDT Standard mode will be selected. This mode uses the Empty Flag ($\overline{EF}[1:2]$) to indicate whether or not there are any words present in the FIFO. It also uses the Full Flag function ($\overline{FF}[1:2]$) to indicate whether or not the FIFO has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using the Read Enable (\overline{REN}) and RCLK.

If, at the time of Master Reset, FWFT/SI is HIGH, then FWFT mode will be selected. This mode uses Output Ready ($\overline{OR}[1:2]$) to indicate whether or not there is valid data at the data outputs (Q_n). It also uses Input Ready ($\overline{IR}[1:2]$) to indicate whether or not the FIFO has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to Q_n after three RCLK rising edges, $\overline{REN} = \text{LOW}$ is not necessary. Subsequent words must be accessed using the Read Enable (\overline{REN}) and RCLK.

Various signals, both input and output signals operate differently depending on which timing mode is in effect.

IDT STANDARD MODE

In this mode, the status flags, $\overline{FF}[1:2]$, $\overline{PAF}[1:2]$, $\overline{PAE}[1:2]$, and $\overline{EF}[1:2]$ operate in the manner outlined in Table 2. To write data into to the FIFO, Write Enable (\overline{WEN}) must be LOW. Data presented to the DATA IN lines will be clocked into the FIFO on subsequent transitions of the Write Clock (WCLK). After the first write is performed, the Empty Flag ($\overline{EF}[1:2]$) will go HIGH. Subsequent writes will continue to fill up the FIFO. The Programmable Almost-Empty flag ($\overline{PAE}[1:2]$) will go HIGH after $n + 1$ words have been loaded into the FIFO, where n is the empty offset value. The default setting for these values are stated in the footnote of Table 1. This parameter is also user programmable. See section on Programmable Flag Offset Loading.

Continuing to write data into the FIFO will cause the Programmable Almost-Full flag ($\overline{PAF}[1:2]$) to go LOW. Again, if no reads are performed, the $\overline{PAF}[1:2]$ will go LOW. The offset "m" is the full offset value. The default setting for these values are stated in the footnote of Table 1. This parameter is also user programmable. See section on Programmable Flag Offset Loading.

When the FIFO is full, the Full Flag ($\overline{FF}[1:2]$) will go LOW, inhibiting further write operations. If no reads are performed after a reset, $\overline{FF}[1:2]$ will go LOW after D writes to the FIFO.

If the FIFO is full, the first read operation will cause $\overline{FF}[1:2]$ to go HIGH. Subsequent read operations will cause $\overline{PAF}[1:2]$ to go HIGH at the conditions described in Table 2. If further read operations occur, without write operations, $\overline{PAE}[1:2]$ will go LOW when there are n words in the FIFO, where n is the empty offset value. Continuing read operations will cause the FIFO to become empty. When the last word has been read from the FIFO, the $\overline{EF}[1:2]$ will go LOW inhibiting further read operations. \overline{REN} is ignored when the FIFO is empty.

When configured in IDT Standard mode, the $\overline{EF}[1:2]$ and $\overline{FF}[1:2]$ outputs are double register-buffered outputs.

Relevant timing diagrams for IDT Standard mode can be found in Figure 10, 11, 12 and 17.

FIRST WORD FALL THROUGH MODE (FWFT)

In this mode, the status flags, $\overline{IR}[1:2]$, $\overline{PAF}[1:2]$, $\overline{PAE}[1:2]$, and $\overline{OR}[1:2]$ operate in the manner outlined in Table 3. To write data into to the FIFO, \overline{WEN} must be LOW. Data presented to the DATA IN lines will be clocked into the FIFO on subsequent transitions of WCLK. After the first write is performed, the Output Ready ($\overline{OR}[1:2]$) flag will go LOW. Subsequent writes will continue to fill up the FIFO. $\overline{PAE}[1:2]$ will go HIGH after $n + 2$ words have been loaded into the FIFO, where n is the empty offset value. The default setting for these values are stated in the footnote of Table 1. This parameter is also user programmable. See section on Programmable Flag Offset Loading.

When the FIFO is full, the Input Ready ($\overline{IR}[1:2]$) flag will go HIGH, inhibiting further write operations. If no reads are performed after a reset, $\overline{IR}[1:2]$ will go HIGH after D writes to the FIFO. Note that the additional word in FWFT mode is due to the capacity of the memory plus output register.

If the FIFO is full, the first read operation will cause the $\overline{IR}[1:2]$ flag to go LOW. Subsequent read operations will cause the $\overline{PAF}[1:2]$ to go HIGH at the conditions described in Table 3. If further read operations occur, without write operations, the $\overline{PAE}[1:2]$ will go LOW when there are $n + 1$ words in the FIFO, where n is the empty offset value. Continuing read operations will cause the FIFO to become empty. When the last word has been read from the FIFO, $\overline{OR}[1:2]$ will go HIGH inhibiting further read operations. \overline{REN} is ignored when the FIFO is empty.

When configured in FWFT mode, the $\overline{OR}[1:2]$ flag output is triple register-buffered, and the $\overline{IR}[1:2]$ flag output is double register-buffered.

Relevant timing diagrams for FWFT mode can be found in Figure 13, 14, 15 and 18.

PROGRAMMING FLAG OFFSETS

Full and Empty Flag offset values are user programmable. The IDT72T36135M have internal registers for these offsets. There are eight default offset values selectable during Master Reset. These offset values are shown in Table 1. Offset values can also be programmed into the FIFO in one of two ways; serial or parallel loading method. The selection of the loading method is done using the $\overline{\text{LD}}$ (Load) pin. During Master Reset, the state of the $\overline{\text{LD}}$ input determines whether serial or parallel flag offset programming is enabled. A HIGH on $\overline{\text{LD}}$ during Master Reset selects serial loading of offset values. A LOW on $\overline{\text{LD}}$ during Master Reset selects parallel loading of offset values.

In addition to loading offset values into the FIFO, it is also possible to read the current offset values. Offset values can be read via the parallel output port Q0-Qn, regardless of the programming mode selected (serial or parallel). It is not possible to read the offset values in serial fashion.

Figure 3, *Programmable Flag Offset Programming Sequence*, summaries the control pins and sequence for both serial and parallel programming modes. For a more detailed description, see discussion that follows.

The offset registers may be programmed (and reprogrammed) any time after Master Reset, regardless of whether serial or parallel programming has been selected. Valid programming ranges are from 0 to D-1.

TABLE 1 — DEFAULT PROGRAMMABLE FLAG OFFSETS

| IDT72T36135M | | | |
|------------------------------------------------------------------------------------------|-------|-------|-------------------------|
| * $\overline{\text{LD}}$ | FSEL1 | FSEL0 | Offsets n,m |
| H | L | L | 1,023 |
| L | H | L | 511 |
| L | L | H | 255 |
| L | L | L | 127 |
| L | H | H | 63 |
| H | H | L | 31 |
| H | L | H | 15 |
| H | H | H | 7 |
| * $\overline{\text{LD}}$ | FSEL1 | FSEL0 | Program Mode |
| H | X | X | Serial ⁽³⁾ |
| L | X | X | Parallel ⁽⁴⁾ |
| *THIS PIN MUST BE HIGH AFTER MASTER RESET TO WRITE OR READ DATA TO/FROM THE FIFO MEMORY. | | | |

NOTES:

1. n = empty offset for $\overline{\text{PAE}}[1:2]$.
2. m = full offset for $\overline{\text{PAF}}[1:2]$.
3. As well as selecting serial programming mode, one of the default values will also be loaded depending on the state of FSEL0 & FSEL1.
4. As well as selecting parallel programming mode, one of the default values will also be loaded depending on the state of FSEL0 & FSEL1.

SYNCHRONOUS vs ASYNCHRONOUS PROGRAMMABLE FLAG TIMING SELECTION

The IDT72T36135M can be configured during the Master Reset cycle with either synchronous or asynchronous timing for $\overline{\text{PAF}}[1:2]$ and $\overline{\text{PAE}}[1:2]$ flags by use of the PFM pin.

If synchronous $\overline{\text{PAF}}/\overline{\text{PAE}}[1:2]$ configuration is selected (PFM, HIGH during MRS), the PAF is asserted and updated on the rising edge of WCLK only and not RCLK. Similarly, $\overline{\text{PAE}}[1:2]$ is asserted and updated on the rising edge of RCLK only and not WCLK. For detail timing diagrams, see Figure 22 for synchronous $\overline{\text{PAF}}[1:2]$ timing and Figure 23 for synchronous $\overline{\text{PAE}}[1:2]$ timing.

If asynchronous $\overline{\text{PAF}}/\overline{\text{PAE}}[1:2]$ configuration is selected (PFM, LOW during MRS), the PAF is asserted LOW on the LOW-to-HIGH transition of WCLK and $\overline{\text{PAF}}[1:2]$ is reset to HIGH on the LOW-to-HIGH transition of RCLK. Similarly, $\overline{\text{PAE}}[1:2]$ is asserted LOW on the LOW-to-HIGH transition of RCLK. $\overline{\text{PAE}}[1:2]$ is reset to HIGH on the LOW-to-HIGH transition of WCLK. For detail timing diagrams, see Figure 24 for asynchronous $\overline{\text{PAF}}[1:2]$ timing and Figure 25 for asynchronous $\overline{\text{PAE}}[1:2]$ timing.

TABLE 2 — STATUS FLAGS FOR IDT STANDARD MODE

| Number of Words in FIFO | IDT72T36135M | FF | PAF | PAE | EF |
|--------------------------|--------------|----|-----|-----|----|
| | 0 | | H | H | L |
| 1 to n ⁽¹⁾ | | H | H | L | H |
| n + 1 to (524,288-(m+1)) | | H | H | H | H |
| (524,288-m) to 524,287 | | H | L | H | H |
| 524,288 | | L | L | H | H |

NOTE:

1. See Table 1 for values for n, m.

TABLE 3 — STATUS FLAGS FOR FWFT MODE

| Number of Words in FIFO | IDT72T36135M | IR | PAF | PAE | OR |
|--------------------------|--------------|----|-----|-----|----|
| | 0 | | L | H | L |
| 1 to n+1 | | L | H | L | L |
| n + 1 to (524,289-(m+1)) | | L | H | H | L |
| (524,289-m) to 524,288 | | L | L | H | L |
| 524,289 | | H | L | H | L |

NOTE:

1. See Table 1 for values for n, m.

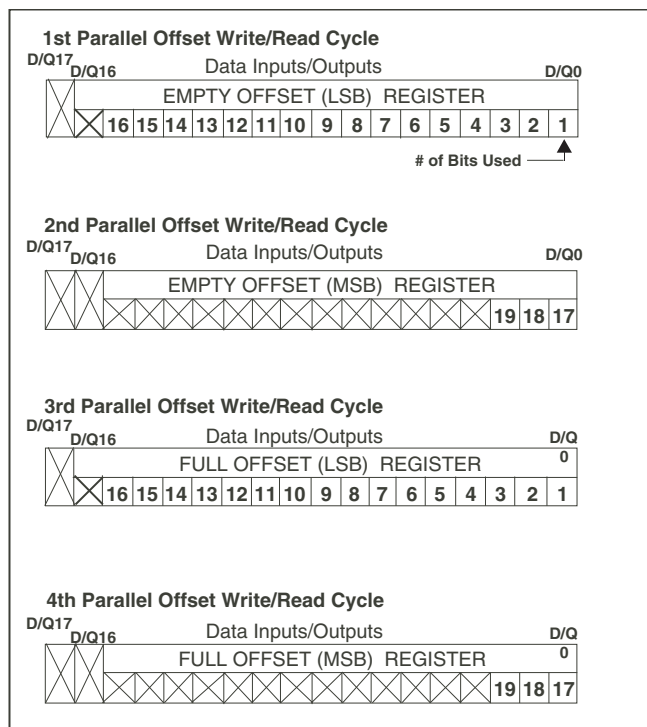
6723 drw07

| \overline{LD} | \overline{WEN} | \overline{REN} | \overline{SEN} | WCLK | RCLK | SCLK | IDT72T36135M |
|-----------------|------------------|------------------|------------------|------|------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0 | 0 | 1 | 1 | | X | X | Parallel write to registers: Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB) |
| 0 | 1 | 0 | 1 | X | | X | Parallel read from registers: Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB) |
| 0 | 1 | 1 | 0 | X | X | | Serial shift into registers: 38 bits for the IDT72T36135M 1 bit for each rising SCLK edge Starting with Empty Offset (LSB) Ending with Full Offset (MSB) |
| X | 1 | 1 | 1 | X | X | X | No Operation |
| 1 | 0 | X | X | | X | X | Write Memory |
| 1 | X | 0 | X | X | | X | Read Memory |
| 1 | 1 | 1 | X | X | X | X | No Operation |

6723 drw08

NOTES:

1. The programming method can only be selected at Master Reset.
2. Parallel reading of the offset registers is always permitted regardless of which programming method has been selected.
3. The programming sequence applies to both IDT Standard and FWFT modes.



6723 drw09

NOTE:

1. Consecutive reads of the offset registers is not permitted. The read operation must be disabled for a minimum of one RCLK cycle in between offset register accesses. (Please refer to Figure 21, *Parallel Read of Programmable Flag Registers (IDT Standard and FWFT Modes)* for more details).

Figure 3. Programmable Flag Offset Programming Sequence

SERIAL PROGRAMMING MODE

If Serial Programming mode has been selected, as described above, then programming of $\overline{\text{PAE}}[1:2]$ and $\overline{\text{PAF}}[1:2]$ values can be achieved by using a combination of the $\overline{\text{LD}}$, $\overline{\text{SEN}}$, SCLK and SI input pins. Programming $\overline{\text{PAE}}[1:2]$ and $\overline{\text{PAF}}[1:2]$ proceeds as follows: when $\overline{\text{LD}}$ and $\overline{\text{SEN}}$ are set LOW, data on the SI input are written, one bit for each SCLK rising edge, starting with the Empty Offset LSB and ending with the Full Offset MSB. 38 bits total required. See Figure 19, *Serial Loading of Programmable Flag Registers*, for the timing diagram for this mode.

Using the serial method, individual registers cannot be programmed selectively. $\overline{\text{PAE}}[1:2]$ and $\overline{\text{PAF}}[1:2]$ can show a valid status only after the complete set of bits (for all offset registers) has been entered. The registers can be reprogrammed as long as the complete set of new offset bits is entered. When $\overline{\text{LD}}$ is LOW and $\overline{\text{SEN}}$ is HIGH, no serial write to the registers can occur.

Write operations to the FIFO are allowed before and during the serial programming sequence. In this case, the programming of all offset bits does not have to occur at once. A select number of bits can be written to the SI input and then, by bringing $\overline{\text{LD}}$ and $\overline{\text{SEN}}$ HIGH, data can be written to FIFO memory via D_n by toggling $\overline{\text{WEN}}$. When $\overline{\text{WEN}}$ is brought HIGH with $\overline{\text{LD}}$ and $\overline{\text{SEN}}$ restored to a LOW, the next offset bit in sequence is written to the registers via SI. If an interruption of serial programming is desired, it is sufficient either to set $\overline{\text{LD}}$ LOW and deactivate $\overline{\text{SEN}}$ or to set $\overline{\text{SEN}}$ LOW and deactivate $\overline{\text{LD}}$. Once $\overline{\text{LD}}$ and $\overline{\text{SEN}}$ are both restored to a LOW level, serial offset programming continues.

From the time serial programming has begun, neither programmable flag will be valid until the full set of bits required to fill all the offset registers has been written. Measuring from the rising SCLK edge that achieves the above criteria; $\overline{\text{PAF}}[1:2]$ will be valid after three more rising WCLK edges plus t_{PAF} , $\overline{\text{PAE}}[1:2]$ will be valid after the next three rising RCLK edges plus t_{PAE} .

It is only possible to read the flag offset values via the parallel output port Qn.

PARALLEL MODE

If Parallel Programming mode has been selected, as described above, then programming of $\overline{\text{PAE}}[1:2]$ and $\overline{\text{PAF}}[1:2]$ values can be achieved by using a combination of the $\overline{\text{LD}}$, WCLK, $\overline{\text{WEN}}$ and D_n input pins. Programming $\overline{\text{PAE}}[1:2]$ and $\overline{\text{PAF}}[1:2]$ proceeds as follows: $\overline{\text{LD}}$ and $\overline{\text{WEN}}$ must be set LOW. When programming the Offset Registers of the TeraSync FIFO's the number of programming cycles will be based on the bus width, the following rules apply:

4 enabled write cycles are required to program the offset registers, (2 per offset). Data on the inputs D_n are written into the Empty Offset Register on the first two LOW-to-HIGH transition of WCLK. Upon the third and fourth LOW-to-HIGH transition of WCLK, data are written into the Full Offset Register. See Figure 3, *Programmable Flag Offset Programming Sequence* for more details.

RETRANSMIT FROM MARK OPERATION

The Retransmit from Mark feature allows FIFO data to be read repeatedly starting at a user-selected position. The FIFO is first put into retransmit mode that will 'mark' a beginning word and also set a pointer that will prevent ongoing FIFO write operations from over-writing retransmit data. The retransmit data can be read repeatedly any number of times from the 'marked' position. The FIFO can be taken out of retransmit mode at any time to allow normal device operation. The 'mark' position can be selected any number of times, each selection over-

writing the previous mark location. Retransmit operation is available in both IDT standard and FWFT modes.

During IDT standard mode the FIFO is put into retransmit mode by a Low-to-High transition on RCLK when the 'MARK' input is HIGH and $\overline{\text{EF}}[1:2]$ is HIGH. The rising RCLK edge 'marks' the data present in the FIFO output register as the first retransmit data. The FIFO remains in retransmit mode until a rising edge on RCLK occurs while MARK is LOW.

Once a 'marked' location has been set (and the device is still in retransmit mode, MARK is HIGH), a retransmit can be initiated by a rising edge on RCLK while the retransmit input ($\overline{\text{RT}}$) is LOW. $\overline{\text{REN}}$ must be HIGH (reads disabled) before bringing $\overline{\text{RT}}$ LOW. The device indicates the start of retransmit setup by setting $\overline{\text{EF}}[1:2]$ LOW, also preventing reads. When $\overline{\text{EF}}[1:2]$ goes HIGH, retransmit setup is complete and read operations may begin starting with the first data at the MARK location. Since IDT standard mode is selected, every word read including the first 'marked' word following a retransmit setup requires a LOW on $\overline{\text{REN}}$ (read enabled).

Note, write operations may continue as normal during all retransmit functions, however write operations to the 'marked' location will be prevented. See Figure 17, *Retransmit from Mark (IDT standard mode)*, for the relevant timing diagram.

During FWFT mode the FIFO is put into retransmit mode by a rising RCLK edge when the 'MARK' input is HIGH and $\overline{\text{OR}}[1:2]$ is LOW. The rising RCLK edge 'marks' the data present in the FIFO output register as the first retransmit data. The FIFO remains in retransmit mode until a rising RCLK edge occurs while MARK is LOW.

Once a marked location has been set (and the device is still in retransmit mode, MARK is HIGH), a retransmit can be initiated by a rising RCLK edge while the retransmit input ($\overline{\text{RT}}$) is LOW. $\overline{\text{REN}}$ must be HIGH (reads disabled) before bringing $\overline{\text{RT}}$ LOW. The device indicates the start of retransmit setup by setting $\overline{\text{OR}}[1:2]$ HIGH.

When $\overline{\text{OR}}[1:2]$ goes LOW, retransmit setup is complete and on the next rising RCLK edge after retransmit setup is complete, ($\overline{\text{RT}}$ goes HIGH), the contents of the first retransmit location are loaded onto the output register. Since FWFT mode is selected, the first word appears on the outputs regardless of $\overline{\text{REN}}$, a LOW on $\overline{\text{REN}}$ is not required for the first word. Reading all subsequent words requires a LOW on $\overline{\text{REN}}$ to enable the rising RCLK edge. See Figure 18, *Retransmit from Mark timing (FWFT mode)*, for the relevant timing diagram.

Note, there must be a minimum of 128 words of data between the write pointer and read pointer when the MARK is asserted. Also, once the MARK is set, the write pointer will not increment past the "marked" location until the MARK is deasserted. This prevents "overwriting" of retransmit data.

HSTL/LVTTL I/O

Both the write port and read port are user selectable between HSTL or LVTTL I/O, via two select pins, WHSTL and RHSTL respectively. All other control pins are selectable via SHSTL, see Table 4 for details of groupings.

Note, that when the write port is selected for HSTL mode, the user can reduce the power consumption (in stand-by mode by utilizing the $\overline{\text{WCS}}$ input).

All "Static Pins" must be tied to VCC or GND. These pins are LVTTL only, and are purely device configuration pins.

TABLE 4 — I/O CONFIGURATION

| WHSTL SELECT | RHSTL SELECT | | SHSTL SELECT | | STATIC PINS | |
|-----------------------------------------------------|-------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------|--------------------------------------|---------------------------------------------------------|-------------------------------------------------------|
| WHSTL: HIGH = HSTL LOW = LVTTTL | RHSTL: HIGH = HSTL LOW = LVTTTL | | SHSTL: HIGH = HSTL LOW = LVTTTL | | LVTTTL ONLY | |
| Dn (I/P) WCLK/WR (I/P) WEN (I/P) WCS (I/P) | RCLK/RD (I/P) RCS (I/P) MARK (I/P) REN (I/P) OE (I/P) RT (I/P) Qn (O/P) | EF/OR[1:2] (O/P) PAF[1:2] (O/P) PAE[1:2] (O/P) FF/IR[1:2] (O/P) TDO (O/P) | SCLK (I/P) LD (I/P) MRS (I/P) TCK (I/P) TMS (I/P) SEN (I/P) FWFT/SI (I/P) | PRS (I/P) TRST (I/P) TDI (I/P) | ASYR (I/P) FSEL1 (I/P) SHSTL (I/P) RHSTL (I/P) | ASYW (I/P) FSEL0 (I/P) PFM (I/P) WHSTL (I/P) |

SIGNAL DESCRIPTION

INPUTS:

DATA IN (D₀ - D_n)

Data inputs for 36-bit wide data (D₀ - D₃₅).

CONTROLS:

MASTER RESET (\overline{MRS})

A Master Reset is accomplished whenever the \overline{MRS} input is taken to a LOW state. This operation sets the internal read and write pointers to the first location of the RAM array. PAE[1:2] will go LOW, PAF[1:2] will go HIGH.

If FWFT/SI is LOW during Master Reset then the IDT Standard mode, along with EF[1:2] and FF[1:2] are selected. EF[1:2] will go LOW and FF[1:2] will go HIGH. If FWFT/SI is HIGH, then the First Word Fall Through mode (FWFT), along with IR[1:2] and OR[1:2], are selected. OR[1:2] will go HIGH and IR[1:2] will go LOW.

All control settings such as RM and PFM are defined during the Master Reset cycle.

During a Master Reset, the output register is initialized to all zeroes. A Master Reset is required after power up, before a write operation can take place. \overline{MRS} is asynchronous.

See Figure 8, *Master Reset Timing*, for the relevant timing diagram.

PARTIAL RESET (\overline{PRS})

A Partial Reset is accomplished whenever the \overline{PRS} input is taken to a LOW state. As in the case of the Master Reset, the internal read and write pointers are set to the first location of the RAM array, PAE[1:2] goes LOW, PAF[1:2] goes HIGH.

Whichever mode is active at the time of Partial Reset, IDT Standard mode or First Word Fall Through, that mode will remain selected. If the IDT Standard mode is active, then FF[1:2] will go HIGH and EF[1:2] will go LOW. If the First Word Fall Through mode is active, then OR[1:2] will go HIGH, and IR[1:2] will go LOW.

Following Partial Reset, all values held in the offset registers remain unchanged. The programming method (parallel or serial) currently active at the time of Partial Reset is also retained. The output register is initialized to all zeroes. \overline{PRS} is asynchronous.

A Partial Reset is useful for resetting the device during the course of operation, when reprogramming programmable flag offset settings may not be convenient.

See Figure 9, *Partial Reset Timing*, for the relevant timing diagram.

ASYNCHRONOUS WRITE (\overline{ASYW})

The write port can be configured for either Synchronous or Asynchronous mode of operation. If during Master Reset the \overline{ASYW} input is LOW, then Asynchronous operation of the write port will be selected. During Asynchronous operation of the write port the WCLK input becomes WR input, this is the Asynchronous write strobe input. A rising edge on WR will write data present on the D_n inputs into the FIFO. (\overline{WEN} must be tied LOW when using the write port in Asynchronous mode).

When the write port is configured for Asynchronous operation the full flag (FF[1:2]) operates in an asynchronous manner, that is, the full flag will be updated based in both a write operation and read operation. Note, if Asynchronous mode is selected, FWFT is not permissible. Refer to Figures 26, 27, 30 and 31 for relevant timing and operational waveforms.

ASYNCHRONOUS READ (\overline{ASYR})

The read port can be configured for either Synchronous or Asynchronous mode of operation. If during a Master Reset the \overline{ASYR} input is LOW, then Asynchronous operation of the read port will be selected. During Asynchronous operation of the read port the RCLK input becomes RD input, this is the Asynchronous read strobe input. A rising edge on RD will read data from the FIFO via the output register and Q_n port. (\overline{REN} must be tied LOW during Asynchronous operation of the read port).

The \overline{OE} input provides three-state control of the Q_n output bus, in an asynchronous manner. (\overline{RCS} , provides three-state control of the read port in Synchronous mode).

When the read port is configured for Asynchronous operation the device must be operating on IDT standard mode, FWFT mode is not permissible if the read port is Asynchronous. The Empty Flag (\overline{EF} [1:2]) operates in an Asynchronous manner, that is, the empty flag will be updated based on both a read operation and a write operation. Refer to figures 28, 29, 30 and 31 for relevant timing and operational waveforms.

RETRANSMIT (\overline{RT})

The Retransmit (\overline{RT}) input is used in conjunction with the MARK input, together they provide a means by which data previously read out of the FIFO can be reread any number of times. If retransmit operation has been selected (i.e. the MARK input is HIGH), a rising edge on RCLK while \overline{RT} is LOW will reset the read pointer back to the memory location set by the user via the MARK input.

If IDT standard mode has been selected the \overline{EF} [1:2] flag will go LOW and remain LOW for the time that \overline{RT} is held LOW. \overline{RT} can be held LOW for any number of RCLK cycles, the read pointer being reset to the marked location. The next rising edge of RCLK after \overline{RT} has returned HIGH, will cause \overline{EF} [1:2] to go HIGH, allowing read operations to be performed on the FIFO. The next read operation will access data from the 'marked' memory location.

Subsequent retransmit operations may be performed, each time the read pointer returning to the 'marked' location. See Figure 17, *Retransmit from Mark (IDT Standard mode)* for the relevant timing diagram.

If FWFT mode has been selected the \overline{OR} [1:2] flag will go HIGH and remain HIGH for the time that \overline{RT} is held LOW. \overline{RT} can be held LOW for any number of RCLK cycles, the read pointer being reset to the 'marked' location. The next RCLK rising edge after \overline{RT} has returned HIGH, will cause \overline{OR} [1:2] to go LOW and due to FWFT operation, the contents of the marked memory location will be loaded onto the output register, a read operation being required for all subsequent data reads.

Subsequent retransmit operations may be performed each time the read pointer returning to the 'marked' location. See Figure 18, *Retransmit from Mark (FWFT mode)* for the relevant timing diagram.

MARK

The MARK input is used to select Retransmit mode of operation. An RCLK rising edge while MARK is HIGH will mark the memory location of the data currently present on the output register, the device will also be placed into retransmit mode. For the IDT72T36135M a minimum of 128 words (x36). Also, once the MARK is set, the write pointer will not increment past the "marked" location until the MARK is deasserted. This prevents "overwriting" of retransmit data.

The MARK input must remain HIGH during the whole period of retransmit mode, a falling edge of RCLK while MARK is LOW will take the device out of retransmit mode and into normal mode. Any number of MARK locations can be set during FIFO operation, only the last marked location taking effect. Once a

mark location has been set the write pointer cannot be incremented past this marked location. During retransmit mode write operations to the device may continue without hindrance.

FIRST WORD FALL THROUGH/SERIAL IN (FWFT/SI)

This is a dual purpose pin. During Master Reset, the state of the FWFT/SI input determines whether the device will operate in IDT Standard mode or First Word Fall Through (FWFT) mode.

If, at the time of Master Reset, FWFT/SI is LOW, then IDT Standard mode will be selected. This mode uses the Empty Flag ($\overline{EF}[1:2]$) to indicate whether or not there are any words present in the FIFO memory. It also uses the Full Flag function ($\overline{FF}[1:2]$) to indicate whether or not the FIFO memory has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using the Read Enable (\overline{REN}) and RCLK.

If, at the time of Master Reset, FWFT/SI is HIGH, then FWFT mode will be selected. This mode uses Output Ready ($\overline{OR}[1:2]$) to indicate whether or not there is valid data at the data outputs (Q_n). It also uses Input Ready ($\overline{IR}[1:2]$) to indicate whether or not the FIFO memory has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to Q_n after three RCLK rising edges, $\overline{REN} = \text{LOW}$ is not necessary. Subsequent words must be accessed using the Read Enable (\overline{REN}) and RCLK.

After Master Reset, FWFT/SI acts as a serial input for loading $\overline{PAE}[1:2]$ and $\overline{PAF}[1:2]$ offsets into the programmable registers. The serial input function can only be used when the serial loading method has been selected during Master Reset. Serial programming using the FWFT/SI pin functions the same way in both IDT Standard and FWFT modes.

WRITE STROBE & WRITE CLOCK (WR/WCLK)

If Synchronous operation of the write port has been selected via \overline{ASYW} , this input behaves as WCLK.

A write cycle is initiated on the rising edge of the WCLK input. Data setup and hold times must be met with respect to the LOW-to-HIGH transition of the WCLK. It is permissible to stop the WCLK. Note that while WCLK is idle, the $\overline{FF}/\overline{IR}[1:2]$, and $\overline{PAF}[1:2]$ flags will not be updated. The Write and Read Clocks can either be independent or coincident.

If Asynchronous operation has been selected this input is WR (write strobe). Data is Asynchronously written into the FIFO via the D_n inputs whenever there is a rising edge on WR. In this mode the WEN input must be tied LOW.

WRITE ENABLE (\overline{WEN})

When the \overline{WEN} input is LOW, data may be loaded into the FIFO RAM array on the rising edge of every WCLK cycle if the device is not full. Data is stored in the RAM array sequentially and independently of any ongoing read operation.

When \overline{WEN} is HIGH, no new data is written in the RAM array on each WCLK cycle.

To prevent data overflow in the IDT Standard mode, $\overline{FF}[1:2]$ will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{FF}[1:2]$ will go HIGH allowing a write to occur. The $\overline{FF}[1:2]$ is updated by two WCLK cycles + t_{SKEW} after the RCLK cycle.

To prevent data overflow in the FWFT mode, $\overline{IR}[1:2]$ will go HIGH, inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{IR}[1:2]$ will go LOW allowing a write to occur. The $\overline{IR}[1:2]$ flag is updated by two WCLK cycles + t_{SKEW} after the valid RCLK cycle.

\overline{WEN} is ignored when the FIFO is full in either FWFT or IDT Standard mode.

If Asynchronous operation of the write port has been selected, then \overline{WEN} must be held active, (tied LOW).

READ STROBE & READ CLOCK (RD/RCLK)

If Synchronous operation of the read port has been selected via \overline{ASYR} , this input behaves as RCLK. A read cycle is initiated on the rising edge of the RCLK input. Data can be read on the outputs, on the rising edge of the RCLK input. It is permissible to stop the RCLK. Note that while RCLK is idle, the $\overline{EF}/\overline{OR}[1:2]$, and $\overline{PAE}[1:2]$ flags will not be updated. The Write and Read Clocks can be independent or coincident.

If Asynchronous operation has been selected this input is RD (Read Strobe). Data is Asynchronously read from the FIFO via the output register whenever there is a rising edge on RD. In this mode the \overline{REN} and \overline{RCS} inputs must be tied LOW. The \overline{OE} input is used to provide Asynchronous control of the three-state Q_n outputs.

WRITE CHIP SELECT (\overline{WCS})

The \overline{WCS} disables all Write Port inputs (data only) if it is held HIGH. To perform normal operations on the write port, the \overline{WCS} must be enabled, held LOW.

READ ENABLE (\overline{REN})

When Read Enable is LOW, data is loaded from the RAM array into the output register on the rising edge of every RCLK cycle if the device is not empty.

When the \overline{REN} input is HIGH, the output register holds the previous data and no new data is loaded into the output register. The data outputs Q_0 - Q_n maintain the previous data value.

In the IDT Standard mode, every word accessed at Q_n , including the first word written to an empty FIFO, must be requested using \overline{REN} provided that \overline{RCS} is LOW. When the last word has been read from the FIFO, the Empty Flag ($\overline{EF}[1:2]$) will go LOW, inhibiting further read operations. \overline{REN} is ignored when the FIFO is empty. Once a write is performed, $\overline{EF}[1:2]$ will go HIGH allowing a read to occur. The $\overline{EF}[1:2]$ flag is updated by two RCLK cycles + t_{SKEW} after the valid WCLK cycle. Both \overline{RCS} and \overline{REN} must be active, LOW for data to be read out on the rising edge of RCLK.

In the FWFT mode, the first word written to an empty FIFO automatically goes to the outputs Q_n , on the third valid LOW-to-HIGH transition of RCLK + t_{SKEW} after the first write. \overline{REN} and \overline{RCS} do not need to be asserted LOW for the First Word to fall through to the output register. In order to access all other words, a read must be executed using \overline{REN} and \overline{RCS} . The RCLK LOW-to-HIGH transition after the last word has been read from the FIFO, Output Ready ($\overline{OR}[1:2]$) will go HIGH with a true read (RCLK with $\overline{REN} = \text{LOW}; \overline{RCS} = \text{LOW}$), inhibiting further read operations. \overline{REN} is ignored when the FIFO is empty.

If Asynchronous operation of the Read port has been selected, then \overline{REN} must be held active, (tied LOW).

SERIAL ENABLE (\overline{SEN})

The \overline{SEN} input is an enable used only for serial programming of the offset registers. The serial programming method must be selected during Master Reset. \overline{SEN} is always used in conjunction with \overline{LD} . When these lines are both LOW, data at the SI input can be loaded into the program register one bit for each LOW-to-HIGH transition of SCLK.

When \overline{SEN} is HIGH, the programmable registers retains the previous settings and no offsets are loaded. \overline{SEN} functions the same way in both IDT Standard and FWFT modes.

OUTPUT ENABLE (\overline{OE})

When Output Enable is enabled (LOW), the parallel output buffers receive data from the output register. When \overline{OE} is HIGH, the output data bus (Q_n) goes into a high impedance state. During Master or a Partial Reset the \overline{OE} is the only input that can place the output bus Q_n , into High-Impedance. During Reset the \overline{RCS} input can be HIGH or LOW, it has no effect on the Q_n outputs.

READ CHIP SELECT (\overline{RCS})

The Read Chip Select input provides synchronous control of the Read output port. When \overline{RCS} goes LOW, the next rising edge of RCLK causes the Qn outputs to go to the Low-Impedance state. When \overline{RCS} goes HIGH, the next RCLK rising edge causes the Qn outputs to return to HIGH Z. During a Master or Partial Reset the \overline{RCS} input has no effect on the Qn output bus, \overline{OE} is the only input that provides High-Impedance control of the Qn outputs. If \overline{OE} is LOW the Qn data outputs will be Low-Impedance regardless of \overline{RCS} until the first rising edge of RCLK after a Reset is complete. Then if \overline{RCS} is HIGH the data outputs will go to High-Impedance.

The \overline{RCS} input does not effect the operation of the flags. For example, when the first word is written to an empty FIFO, the $\overline{EF}[1:2]$ will still go from LOW to HIGH based on a rising edge of RCLK, regardless of the state of the \overline{RCS} input.

Also, when operating the FIFO in FWFT mode the first word written to an empty FIFO will still be clocked through to the output register based on RCLK, regardless of the state of \overline{RCS} . For this reason the user must take care when a data word is written to an empty FIFO in FWFT mode. If \overline{RCS} is disabled when an empty FIFO is written into, the first word will fall through to the output register, but will not be available on the Qn outputs which are in HIGH-Z. The user must take \overline{RCS} active LOW to access this first word, place the output bus in LOW-Z. \overline{REN} must remain disabled HIGH for at least one cycle after \overline{RCS} has gone LOW. A rising edge of RCLK with \overline{RCS} and \overline{REN} active LOW, will read out the next word. Care must be taken so as not to lose the first word written to an empty FIFO when \overline{RCS} is HIGH. Refer to Figure 16, **\overline{RCS} and \overline{REN} Read Operation (FWFT Mode)**. The \overline{RCS} pin must also be active (LOW) in order to perform a Retransmit. See Figure 12 for *Read Cycle and Read Chip Select Timing (IDT Standard Mode)*. See Figure 15 for *Read Cycle and Read Chip Select Timing (First Word Fall Through Mode)*.

If Asynchronous operation of the Read port has been selected, then \overline{RCS} must be held active, (tied LOW). \overline{OE} provides three-state control of Qn.

WRITE PORT HSTL SELECT (WHSTL)

The control inputs, data inputs and flag outputs associated with the write port can be setup to be either HSTL or LVTTTL. If WHSTL is HIGH during the Master Reset, then HSTL operation of the write port will be selected. If WHSTL is LOW at Master Reset, then LVTTTL will be selected.

The inputs and outputs associated with the write port are listed in Table 4, I/O Configuration.

READ PORT HSTL SELECT (RHSTL)

The control inputs, data inputs and flag outputs associated with the read port can be setup to be either HSTL or LVTTTL. If RHSTL is HIGH during the Master Reset, then HSTL operation of the read port will be selected. If RHSTL is LOW at Master Reset, then LVTTTL will be selected for the read port.

The inputs and outputs associated with the read port are listed in Table 4, I/O Configuration.

SYSTEM HSTL SELECT (SHSTL)

All inputs not associated with the write and read port can be setup to be either HSTL or LVTTTL. If SHSTL is HIGH during Master Reset, then HSTL operation of all the inputs not associated with the write and read port will be selected. If SHSTL is LOW at Master Reset, then LVTTTL will be selected. The inputs associated with SHSTL are listed in Table 4, I/O Configuration.

LOAD (\overline{LD})

This is a dual purpose pin. During Master Reset, the state of the \overline{LD} input, along with FSEL0 and FSEL1, determines one of eight default offset values for the $\overline{PAE}[1:2]$ and $\overline{PAF}[1:2]$ flags, along with the method by which these offset

registers can be programmed, parallel or serial (see Table 1). After Master Reset, \overline{LD} enables write operations to and read operations from the offset registers. Only the offset loading method currently selected can be used to write to the registers. Offset registers can be read only in parallel.

After Master Reset, the \overline{LD} pin is used to activate the programming process of the flag offset values $\overline{PAE}[1:2]$ and $\overline{PAF}[1:2]$. Pulling \overline{LD} LOW will begin a serial loading or parallel load or read of these offset values. THIS PIN MUST BE HIGH AFTER MASTER RESET TO WRITE OR READ DATA TO/FROM THE FIFO MEMORY.

PROGRAMMABLE FLAG MODE (PFM)

During Master Reset, a LOW on PFM will select Asynchronous Programmable flag timing mode. A HIGH on PFM will select Synchronous Programmable flag timing mode. If asynchronous $\overline{PAE}/\overline{PAF}[1:2]$ configuration is selected (PFM, LOW during \overline{MRS}), the $\overline{PAE}[1:2]$ is asserted LOW on the LOW-to-HIGH transition of RCLK. $\overline{PAE}[1:2]$ is reset to HIGH on the LOW-to-HIGH transition of WCLK. Similarly, the $\overline{PAF}[1:2]$ is asserted LOW on the LOW-to-HIGH transition of WCLK and $\overline{PAF}[1:2]$ is reset to HIGH on the LOW-to-HIGH transition of RCLK.

If synchronous $\overline{PAE}/\overline{PAF}[1:2]$ configuration is selected (PFM, HIGH during \overline{MRS}), the $\overline{PAE}[1:2]$ is asserted and updated on the rising edge of RCLK only and not WCLK. Similarly, $\overline{PAF}[1:2]$ is asserted and updated on the rising edge of WCLK only and not RCLK. The mode desired is configured during master reset by the state of the Programmable Flag Mode (PFM) pin.

OUTPUTS:**FULL FLAG ($\overline{FF}/\overline{IR}[1:2]$)**

This is a dual purpose pin. In IDT Standard mode, the Full Flag ($\overline{FF}[1:2]$) function is selected. When the FIFO is full, $\overline{FF}[1:2]$ will go LOW, inhibiting further write operations. When $\overline{FF}[1:2]$ is HIGH, the FIFO is not full. If no reads are performed after a reset (either \overline{MRS} or \overline{PRS}), $\overline{FF}[1:2]$ will go LOW after D writes to the FIFO (D = 524,288 for the IDT72T36135M). See Figure 10, *Write Cycle and Full Flag Timing (IDT Standard Mode)*, for the relevant timing information. Please see Flagging section for external gating instructions of these flags.

In FWFT mode, the Input Ready ($\overline{IR}[1:2]$) function is selected. $\overline{IR}[1:2]$ goes LOW when memory space is available for writing in data. When there is no longer any free space left, $\overline{IR}[1:2]$ goes HIGH, inhibiting further write operations. If no reads are performed after a reset (either \overline{MRS} or \overline{PRS}), $\overline{IR}[1:2]$ will go HIGH after D writes to the FIFO (D = 524,288 for the IDT72T36135M). See Figure 13, *Write Timing (FWFT Mode)*, for the relevant timing information.

The $\overline{IR}[1:2]$ status not only measures the contents of the FIFO memory, but also counts the presence of a word in the output register. Thus, in FWFT mode, the total number of writes necessary to deassert $\overline{IR}[1:2]$ is one greater than needed to assert $\overline{FF}[1:2]$ in IDT Standard mode.

$\overline{FF}/\overline{IR}[1:2]$ is synchronous and updated on the rising edge of WCLK. $\overline{FF}/\overline{IR}[1:2]$ are double register-buffered outputs.

Note, when the device is in Retransmit mode, this flag is a comparison of the write pointer to the 'marked' location. This differs from normal mode where this flag is a comparison of the write pointer to the read pointer.

EMPTY FLAG ($\overline{EF}/\overline{OR}[1:2]$)

This is a dual purpose pin. In the IDT Standard mode, the Empty Flag ($\overline{EF}[1:2]$) function is selected. When the FIFO is empty, $\overline{EF}[1:2]$ will go LOW, inhibiting further read operations. When $\overline{EF}[1:2]$ is HIGH, the FIFO is not empty. See Figure 11, *Read Cycle, Empty Flag and First Word Latency Timing (IDT Standard Mode)*, for the relevant timing information. Please see Flagging section for external gating instructions of these flags.

In FWFT mode, the Output Ready ($\overline{OR}[1:2]$) function is selected. $\overline{OR}[1:2]$ goes LOW at the same time that the first word written to an empty FIFO appears valid on the outputs. $\overline{OR}[1:2]$ stays LOW after the RCLK LOW to HIGH transition that shifts the last word from the FIFO memory to the outputs. $\overline{OR}[1:2]$ goes HIGH only with a true read (RCLK with $\overline{REN} = \text{LOW}$). The previous data stays at the outputs, indicating the last word was read. Further data reads are inhibited until $\overline{OR}[1:2]$ goes LOW again. See Figure 14, *Read Timing (FWFT Mode)*, for the relevant timing information.

$\overline{EF}/\overline{OR}[1:2]$ is synchronous and updated on the rising edge of RCLK.

In IDT Standard mode, $\overline{EF}[1:2]$ is a double register-buffered output. In FWFT mode, $\overline{OR}[1:2]$ is a triple register-buffered output.

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}[1:2]$)

The Programmable Almost-Full flag ($\overline{PAF}[1:2]$) will go LOW when the FIFO reaches the almost-full condition. In IDT Standard mode, if no reads are performed after reset (\overline{MRS}), $\overline{PAF}[1:2]$ will go LOW after (D - m) words are written to the FIFO. The $\overline{PAF}[1:2]$ will go LOW after (524,288-m) writes for the IDT72T36135M. The offset “m” is the full offset value. The default setting for this value is stated in the footnote of Table 2, Status Flags for IDT Standard Mode. Please see Flagging section for external gating instructions of these flags.

In FWFT mode, the $\overline{PAF}[1:2]$ will go LOW after (524,289-m) writes for the IDT72T36135M, where m is the full offset value. The default setting for this value is stated in Table 3, Status Flags for FWFT Mode.

See Figure 22, *Synchronous Programmable Almost-Full Flag Timing (IDT Standard and FWFT Mode)*, for the relevant timing information.

If asynchronous $\overline{PAF}[1:2]$ configuration is selected, the $\overline{PAF}[1:2]$ is asserted LOW on the LOW-to-HIGH transition of the Write Clock (WCLK). $\overline{PAF}[1:2]$ is reset to HIGH on the LOW-to-HIGH transition of the Read Clock (RCLK). If synchronous $\overline{PAF}[1:2]$ configuration is selected, the $\overline{PAF}[1:2]$ is updated on the rising edge of WCLK. See Figure 24, *Asynchronous Almost-Full Flag Timing (IDT Standard and FWFT Mode)*.

Note, when the device is in Retransmit mode, this flag is a comparison of the write pointer to the ‘marked’ location. This differs from normal mode where this flag is a comparison of the write pointer to the read pointer.

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}[1:2]$)

The Programmable Almost-Empty flag ($\overline{PAE}[1:2]$) will go LOW when the FIFO reaches the almost-empty condition. In IDT Standard mode, $\overline{PAE}[1:2]$ will go LOW when there are n words or less in the FIFO. The offset “n” is the empty offset value. The default setting for this value is stated in the footnote of Table 1. Please see Flagging section for external gating instructions of these flags.

In FWFT mode, the $\overline{PAE}[1:2]$ will go LOW when there are n+1 words or less in the FIFO. The default setting for this value is stated in Table 1.

See Figure 23, *Synchronous Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Mode)*, for the relevant timing information.

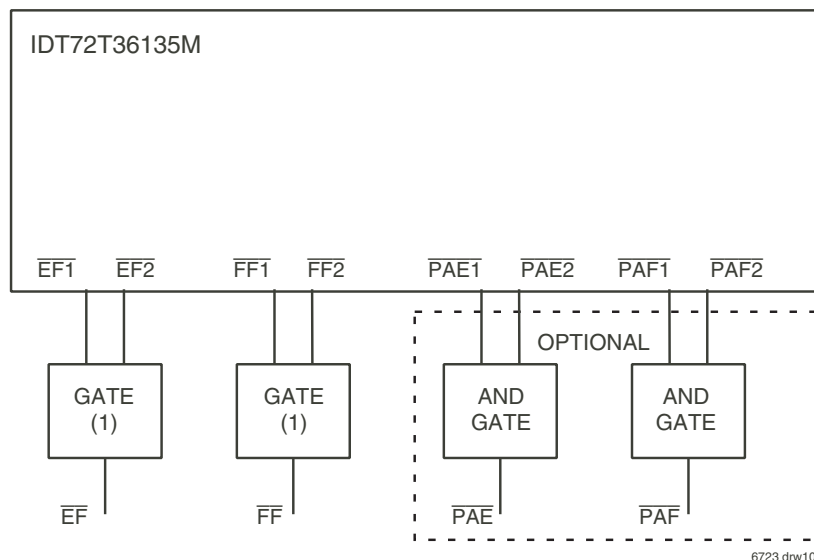
If asynchronous $\overline{PAE}[1:2]$ configuration is selected, the $\overline{PAE}[1:2]$ is asserted LOW on the LOW-to-HIGH transition of the Read Clock (RCLK). $\overline{PAE}[1:2]$ is reset to HIGH on the LOW-to-HIGH transition of the Write Clock (WCLK). If synchronous $\overline{PAE}[1:2]$ configuration is selected, the $\overline{PAE}[1:2]$ is updated on the rising edge of RCLK. See Figure 25, *Asynchronous Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Mode)*.

CONSIDERATIONS FOR READING FLAG OUTPUTS

On this device, there are two sets of flagging outputs for the empty flag ($\overline{EF1}$ & $\overline{EF2}$), full flag ($\overline{FF1}$ & $\overline{FF2}$), Programmable Almost Empty Flag (PAE1 & PAE2), and Programmable Almost Full Flag (PAF1 & PAF2) the user must work with in order to be able to correctly read the status of each flag. Since this device is a multi-chip module (MCM), both die’s flags must be read accordingly to avoid skewing problems between the two internal die.

To remedy this function, the user must tie together $\overline{FF1}$ & $\overline{FF2}$, and $\overline{EF1}$ & $\overline{EF2}$ flag outputs to an external gate from a neighboring programmable device such as an FPGA or PLD and read from the output of the logical gate. An OR

gate is used for FWFT mode and an AND gate is used for IDT mode. This must be done to avoid timing skew problems between the two sets of flags. For the PAE[1:2] and PAF[1:2] active low output flags, the user has the option to leave the PAE[1:2] and PAF[1:2] as is and use both pins at different programmable water marks for measuring buffer status. Please see the section on Parallel Programming Mode to understand how to program these two sets of flags as different water marks in Functional Description section of the datasheet. This gives added flexibility for queue management. Below is an example diagram for how this is accomplished.



NOTE:
1. An “OR” Gate is used for FWFT mode, and an “AND” Gate is used for IDT Standard mode.

Figure 4. Output Flag Gating Considerations

PIN COMPATIBILITY WITH 9M TERASYNC (IDT72T36125) CONSIDERATIONS

The IDT72T36135M can be a drop and replacement for the 9M TeraSync (IDT72T36125) if specific pin changes are made to the 18M FIFO. Since the 18M TeraSync is a Multi-Chip Module (MCM), containing two 9M TeraSyncs (IDT72T18125) in width expansion mode, certain functionality can not be offered in the 18M TeraSync such as bus matching, single flag outputs and

interspersed parity. From these changes, the 18M FIFO has removed specific inputs such as IW, OW, BM, BE, IP, while also gaining another set of output flags as specified in **Considerations for Reading Flag Outputs** which are $\overline{EF2}$, $\overline{FF2}$, PAE2, and PAF2.

To maintain drop-in replacement compatibility for the 18M TeraSync, the pin changes on the pin diagram for the 18M TeraSync FIFO from the 9M TeraSync FIFO have been identified, and listed in the table below.

TABLE 5 — PIN CHANGES BETWEEN 9M TERASYNC AND 18M TERASYNC

| 9M TeraSync FIFO (IDT72T36125) pins changed | 18M TeraSync FIFO (IDT72T36135M) new pins |
|------------------------------------------------|----------------------------------------------|
| BM | $\overline{EF2}$ |
| IP | $\overline{PAE2}$ |
| IW | NC (No Connect) |
| OW | NC (No Connect) |
| HF | $\overline{PAF2}$ |
| EREN | $\overline{FF2}$ |
| ERCLK | NC (No Connect) |
| BE | GND |

NOTES:
1. Internally, the 9M pins on the left side of the table will be tied to the GND or VDD plane, respectively in the 18M device.
2. Please see IDT72T36125 TeraSync FIFO datasheet for additional features listed.

JTAG FUNCTIONALITY AND CONFIGURATION

The IDT72T36135M is composed of two independent memory arrays, and thus cannot be treated as a single JTAG device in the scan chain. The two arrays (A and B) each have identical characteristics and commands but must be treated as separate entities in JTAG operations. Please refer to Figure 5, *JTAG Configuration for IDT72T36135M*.

JTAG signaling must be provided serially to each array and utilize the information provided in the Scan Register Descriptions, JTAG Instruction Description. Specifically, commands for Array B must precede those Array A in any JTAG operations sent to the IDT72T36135M. Please reference Application Note AN-411, "JTAG Testing of Multichip Modules" for specific instructions on performing JTAG testing on the IDT72T36135M. AN-411 is available at www.idt.com.

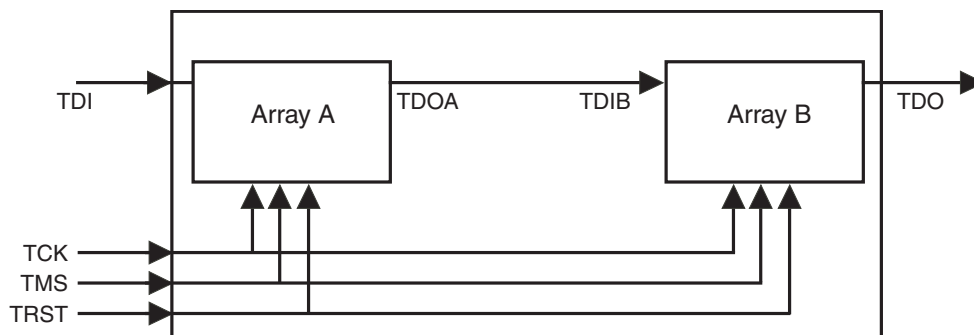
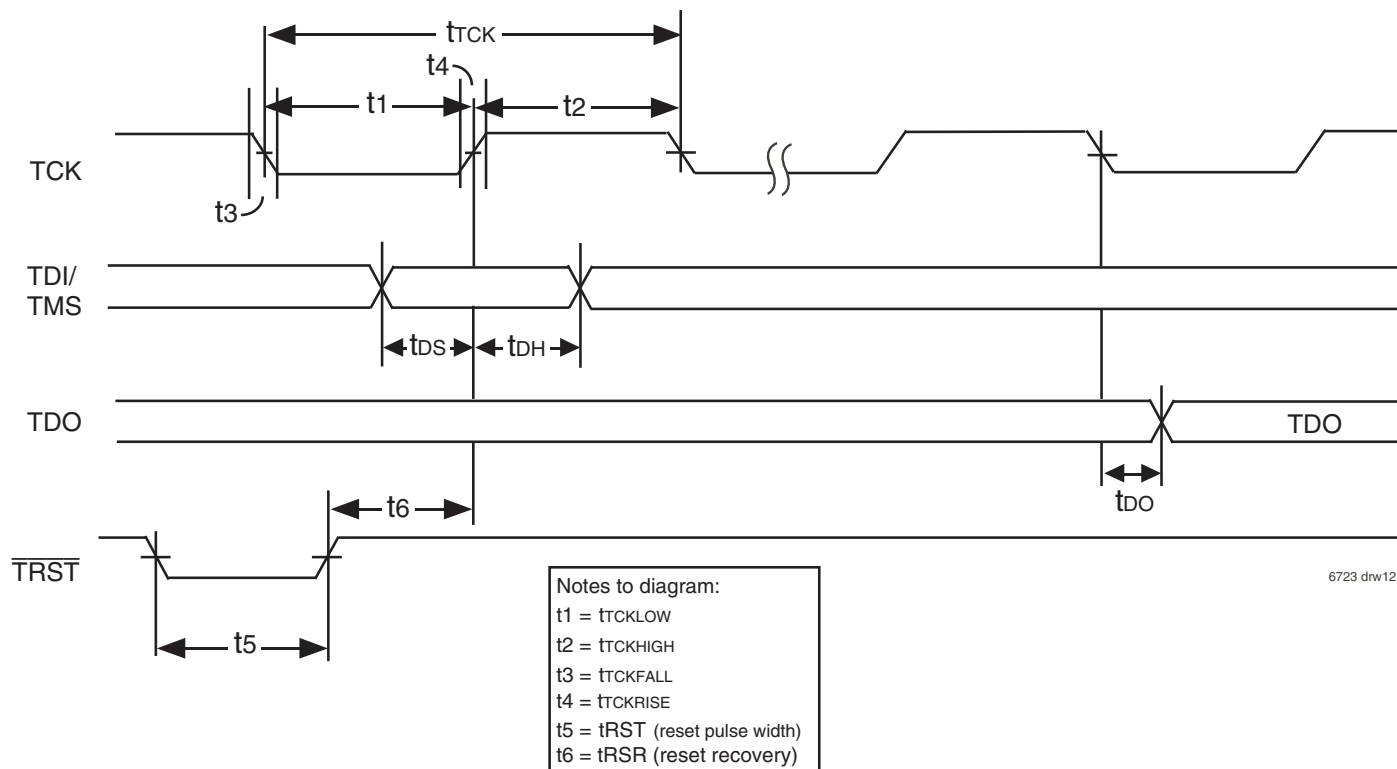


Figure 5. JTAG Configuration for IDT72T36135M

JTAG TIMING SPECIFICATION



6723 drw12

SYSTEM INTERFACE PARAMETERS

| Parameter | Symbol | Test Conditions | IDT72T36135M | | |
|------------------|---------------------|-----------------|--------------|------|-------|
| | | | Min. | Max. | Units |
| Data Output | tDO ⁽¹⁾ | | - | 20 | ns |
| Data Output Hold | tDOH ⁽¹⁾ | | 0 | - | ns |
| Data Input | tDS | trise=3ns | 10 | - | ns |
| | tDH | tfall=3ns | 10 | - | ns |

NOTE:

1. 50pf loading on external output signals.

JTAG AC ELECTRICAL CHARACTERISTICS

(Vcc = 2.5V ± 5%; Tcase = 0°C to +85°C)

| Parameter | Symbol | Test Conditions | IDT72T36135M | | |
|-------------------------|----------|-----------------|--------------|------------------|-------|
| | | | Min. | Max. | Units |
| JTAG Clock Input Period | tTCK | - | 100 | - | ns |
| JTAG Clock HIGH | tTCKHIGH | - | 40 | - | ns |
| JTAG Clock Low | tTCKLOW | - | 40 | - | ns |
| JTAG Clock Rise Time | tTCKRISE | - | - | 5 ⁽¹⁾ | ns |
| JTAG Clock Fall Time | tTCKFALL | - | - | 5 ⁽¹⁾ | ns |
| JTAG Reset | tTRST | - | 50 | - | ns |
| JTAG Reset Recovery | tRSR | - | 50 | - | ns |

NOTE:

1. Guaranteed by design.