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73M1903C
Modem Analog Front End

Simplifying System Integration™

DATA SHEET

DS_1903C_033

March 2010

DESCRIPTION

The 73M1903C Analog Front End (AFE) IC includes fully differential hybrid driver outputs, which connect to the telephone line interface through a transformer-based DAA. The receive pins are also fully differential for maximum flexibility and performance. This arrangement allows for the design of a high performance hybrid circuit to improve signal to noise performance under low receive level conditions, and compatibility with any standard transformer intended for PSTN communications applications.

The device incorporates a programmable sample rate circuit to support soft modem and DSP based implementations of all speeds up to V.92 (56 kbps). The sampling rates supported are from 7.2 kHz to 16.0 kHz by programming the pre-scaler NCO and the PLL NCO.

The 73M1903C device incorporates a digital host interface that is compatible with the serial ports found on most commercially available DSPs and processors and exchanges both payload and control information with the host. This interface can be configured as a single master/slave mode or as a daisy chain mode that allows the user to connect up to eight 73M1903C devices to a single host for multi Analog Front End applications, such as, central server modems.

Costs saving features of the device include an input reference frequency circuit, which accepts a range of crystals from 4.9-27 MHz. It also accepts external reference clock values between 1 MHz and 40 MHz generated by the host processor. In most applications, this eliminates the need for a dedicated crystal oscillator and reduces the bill of materials (BOM).

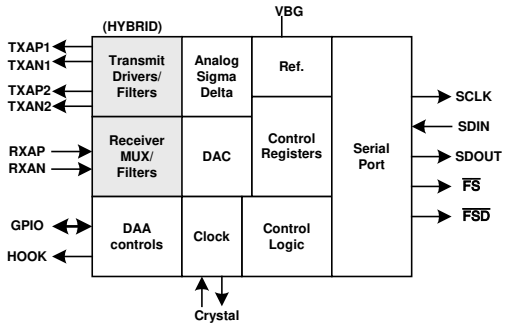
The 73M1903C also supports two analog loop back and one digital loop back test modes.

FEATURES

- Two pairs of software selectable transmit differential outputs for worldwide impedance driver implementations.
- Up to 56 kbps (V.92) performance
- Programmable sample rates (7.2-16.0 kHz)
- Reference clock range of 1-40 MHz
- Crystal frequency range of 4.9-27 MHz
- Master or slave mode operation
- Daisy chain configurable synchronous serial Host interface
- Low power modes
- Fully differential receiver and transmitter Drivers for transformer interface
- 3.0 V – 3.6 V operation
- 5 V tolerant I/O
- Industrial temperature range (-40 to +85 °C)
- JATE compliant transmit spectrum
- Package option: 32-pin QFN

APPLICATIONS

- Central site server modems
- Set Top Boxes
- Personal Video Recorders (PVR)
- Multifunction Peripherals (MFP)
- Fax Machines
- Internet Appliances
- Game Consoles
- Point of Sale Terminals
- Automatic Teller Machines
- Speaker Phones
- Digital Answering Machines
- RF Modems



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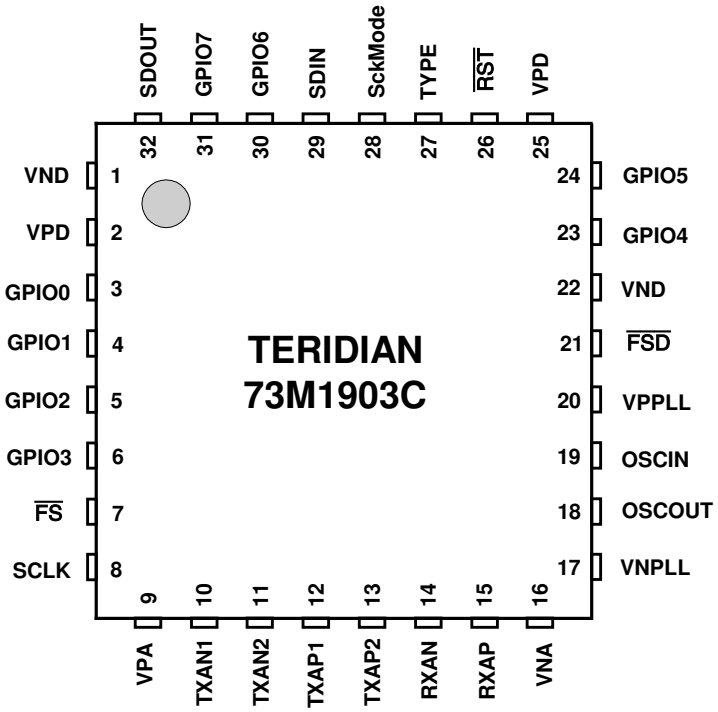
Figures

Tables

1 Pin Description

The 73M1903C modem Analog Front End (AFE) IC is available in a 32-pin QFN package.



73M1903C QFN 32

Table 1 describes the function of each pin. There are three pairs of power supply pins, VPA (analog), VPD (digital) and VPPLL (PLL). They should be separately decoupled from the supply source in order to isolate digital noise from the analog circuits internal to the chip. VPPLL can be directly connected to VPD. Failure to adequately isolate and decouple these supplies will compromise device performance.

Table 1: 32 QFN Pin Description

Pin Name	Type	Pin #	Description
VND	GND	1, 22	Negative Digital Ground.
VNA	GND	16	Negative Analog Ground.
VPD	PWR	2, 25	Positive Digital Supply.
VPA	PWR	9	Positive Analog Supply.
VPPLL	PWR	20	Positive PLL Supply, shared with VPD.
VNPLL	PWR	17	Negative PLL Ground.
RST	I	26	Master reset. When this pin is a logic 0 all registers are reset to their default states; Weak-pulled high-default. A low pulse longer than 100 ns is needed to reset the device. The device will be ready within 100 µs after this pin goes to logic 1 state.
OSCIN	I	19	Crystal oscillator input. When providing an external clock source, drive OSCIN.
OSCOUT	O	18	Crystal oscillator circuit output pin.
GPIO(0-7)	I/O	3, 4, 5, 6, 23 24, 30, 31	Software definable digital input/output pins.

Pin Name	Type	Pin #	Description
RXAN	I	14	Receive analog negative input.
RXAP	I	15	Receive analog positive input.
TXAN1	O	10	Transmit analog negative output 1.
TXAN2	O	11	Transmit analog negative output 2.
TXAP1	O	12	Transmit analog positive output 1.
TXAP2	O	13	Transmit analog positive output 2.
SCLK	I/O	8	Serial interface clock. With master mode and SCLK continuous selected, Freq = 256*Fs (=2.4576 MHz for Fs=9.6 kHz). For slave mode, this pin must be pulled down by a resistor (<4.7 kΩ).
SDOUT	O	32	Serial data output (or input to the host).
SDIN	I	29	Serial data input (or output from the host).
FS	O	7	Frame synchronization. (Active Low)
TYPE	I	27	Type of frame sync. 0 = late (mode0); 1 = early (mode1). Weak-pulled high – default
SckMode	I	28	Controls the SCLK behavior after FS. Open, weak-pulled high = SCLK Continuous; tied low = 32 clocks per R/W cycle.
FSD	O	21	Delayed frame sync to support daisy chain mode with additional 73M1903C devices.

2 Modem Analog Front End (MAFE) Serial Interface

The Modem Analog Front End (MAFE) serial data port is a bi-directional port that is supported by most DSPs. The typical I^2S (Inter-IC Sound, NXP semiconductor) bus can be easily converted into MAFE compatible interface. The 73M1903C can be configured either as a master or a slave of the serial interface. When the 73M1903C is configured as a master device, it generates a serial bit clock, Sclk, from a system clock, Sysclk, which is normally an output from an on-chip PLL that can be programmed by the user. In master mode, the serial bit clock is always derived by dividing the system clock by 18. The Sclk rate, Fsclk, is related to the frame synchronization rate (sample rate), Fs, by the relationship Fsclk = 256 x Fs or Fs = Fsclk / 256 = Fsys / 18 / 256 = Fsys / 4608, where Fsys is the frequency of Sysclk. Fs is also the rate at which both transmit and receive data bytes are sent (received) to (by) the Host.

Throughout this document two pairs of sample rate, Fs, and crystal frequency, Fxtal, will be often cited to facilitate discussions. They are:

1. $Fxtal_1$ = 27 MHz, Fs_1 = 7.2 kHz
2. $Fxtal_2$ = 18.432 MHz, Fs_2 = 8 kHz.
3. $Fxtal_3$ = 24.576 MHz, Fs_3 = 9.6 kHz

Upon reset, until a switch to the PLL based clock, Pllclk, occurs, the system clock will be at the crystal frequency, Fxtal, and therefore the serial bit clock will be sclk = Fsys/18 = Fxtal/18.

Examples:

1. If $Fxtal_1$ = 27.000 MHz, then sclk=1.500 MHz and Fs=sclk/256 = 5.859375 kHz.
2. If $Fxtal_2$ = 18.432 MHz, then sclk=1.024 MHz and Fs=sclk/256 = 4.00 kHz.
3. If $Fxtal_3$ = 24.576 MHz, then sclk=1.3653 MHz and Fs=sclk/256 = 5.33 kHz.

When 73M1903C is programmed through the serial port to a desired Fs and the PLL has settled out, the system clock will transition to the PLL-based clock in a glitch-less manner.

Examples:

1. If Fs_1 = 7.2 kHz, Fsys = 4608 * Fs = 33.1776 MHz and sclk = Fsys / 18 = 1.8432 MHz.
2. If Fs_2 = 8.0 kHz, Fsys = 4608 * Fs = 36.8640 MHz and sclk = Fsys / 18 = 2.048 MHz.
3. If Fs_3 = 9.6 kHz, Fsys = 4608 * Fs = 44.2368 MHz and sclk = Fsys / 18 = 2.4576 MHz.

This transition is entirely controlled by the host. Upon reset or power down of PLL and/or analog front end, the chip will automatically run off the crystal until the host forces the transition by setting Frcvco bit (Bit 7 in Register0E). The transition should be forced on or after the second frame synch period following the write to a designated PLL programming registers (Register08 to Register0D).

When reprogramming the PLL the host should first transition the system clock to the crystal before reprogramming the PLL so that any transients associated with it will not adversely impact the serial port communication.

Power saving is accomplished by disabling the analog front end by clearing ENFE bit (bit 7 Register00).

During the normal operation, a data frame sync signal ($\overline{FS}$) is generated by the 73M1903C at the rate of Fs. For every data $\overline{FS}$ there are 16 bits transmitted and 16 bits received.

The frame synchronization ($\overline{FS}$) signal is pin programmable for type (Figure 1). $\overline{FS}$ can either be early or late determined by the state of the TYPE input pin. When Type pin is left open (high), an early $\overline{FS}$ is generated in the bit clock prior to the first data bit transmitted or received. When held low, a late $\overline{FS}$ operates as a chip select; the $\overline{FS}$ signal is active (low) for all bits that are transmitted or received. The TYPE input pin is sampled when the reset pin is active (low) and ignored at all other times. The final state of the TYPE pin as the reset pin is de-asserted determines the frame synchronization mode used.

2.1 Serial Data and Control

The bits transmitted on the SDOUT pin are defined as follows:

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RX15	RX14	RX13	RX12	RX11	RX10	RX9	RX8	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0

If the HC bit (Bit 0 of Register 01) is set to zero, the 16 bits that are received on the SDIN are defined as follows:

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TX15	TX14	TX13	TX12	TX11	TX10	TX9	TX8	TX7	TX6	TX5	TX4	TX3	TX2	TX1	CTL

In this case LSB(TX0) in a transmit bit stream is forced to 0 automatically.

If the Hardware Control bit (Bit 0 of Register 01) is set to one, the 16 bits that are received on the SDIN input are defined as follows:

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TX15	TX14	TX13	TX12	TX11	TX10	TX9	TX8	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0

Bit 15 is transmitted/received first. Bits RX15:0 are the receive code word. Bits TX15:0 are the transmit code word. If the hardware control bit is set to one, a control frame is initiated between every pair of data frames. If the hardware control bit is set to zero, CTL is used by software to request a control frame. If CTL is high, a control frame will be initiated before the next data frame. A control frame allows the controller to read or write status and control to the 73M1903C.

The control word received on the SDIN pin is defined as follows:

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

The control word transmitted on the SDOUT pin is defined as follows:

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

If the R/W bit (Bit15 of control word) is set to a 0, the data byte transmitted on the SDOUT pin is all zeros and the data received on the SDIN pin is written to the register pointed to by the received address bits; A6-A0. If the R/W bit is set to a 1, there is no write to any register and the data byte transmitted on the SDOUT pin is the data contained in the register pointed to by address bits A6-A0. Only one control frame can occur between any two data frames.

Writes to unimplemented registers are ignored. Reading an unimplemented register returns an unknown value. The position of a control data frame is controlled by the SPOS; bit 1 of register 01h. If SPOS is set to a 0 the control frames occur mid way between data frames, i.e., the time between data frames is equal. If SPOS is set to a 1, the control frame is ¼ of the way between consecutive data frames, i.e., the control frame is closer to the first data frame. This is illustrated in Figure 2.

The 73M1903C IC includes a feature that shuts off the serial clock (SCLK) after 32 cycles of SCLK following the frame synch (Figure 1). The SckMode pin controls this mode. If this pin is left open, the clock will run continuously. If SckMode is set low, the clock will be gated on for 32 clocks for each FS. The SDOUT and $\overline{FS}$ pins change values following a rising edge of SCLK. The SDIN pin is sampled on the falling edge of SCLK. Figure 3 shows the timing diagrams for the serial port.

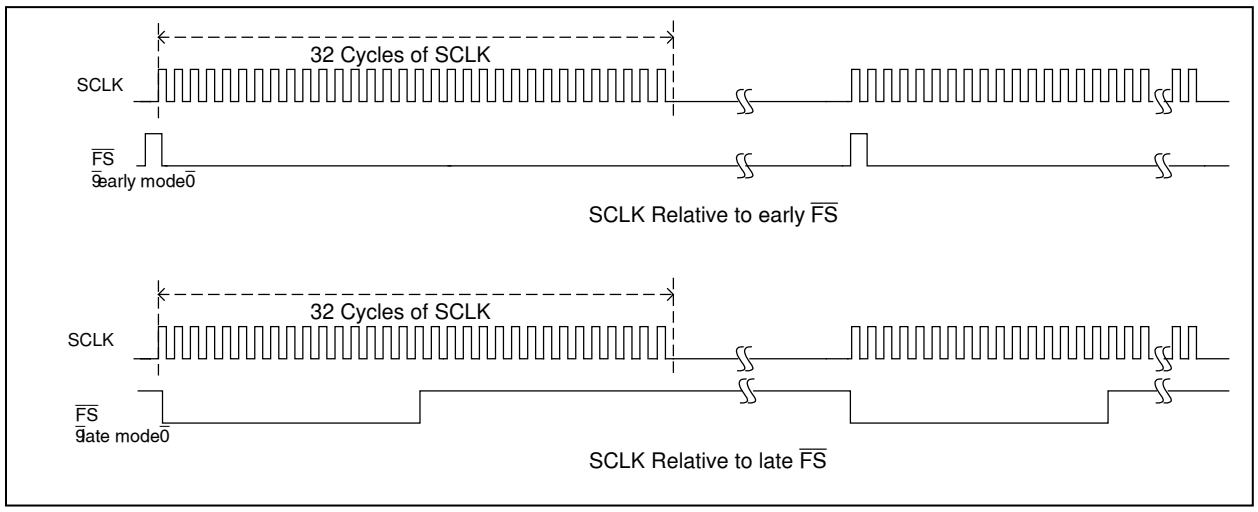


Figure 1: Effect of the TYPE (FS mode) on $\overline{FS}$ with SckMode=0

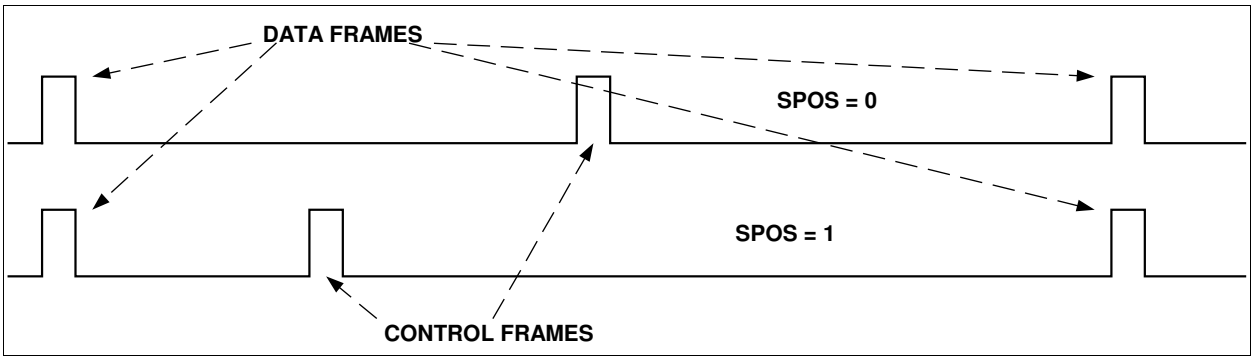
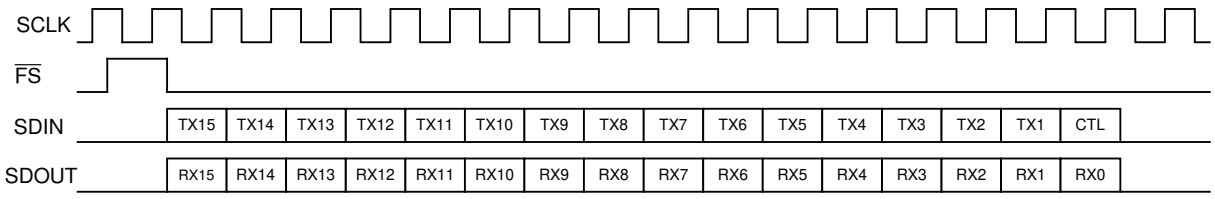
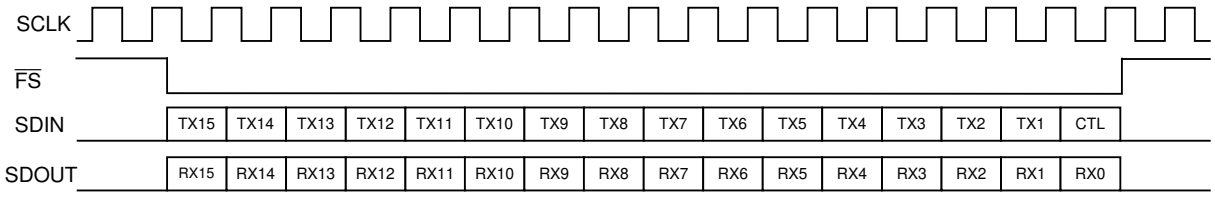


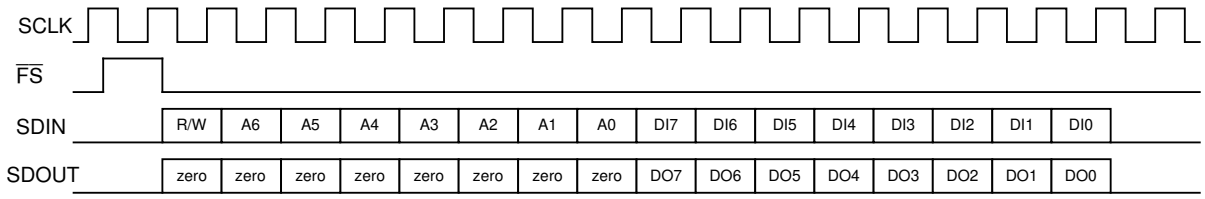
Figure 2: Control Frame Position versus SPOS



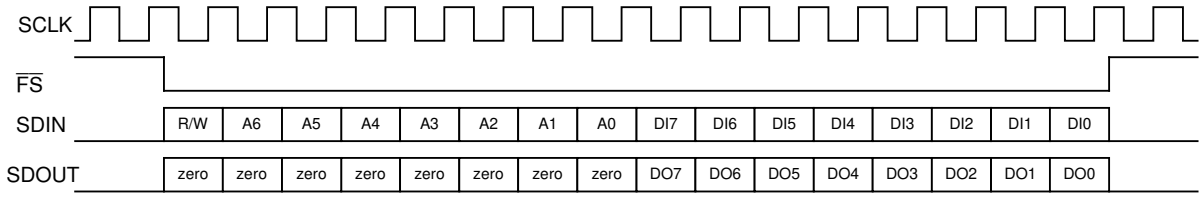
Data Frame with earlyl Frame Sync



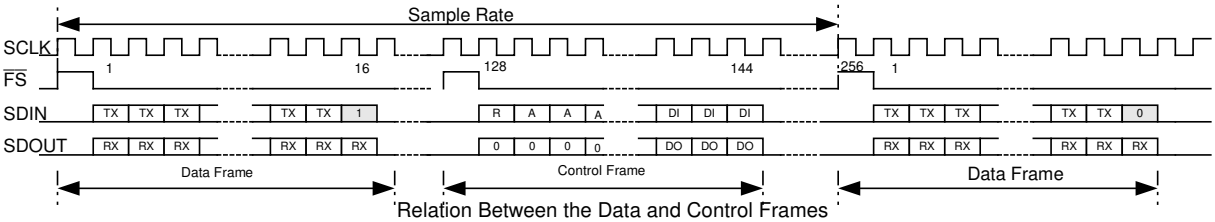
Data Frame with late Frame Sync



Control Frame with early Frame Sync



Control Frame with late Frame Sync



Relation Between the Data and Control Frames
(Master Mode, continuous clock, default SPOS)

Figure 3: Serial Port Timing Diagrams

2.2 Slave Mode and DAISY CHAIN

If the SCLK pin is externally pulled down to ground by a <4.7KΩ resistor, the 79M1903C device is in the slave mode, after reset. In this mode of operation the serial clock (SCLK) and $\overline{FS}$ are inputs to 79M1903C provided by the Master device. The serial clock input must be connected to OSCIN pin while SCLK pin of 73M1903C is unconnected, except for the resistor connected to ground (see Figures 4 and 5). The 73M1903C PLL must be programmed to multiply the serial clock frequency by an appropriate factor in order to obtain Fsys. Therefore the serial clock has to be continuous and without low frequency jitter (the high frequency jitter is rejected by the 79M1903C PLL). The SckMode pin is not used since the Master device provides $\overline{FS}$ and serial clock.

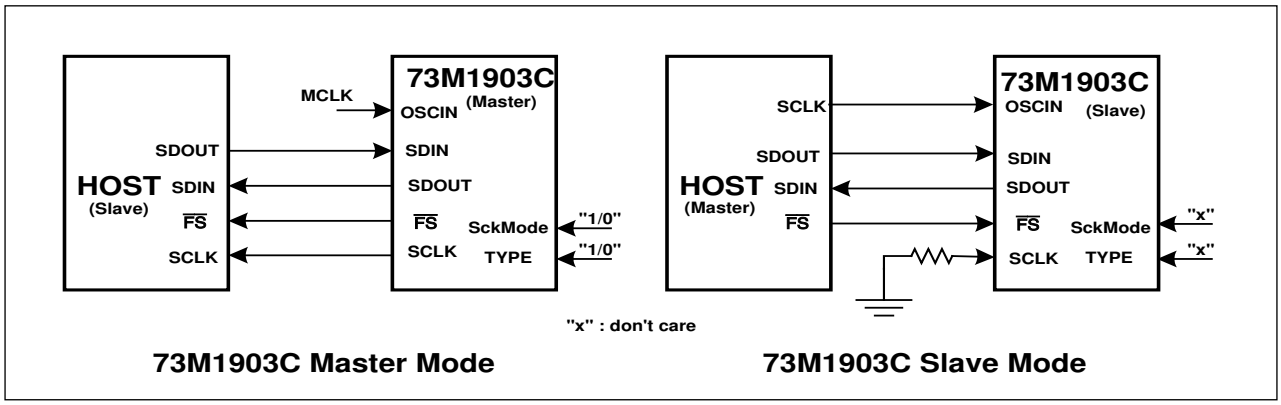


Figure 4: 73M1903C Host Connection in Master and Slave Modes

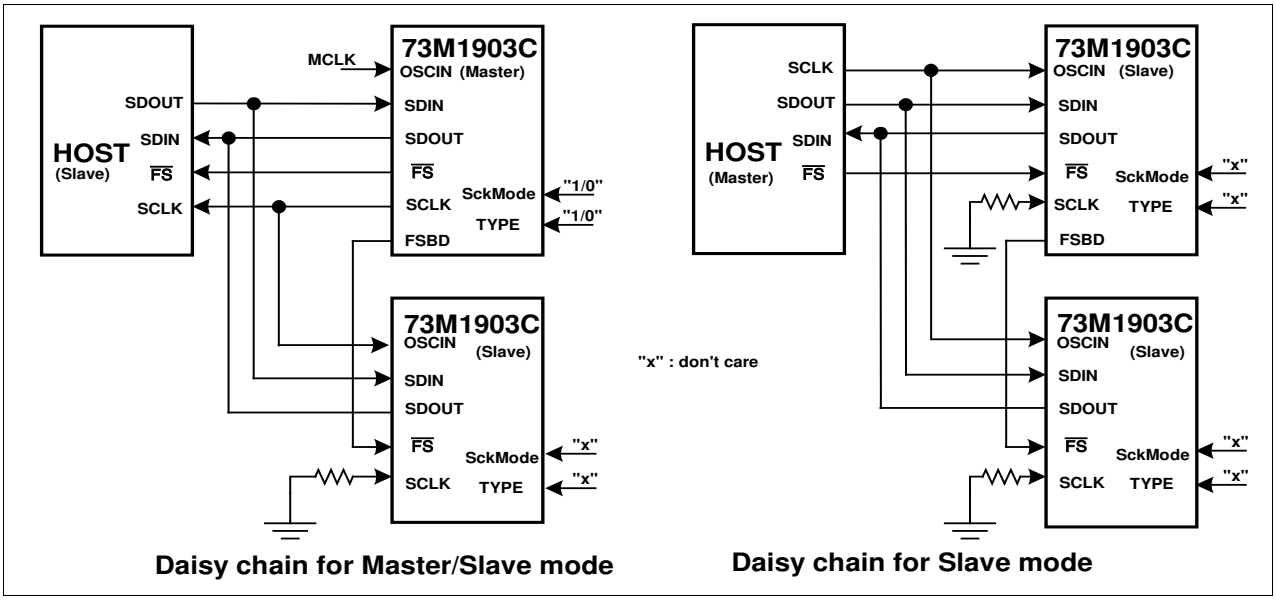


Figure 5: 73M1903C Daisy Chaining for Master/Slave Mode and Slave Modes

In order to daisy chain two or more 73M1903C devices, the master must be programmed into hardware controlled control frame mode by setting the HC bit (bit 0 in Register01) to 1, then set FSDEn (bit 3 in Register06), and then set CkoutEn bit (bit 3 in Register01) to allow the $\overline{FSD}$ to come through. The first frame after enabling $\overline{FSD}$ must be Data. For the two daisy chained devices, the data/control frames are 32 bits. The first 16 bits go to the first device; the next 16 bits go to the second device in the chain, as timed by $\overline{FSD}$ of the first device. For four daisy-chained devices, the data/control frames are 64 bits. The first 16 bits go to the first device in the chain; the next 16 bits go to the second device in the chain as started by $\overline{FSD}$ of the first device, etc. $\overline{FSD}$ is always "Late Type" frame sync.

Up to eight 73M1903C devices may be daisy-chained if the control frame sync is placed at the middle of the data frame sync interval. Four devices may be daisy-chained if the control frame sync is placed at the 1/4 of the data frame sync interval. In all cases involving slave and daisy chain operation, only hardware controlled Control Frames are supported. Software requested control frames are not allowed.

In slave mode the relationship of Fs and Fsclk is Fsclk/Fs, with a range of from 96 to 256 SCLKs per Fs. Again, the host controls the relationship of $\overline{FS}$ to SCLK, with the condition that Fsclk>750 kHz and Fsys=4608*Fs. The 79M1903C PLL must be programmed to generate Fsys with those conditions. To program the 73M1903C NCOs, OSCIN (Fsclk)=SCLK=Fref when Pdvsr=1 and Prst=0 in the calculations. Fsys in the previous discussion is Fvco in the calculations which is equal to 4608*Fs. For example, two typical cases are Fsclk=256*Fs and Fsclk=144*Fs.

For the case when Fsclk=256*Fs and Fs=8 kHz, the 79M1903C PLL has to be set to Fsys=4608*Fs=36.864 MHz, and Sclk=256*8 kHz=2.048 MHz. Therefore Ndvsr=36.864/2.048=18 (12h) and Nrst=0

For the case when Fsclk=144*Fs and d Fs=8 kHz, the 79M1903C PLL has to be set to Fsys=4608*Fs=36.864 MHz and Sclk=144*8 kHz=1.152 MHz. Therefore Ndvsr=36.864/1.152=32 (20h) and Nrst=0

2.3 Control Register Map

Table 2 shows the map of addressable registers in the 73M1903C. Each register and its bits are described in detail in the following sections.

Table 2: Register Map

Register Name	Address	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CTRL	00h	08h	ENFE	SELTX2	TXBST[1:0]		TXDIS	RXG[1:0]		RXGAIN
TEST	01h	00h	TMEN	DIGLB	ANALB	INTLB	CkoutEn	RXPULL	SPOS	HC
DATA	02h	FFh	GPIO7	GPIO 6	GPIO 5	GPIO 4	GPIO 3	GPIO 2	GPIO 1	GPIO 0
DIR	03h	FFh	DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
Register04	04h	00h	Reserved							
Register05	05h	00h	Reserved							
REV	06h	60h	**Rev[3:0]**				FSDEn	Reserved		
Register07	07h	00h	Reserved							
PLL_PSEQ	08h	00h	Pseq[7:0]							
PLL_RST	09h	0Ah	Prst[2:0]			Pdvsr[4:0]				
PLL_KVCO	0Ah	22h	Ichp[3:0]				Reserved	Kvco[2:0]		
PLL_DIV	0Bh	12h	–	Ndvsr[6:0]						
PLL_SEQ	0Ch	00h	Nseq[7:0]							
XTAL_BIAS	0Dh	C0h	Xtal[1:0]		Reserved		–	Nrst[2:0]		
PLL_LOCK	0Eh	00H	Frcvco	PwdnPll	**LockDet**	–	–	–	–	–

Note: Register or bit names in bold underline denotes the READ ONLY bits and registers.
Register bits marked "– " are not used. Writing any value to these bits does not affect the operation.
Reserved are bits reserved for factory test purpose only. Do not attempt to write these locations to values other than their default to prevent unexpected operation.
Register Bit notations used in this document are as follows.
- Registerxx: Register05 represents the register with Address 0x05
- BIT(s)NAME[MSB:LSB] ; Rev[3:0] represents 4 bits of Rev3, Rev2, Rev1 and Rev0.
-(RegisterAddress[BIT(s)]) ; (0X00[7]) represents Bit 7 of Register address 0x00, ENFE bit
(0X06[7:4]) represents Bit 7, Bit 6, Bit 5 and Bit 4 of Register address 06, Rev[3:0].

3 System Control Registers

Register00 (CTRL): Address 00h

Reset State 08h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ENFE	SelTX2	TXBST	TXBST0	TXDIS	RXG1	RXG0	RXGAIN

ENFE (0X00[7]) Enable Front End.
1 = Enable the digital filters and analog front end.
0 = Disable the analog blocks shut off the clocks to the digital and analog receive/transmit circuits.

SelTX2 (0X00[6]) Select Tx driver 2
1 = Selects Secondary transmitter (TXAP2 and TXAN2) if TXDIS=0
0 = Selects Primary transmitter (TXAP1 andTXAN1) if TXDIS=0

TXBST1 (0X00[5])
1 = Add a gain of 1.335dB (16.6%) to the transmitter; also the common mode voltage of the transmit path is increased to 1.586 V. This is intended for enhancing DTMF transmit power only and should not be used in data mode.
0 = No gain is added

TXBST0 (0X00[4])
1 = A gain of 1.65 dB(21%) is added to the transmitter
0 = The gain of the transmitter is nominal

TXDIS (0X00[3])
1 = Tri-state the TXAP1,2 and TXAN1,2 pins, provides a bias of VBG into 80 k Ω for each output pin

RXG(1:0) (0X00[2:1]) Rx Gain Selection
00 = 6 dB Receive Gain
01 = 9 dB
10 = 12 dB
11 = 0 dB

RXGAIN (0X00[0]) 20 dB RxGain Enable. This gain selection can be used for line snoop or Caller ID detection.
1 = Increase the gain of the receiver by 20 dB.
0 = Normal operation

Register01 (TEST): Address 01h

Reset State 00h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMEN	DIGLB	ANALB	INTLB	CkoutEn	RXPULL	SPOS	HC

TMEN (0X01[7]) Test Mode Enable.
0 = Normal operation
1 = Enable test modes.

DIGLB (0X01[6]) Digital Loop back Enable
0 = Normal operation
1 = Tie the serial bit stream from the digital transmit filter output to the digital receive filter input.

ANALB (0X01[5]) Analog Loop back Enable
0 = Normal operation
1 = Tie the analog output of the transmitter to the analog input of the receiver.

INTLB (0X01[4]) Internal Loop back Enable. (Remote Analog Loop back)
0 = Normal operation
1 = Tie the digital serial bit stream from the analog receiver output to the analog transmitter input.

CkoutEn (0X01[3]) Clock Output Enable
1 = Enable the CLKOUT output; This bit must be set after the FSDEn bit is set to enable daisy chain mode.
0 = CLKOUT tri-stated, for normal operation.

RXPULL (0X01[2])
1 = Pulls DC Bias to RXAP/RXAN pins, thru 100Kohm each, to VREF, to be used in testing Rx path.
0 = No DC Bias to RXAP/RXAN pins

SPOS (0X01[1])
1 = Control frames occur after one quarter of the time between data frames has elapsed.
0 = Control frames occur half way between data frames.

HC (0X01[0])
1 = Control frame generation is under hardware control, bit 0 of data frames on SDIN is bit 0 of the transmit word and control frames happen automatically after every data frame.
0 = Control frame generation is under software control, bit 0 of data frames on SDIN is a control frame request bit and control frames happen only on request.

Register06 (REV): Address 06h

Reset State 60h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rev(3:0)				FSDEn	Reserved		

Rev(3:0) (0X06[7:4]) Contain the revision ID of the 73M1903C device. The rest of this register is for chip development purposes only and is not intended for customer use. Do not write to reserved locations.

FSDEn (0X06[3]) Delayed Frame Sync Enable. This bit shall be enabled if the daisy chain mode is used.
1 = Delayed frame sync for daisy chaining of additional 73M1903C devices.
0 = $\overline{\text{FSD}}$ tristated, for normal operation.

4 GPIO Registers

The 73M1903C provides 8 user definable I/O pins. Each pin is programmed separately as either an input or an output by a bit in a direction register. If the bit in the direction register is set high, the corresponding pin is an input whose value is read from the GPIO data register. If it is low, the pin will be treated as an output whose value is set by the GPIO data register.

To avoid unwanted current contention and consumption in the system from the GPIO port before the GPIO is configured after a reset, the GPIO port I/Os are initialized to a high impedance state. The input structures are protected from floating inputs, and no output levels are driven by any of the GPIO pins. The GPIO pins are configured as inputs or outputs when the host controller (or DSP) writes to the GPIO direction register. The GPIO direction and data registers are initialized to all ones (FFh) upon reset**.**

Register02 (DATA): Address 02h

Reset State FFh

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

GPIO(7:0) (0X02[7:0]) Bits in this register will be asserted on the GPIO(7:0) pins if the corresponding direction register bit is a 0. Reading this address will return data reflecting the values of pins GPIO(7:0).

Register03 (DIR): Address 03h

Reset State FFh

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0

DIR(7:0) (0X03[7:0]) This register is used to designate the GPIO pins as either inputs or outputs. If the register bit is reset to 0, the corresponding GPIO pin is programmed as an output. If the register bit is set to a 1, the corresponding pin will be configured as an input.

5 PLL Configuration Registers

Register08 (PLL_PSEQ): Address 08h

Reset State 00h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pseq(7:0)							

Pseq(7:0) (0X08[7:0]) This corresponds to the sequence of divisor. If Prst(2:0) setting in Register09 is 00, this register is ignored.

Register09 (PLL_RST): Address 09h

Reset State 0Ah

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Prst(2:0)			Pdvsr(4:0)				

Prst(2:0) represents the rate at which the sequence register is reset.
Pdvsr(4:0) represents the divisor.

Register0A (PLL_KVCO): Address 0Ah

Reset State 22h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ichp(3:0)				Reserved	Kvco(2:0)		

Ichp(3:0) (0X0A[:47]) represents the size of the charge pump current in the PLL. This charge pump current can be calculated with Ichp = 2.0µA* (2 + Ichp0 + Ichp1 * 2^1 + Ichp2 * 2^2+Ichp3 * 2^3)* (T/To), where To=300 C° and T=Temperature in K°.
Bit 3 is a reserved control bit. This bit shall remain 0 always.
Kvco(2:0) (0X0A[2:0]) Represents the magnitude of Kvco associated with the VCO within PLL.

Table 3: Fvco and Kvco Settings at 25°C

Kvco2	Kvco1	Kvco0	Fvco	Kvco
0	0	0	33 MHz	38 MHz/v
0	0	1	36 MHz	38 MHz/v
0	1	0	44 MHz	40 MHz/v
0	1	1	48 MHz	40 MHz/v
1	0	0	57 MHz	63 MHz/v
1	0	1	61 MHz	63 MHz/v
1	1	0	69 MHz	69 MHz/v
1	1	1	73 MHz	69 MHz/v

Register0B (PLL_DIV): Address 0Bh

Reset State 12h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused	Ndvsr(6:0)						

Ndvsr(6:0) (0X0B[6:0]) Represents the divisor. If Nrst{2:0] =0 this register is ignored.

Register0C (PLL_SEQ): Address 0Ch

Reset State 00h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Nseq(7:0)							

Nseq(7:0) (0X0C[7:0]) Represents the divisor sequence.

Register0D (XTAL_BIAS): Address 0Dh

Reset State 48h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Xtal(1:0)		Reserved		–	Nrst(2:0)		

Xtal(1:0) (0X0D[7:6]) Crystal Oscillator bias current selection
00 = Xtal osc. bias current at 120 µA
01 = Xtal osc. bias current at 180 µA
10 = Xtal osc. bias current at 270 µA
11 = Xtal osc. bias current at 450 µA
If OSCIN is used as a Clock input, the 00 setting should be used to save power.

Nrst(2:0) (0X0D[2:0]) Represents the rate at which the NCO sequence register is reset.
The address 0Dh must be the last register to be written to when effecting a change in PLL.

Register0E (PLL_LOCK): Address 0Eh

Reset State 00h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Frcvco	PwdnPLL	LockDet	–	–	–	–	–

Frcvco (0X0E[7]) Force Vco as System clock Enable.
0 = Xtal oscillator as system clock.
1 = forces VCO as system clock. This bit is set to 0 upon reset, PwdnPll = 1 or ENFE = 0. Both PwdnPll and ENFE are delayed coming out of digital section to keep PLL alive long enough to transition the system clock to crystal clock when Frcvco is reset by PwdnPLL or ENFE.

PwdnPll (0X0E[6]) PLL Power down Enable Please refer to the Table 4.
1 = forces Power down of PLL analog section.
0 = normal operation

LockDet (0X0E[5]) PLL Lock indicator. Read only.
1 = PLL locked
0 = PLL not locked.

Table 4: PLL Power Down

ENFE (Register00 bit7)	PwdnPll (Register0E bit6)	PLL
0	X	PLL Power Off
1	0	PLL Power On
1	1	PLL Power Off

6 Clock Generation

6.1 Crystal Oscillator and Prescaler NCO

The crystal oscillator operates over wide choice of crystals (from 4.9 MHz to 27 MHz) and it is first input to a Numerically Controlled Oscillator (NCO) -based prescaler (divider) prior to being passed onto an on-chip PLL. The intent of the prescaler is to convert the crystal oscillator frequency, Fxtal, to a convenient frequency to be used as a reference frequency, Fref, for the PLL. The NCO prescaler requires a set of three numbers to be entered through the serial port (Pseq[7:0], Prst[2:0] and Pdvsr[2:0]. The PLL also requires 3 numbers as for programming; Ndvsr[6:0], Nseq[7:0], and Nrst[2:0]. The following is a brief description of the registers that control the NCOs, PLLs, and sample rates for the 73M1903C IC. The tables show some examples of the register settings for different clock and sample rates. A more detailed discussion on how these values are derived can be found in Appendix B.

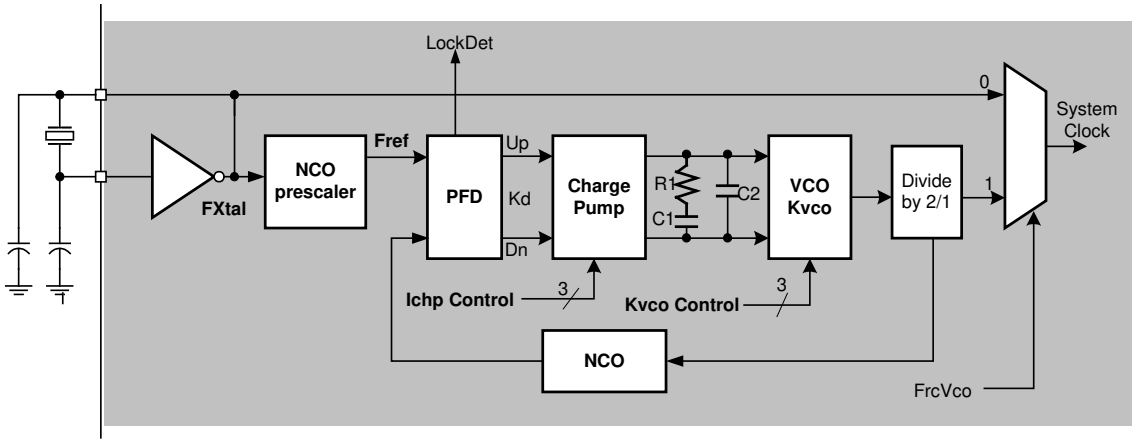


Figure 6: Clock Generation

Table 5: Clock Generation Register Settings for Fxtal = 27 MHz

Reg Address / Fs(kHz)	8h	9h	Ah	Bh	Ch	Dh*	Ichp (µA)	Kvco [2:0]
7.2	DA	EF	20	13	10	C4	8	0
8.0	DA	EF	31	15	04	C2	10	1
2.4*8/7*3 = 8.22857142858	80	F5	41	1D	06	C2	12	1
8.4	DA	EF	31	16	14	C4	10	1
9.0	DA	EF	31	18	XX	C0	10	1
9.6	DA	EF	32	19	1A	C4	10	2
2.4*10/7*3 = 10.2857142857	DA	EF	43	1B	54	C6	12	3
2.4*8/7*4 = 10.9714285714*	40	C7	23	0D	A4	C7	8	3
11.2*	54	C7	23	0E	10	C4	8	3
12.0	DA	EF	24	20	XX	C0	8	4
12.8*	80	E8	15	11	0E	C3	6	5
2.4*10/7*4 = 13.7142857143	54	CB	26	1A	0E	C3	8	6
14.4	DA	EF	46	26	14	C4	12	6
16.0	A4	E9	17	19	1A	C4	6	7

Table 6: Clock Generation Register Settings for Fxtal = 24.576 MHz

Reg Address / Fs(kHz)	8h	9h	Ah	Bh	Ch	Dh*	Ichp (µA)	Kvco [2:0]
7.2	XX	0A	10	0D	02	C1	6	0
8.0	XX	0A	11	0F	XX	C0	6	1
2.4*8/7*3 = 8.22857142858	0E	68	11	0D	02	C1	6	1
8.4	XX	0A	21	0F	0E	C3	8	1
9.0	XX	0A	21	10	FE	C7	8	1
9.6	XX	0A	22	12	XX	C0	8	2
2.4*10/7*3 = 10.2857142857	04	49	23	12	XX	C0	8	3
2.4*8/7*4 = 10.9714285714	0E	68	23	12	XX	C0	8	3
11.2	XX	0A	23	15	XX	C0	8	3
12	XX	0A	14	16	02	C1	6	4
12.8	XX	0A	15	18	XX	C0	6	5
2.4*10/7*4 = 13.7142857143	XX	07	16	12	XX	C0	6	6
14.4	XX	0A	26	1B	XX	C0	8	6
16.0	XX	08	17	18	XX	C0	6	7

Table 7: Clock Generation Register Settings for Fxtal = 9.216 MHz

Reg Address / Fs(kHz)	8h	9h	Ah	Bh	Ch	Dh*	Ichp (µA)	Kvco [2:0]
7.2	XX	04	20	0E	14	C4	8	0
8.0	XX	04	31	10	XX	C0	10	1
8.4	XX	04	31	10	1E	C4	10	1
9.0	XX	04	31	12	XX	C0	10	1
9.6	XX	04	32	13	10	C4	10	2
2.4*8/7*4 = 10.9714285714	02	23	33	13	10	C4	10	3
11.2	XX	04	33	16	14	C4	10	3
12	XX	04	24	18	XX	C0	8	4
12.8	XX	04	35	19	1A	C4	10	5
14.4	XX	08	66	39	1A	C4	16	6
16.0	XX	03	17	18	XX	C0	6	7

Table 8: Clock Generation Register Settings for Fxtal = 24.000 MHz

Reg Address / Fs(kHz)	8h	9h	Ah	Bh	Ch	Dh*	Ichp (µA)	Kvco [2:0]
7.2	DA	EF	30	15	1A	C4	10	0
8.0	02	2C	31	13	10	C4	10	1
2.4*8/7*3 = 8.22857142858	08	72	41	1C	3E	C5	12	1
8.4	DA	EF	41	19	10	C4	12	1
9.0	08	66	11	0A	1E	C4	6	1
9.6	DA	EF	42	1C	1E	C4	12	2
2.4*10/7*3 = 10.2857142857	DA	EF	43	1E	7E	C6	12	3
2.4*8/7*4 = 10.9714285714	3E	A9	33	14	76	C6	10	3
11.2	DA	EF	53	21	1A	C4	14	3
12	08	66	14	0E	14	C4	6	4
12.8	DA	EF	45	26	14	C4	12	5
2.4*10/7*4 = 13.7142857143	10	8C	46	20	80	C7	12	6
14.4	54	CA	46	1C	3E	C5	12	6
16.0	A4	E9	17	1C	1E	C4	6	7

Table 9: Clock Generation Register Settings for Fxtal = 25.35 MHz

Reg Address / Fs(kHz)	8h	9h	Ah	Bh	Ch	Dh*	Ichp (µA)	Kvco [2:0]
7.2	92	F4	50	1A	06	C2	14	0
16.0	40	CA	17	1D	02	C1	6	7

6.2 Analog I/O

Figure 7 shows the block diagram of the analog front end. The analog interface circuit uses differential transmit and receive signals to and from the external circuitry.

The hybrid driver in the 73M1903C is capable of connecting directly, but not limited to, a transformer-based Direct Access Arrangement (DAA). The hybrid driver is capable of driving the DAA's line coupling transformer and load impedance. The hybrid drivers can also drive high impedance loads without modification.

An on-chip band gap voltage is used to provide an internal voltage reference and bias currents for the analog receive and transmit channels. The reference derived from the bandgap, nominally 1.25 V, is multiplied to 1.36 Volts and output at the VREF pin. Several voltage references, nominally 1.25 V, are used in the analog circuits. The band gap and reference circuits are disabled after a chip reset since the ENFE (Register00 bit7) is reset to a default state of zero. When ENFE=0, the band gap voltage and the analog bias currents are disabled. In this case all of the analog circuits are powered down and draw less than 5 µA of current.

A clock generator (CKGN) is used to create all of the non-overlapping phase clocks needed for the time sampled switched-capacitor circuits, ASDM, DAC1, and TLPF. The CKGN input is 2 times the analog/digital interface sample rate or 3.072 MHz clock for Fs=8 kHz.

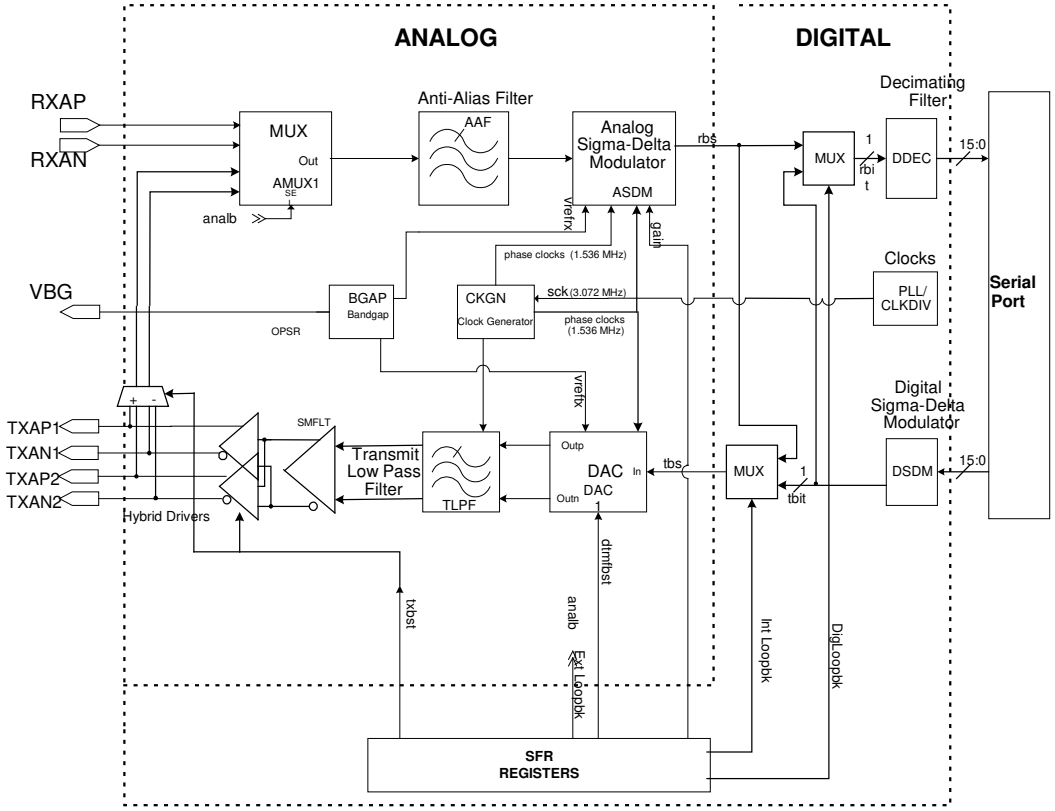


Figure 7: Analog Block Diagram

6.3 Modem Transmitter

The modem transmitter begins with a 48 tap Transmit Interpolation Filter (TIF) that takes in the 16-bit, two's compliment numbers (TXD) at SDIN pin at Fs=8 kHz rate. It up-samples (interpolates) the data to 16 kHz rate rejecting the images at multiples of 8 kHz that exist in the original TXD data stream and outputs 16-bit, two's compliment numbers to a digital sigma-delta modulator. The gain of the interpolation filter is 0.664 (–3.56 dB) at dc.

The digital sigma-delta modulator (DSDM) takes 16-bit, two's compliment numbers as input and generates a 1's bit stream which feeds into a D to A converter (DAC1). The gain through DSDM is 1.0. DSDM takes 16-bit, two's compliment numbers as input and generates a 1's bit stream that feeds into a D to A converter (DAC1).

DAC1 consists of a 5-tap FIR filter and a first order switched capacitor low pass filter both operating at 1.536 MHz. It possesses nulls at multiples of 384 kHz to allow decimation by the succeeding filter.

DAC1's differential output is fed to a 3rd-order switched-capacitor low pass filter (TLPF). The output of TLPF drives a continuous time smoothing filter. The sampling nature of the transmitter leads to an additional filter response that affects the in-band signals. The response is in the form of sin(x)/x and can be expressed as 20*log [(sin(PI*f/fs))/(PI*f/fs)] where f = signal frequency and fs = sample frequency = 16 kHz. Figure 8 and Figure 9 show the frequency response of the transmit path from TXD to TXAP/TXAN. The transmit bandwidth is about 3.65 kHz when Fs=8 kHz. The bandwidth scales with Fs, the sampling rate. In case of Fs=9.6 kHz , then the bandwidth is 3.65 kHz x 9.6/8 = 4.38 kHz and Fs=10.28 kHz, the bandwidth is 3.65 kHz x 10.28/8 = 4.69 kHz. This is applicable for both transmit and receive path filters.

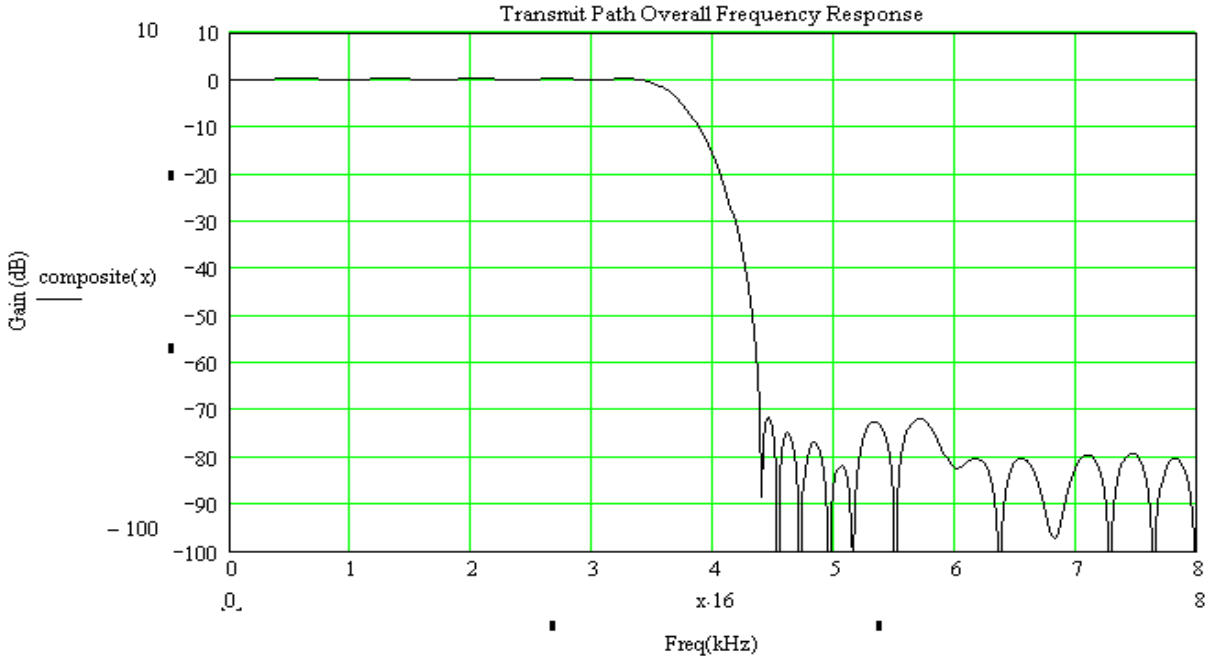


Figure 8: Overall TX Path Frequency Response at 8 kHz Sample Rate

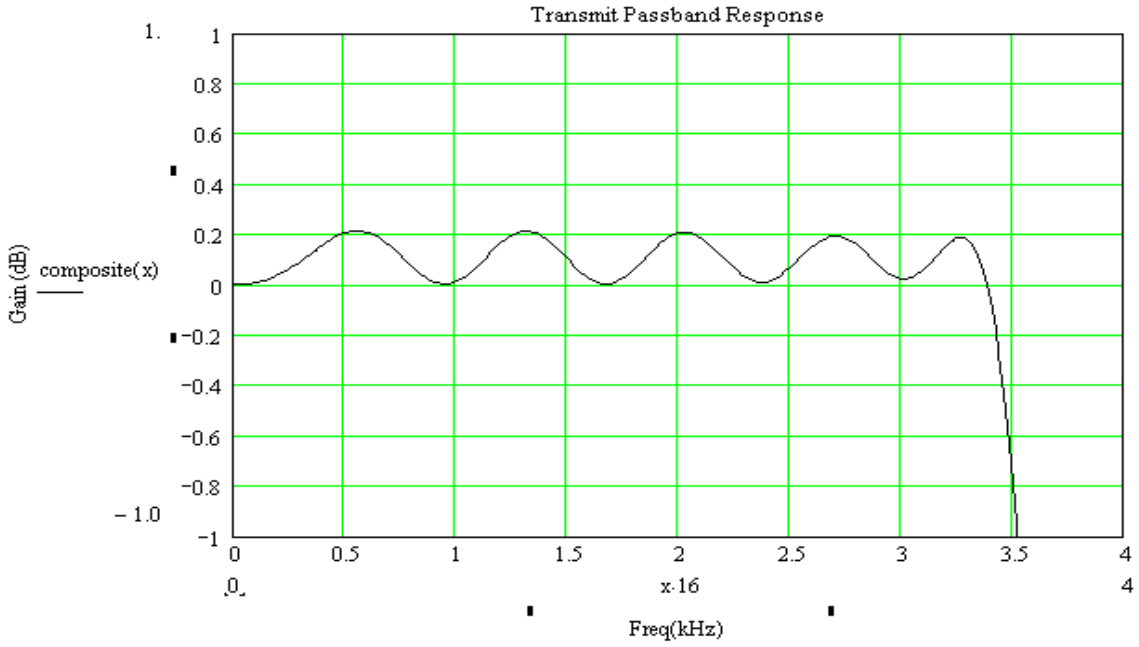


Figure 9: Frequency Response of TX Path for DC to 4 kHz in Band Signal at 8 kHz Sample Rate

6.4 Transmit Levels

The 16-bit transmit code word written by the DSP to the Digital Sigma-Delta Modulator (DSDM) (via TIF) has a linear relationship with the analog output signal. So, decreasing a code word by a factor of 0.5 will result in a 0.5 (-6dB) gain change in the analog output signal.

The following formula describes the relationship between the transmit code word and the output level at the transmit pins (TXAP/TXAN):

Vout (V) = 2 * code/32,767 * DSDMgain * dacGAIN * VREF * TLPFgain * SMFLTgain * FreqFctr

Vout is the differential peak voltage at the TXAP and TXAN pins.

Code is the 16-bit, two's compliment transmit code word written out by the DSP to the DSDM (via TIF). The code word falls within a range of ± 32,767. For a sinusoidal waveform, the peak code word is used in the formula to obtain the peak output voltage.

DSDMgain is the scaling factor used on the transmit code word to reduce the possibility of saturating the modulator. This value is set to 0.640625(–3.555821dB) at dc in the 48 tap transmit interpolation filter (TIF) that precedes DSDM.

dacGAIN is the gain of the DAC. The value *dacGAIN* is calculated based on capacitor values inside DAC1 and *dacGAIN*=8/9=0.8889. The number 32,767 refers to the code word that generates an 82% 1's pulse density at the output of the DSDM. As can be seen from the formula, the D to A conversion is dependent on the level of *VREF*. Also when DTMFBST bit is set, *VREF* is increased from 1.36 V to 1.586 V to allow higher transmit level or 16.6% increase in gain. This bit is intended for enhancing the DTMF transmit level and should not be used in data mode.

TLPFgain is the gain of TLPF and nominally equals to 0.00 dB or 1.0.

SMFLTgain is the gain of SMFLT and nominally equal to 1.445 or 3.2 dB.
When TXBST0 bit is set, the gain is further increased by 1.65 dB (1.21) for the total of 4.85 dB. This is to accommodate greater hybrid insertion loss encountered in some applications.
FreqFctr shows dependency of the entire transmit path on frequency. See Figure 8.

With the transmit code word of +/- 32,767, the nominal differential swing at the transmit pins at dc is:

Vout (V) = 2 * code/32,767 * DSDMgain * dacGAIN * VREF * TLPFgain * SMFLTgain * FreqFctr
= 2 * 32,767/32767 * 0.6640625 * 0.8889 * 1.36 * 1.0 * 1.4454 * 1.0 = 2.31Vpk diff.

When DTMFBST bit is set, Vout (V) = 1.166 * 2.31= 2.693Vpk diff.
When TXBST0 bit is set, Vout (V) = 1.21 * 2.31= 2.795Vpk diff. (1)

When both DTMFBST and TXBST0 are set to 1, Vout (V) = 2.795 * 1.166 = 3.259Vpk diff.

[1] If not limited by power supply or internal reference.

6.5 Transmit Power – dBm

To calculate the analog output power, the peak voltage must be calculated and the peak to rms ratio (crest factor) must be known. The following formula can be used to calculate the output power, in dBm referenced to 600 Ω.

Pout (dBm) = 10 * log [(Vout (V) / cf)^2 / (0.001 * 600)]

The following example demonstrates the calculation of the analog output power given a 1.2 kHz FSK tone (sine wave) with a peak code word value of 11,878 sent out by the DSP.

The differential output voltage at TXAP-TXAN will be:

With FreqFctr = 1.02, (See Figure 8)
Vout (V) = 2 * (11,878/32,767) * 0.6640625 * 0.8889 * 1.36 * 1.0 * 1.4454 * 1.02 = 0.841 V_{pk}.

The output signal power will be:
Pout (dBm) = 10 * log [(0.841 / 1.41)^2 / (0.001 * 600)] = - 2.29 dBm**.**

Table 10: Peak to RMS Ratios and Maximum Transmit Levels for Various Modulation Types

Transmit Type	Crest Factor	Max Line Level
V.90	4.0	-12 dBm
QAM	2.31	-9 dBm
DPSK	1.81	-9 dBm
FSK	1.41	-9 dBm
DTMF	1.99	-5.7 dBm