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73M1866B/73M1966B
MicroDAA™ with PCM Highway

Simplifying System Integration™

DATA SHEET

DS_1x66B_001 **April 2010**

DESCRIPTION

The 73M1866B and 73M1966B use the Teridian patented Data Access Arrangement function (MicroDAA®) designed exclusively for Foreign-Exchange-Office (FXO) in Voice-over-IP (VoIP) applications. These devices provide much of the circuitry required to connect PCM formatted voice channels to a PSTN via a two-wire twisted pair interface. The package options provide the necessary functional programmability and protection required for easy worldwide homologation.

The family of devices consists of the 73M1866B and the 73M1966B. The 73M1866B MicroDAA is the world's first single-package silicon Data Access Arrangement (DAA). Suitable applications for the 73M1866B and 73M1966B devices include VoIP equipment that must provide connectivity to the PSTN for purposes of guaranteeing emergency service calling, redundancy for supplementary connectivity for voice, and maintenance services.

The 73M1966B device set consists of the 73M1906B Host-Side Device that provides digital data, control interfaces and power to the 73M1916 Line-Side Device.

These devices are based on an innovative and patented technology, which sets new standards in reliability and cost. A small pulse transformer forms a digital isolation barrier, transferring both power and data to the PSTN line-side components. This method results in reliable operation in the presence of EMI and a tolerance to line voltage variations by providing power to the Line-Side Device across the barrier. The devices also support the ability to provide up to an additional +6 dB of analog gain to the line-side transmit and +3 dB in the receive signal paths. The device supports transmit and receive digital gain ranging from –18 dB to +7.375 dB by increments of 0.125 dB.

The digital side provides a PCM highway interface with automatic clock rate detection. With an 8-kHz sampling rate, the devices include an ITU-T G.711 compliant codec with selectable µ-law and A-law companding modes. The devices also provide a 16-bit linear mode, which is suitable for interfacing with wide band codecs, as well as 16 kHz sampling rate. Device control is performed over an SPI interface. The SPI supports daisy chain operation.

Through its PCM interface, the 73M1966B can be connected to other PCM enabled devices such as POTS codecs, ISDN codecs, E1/T1 framers, etc.

Additional DAA functions supported by the 73M1x66B devices include a call progress monitor, Caller ID Type I and II, ring detection, pulse dialing, billing tone detection and polarity reversal detection.

APPLICATIONS

- Computer Telephony
- VOIP Equipment
- PBX Systems
- Internet Appliances
- Voicemail Systems
- POTS Termination Equipment

FEATURES

- PCM highway data interface supporting both slave and master modes
- PCM highway interface supporting both E-1 and T-1
- SPI control interface, with daisy chain support for up to 16 devices
- Designed to meet global DAA compliance FCC, ETSI ES 203 021-2, JATE and other PTT standards.
- 8 kHz and 16 kHz sample rates
- 16-bit linear mode
- TX and RX gains adjustable in 0.125 dB increments
- µ-Law, A-law *ITU-T Recommendation G.711* compliant compander operation
- Automatic clock rate detection
- Low power modes
- Polarity Reversal detection
- GPIO for user-configurable I/O ports
- Call Progress Monitor
- Isolation up to 6 kV
- THD -80 dB
- 5 V tolerant I/O on selected pins
- 3.0 V – 3.6 V operating voltage
- Industrial temperature range (-40 °C to +85 °C)
- 5x5 mm 32-pin QFN or 20-pin TSSOP packages
- RoHS compliant (6/6) lead-free package

Table of Contents

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Tables

1 Introduction

The 73M1966B is a two-device chip set that provides embedded FXO functionality by connecting a PCM interface to a voice-band PSTN. The device set supports *ITU-T Recommendation G.711* µ-law and A-law companding, and also a 16-bit linear mode. High-voltage isolation is provided by the physical separation of the Host-Side (73M19106) and Line-Side (73M1916) Devices. The Host-Side and the Line-Side Devices communicate with each other using a single pulse transformer. A few low-cost components complete the DAA interface to the network. The pulse transformer transmits encoded digital data rather than analog signals as with other transformer designs. Data is transmitted and received without the usual degradation from common mode noise and magnetic coupling typical of other capacitive and voice-band transformer techniques. The data stream passed between the Host-Side and Line-Side Devices includes the media stream data, control, status, and clocking information.

This data sheet describes both the 73M1966B and 73M1866B, which will be collectively referred to as the 73M1x66B in this document.

A unique capability of the 73M1x66B Host Side device (73M1906B) is its ability to provide power to the 73M1x66B Line Side device (73M1916) via the pulse transformer.

The 73M1906B exchanges control and status information with the host using the SPI interface, while the PCM encoded media streams connect with other PCM-enabled devices using the PCM highway bus interface.

Figure 1 shows a reference block diagram of the 73M1x66B connected by a pulse transformer and example external line interface circuitry shown for clarification.

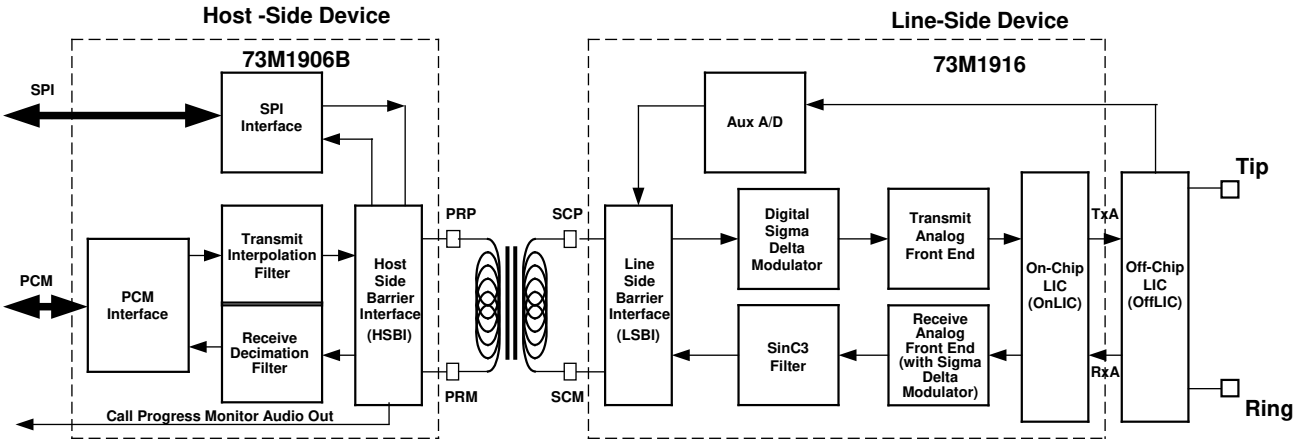

Figure 1: Simple 73M1x66B Reference Block Diagram

The Host-Side Device (73M1906B) consists of:

1. PCM Interface Block (PCM)
2. SPI Interface Block (SPI)
3. Transmit Interpolation Filter
4. Receive Decimation Filter
5. Host-Side Barrier Interface Circuit (HSBI)

The Line-Side Device (73M1916) consists of:

1. Digital Sigma Delta Modulator
2. Transmit Analog Front End
3. Receive Analog Front End including Sigma Delta Modulator
4. $Sinc^3$ Filter (Sinc3)
5. On-chip Line Interface Circuit
6. Line-Side Barrier Interface Circuit (LSBI)

Received data from a host connected to the PCM bus is interpolated from the sampling frequency of 8 kHz or 16 kHz (for PCM encoded streams) to twice the sampling frequency. The control information is multiplexed with the audio stream signals and transmitted across the isolation barrier to the Line-Side Device. In the Line-Side Device, the two streams are separated and the audio signal is converted to analog for transmission to the line.

An audio stream received at the analog line input pins is converted to a serialized data stream and, along with status information such as line condition from the Auxiliary Analog to Digital Converter, is transmitted over the isolation barrier using the pulse transformer. The data is extracted with status information being transmitted on the SPI. The audio stream is sent to a host using the PCM bus.

The 73M1x66B is an enhanced version of the 73M1966 that includes the additional functionality of finer resolution of transmit and receive gain, receiver DC offset subtraction and support for T-1 PCLK frequencies.

2 Pinout

The 73M1906B and the 73M1916 are supplied as 20-pin TSSOP packages and as 32-pin QFN packages.

2.1 73M1906B 20-Pin TSSOP Pinout

Figure 2 shows the 73M1906B 20-pin TSSOP pinout.

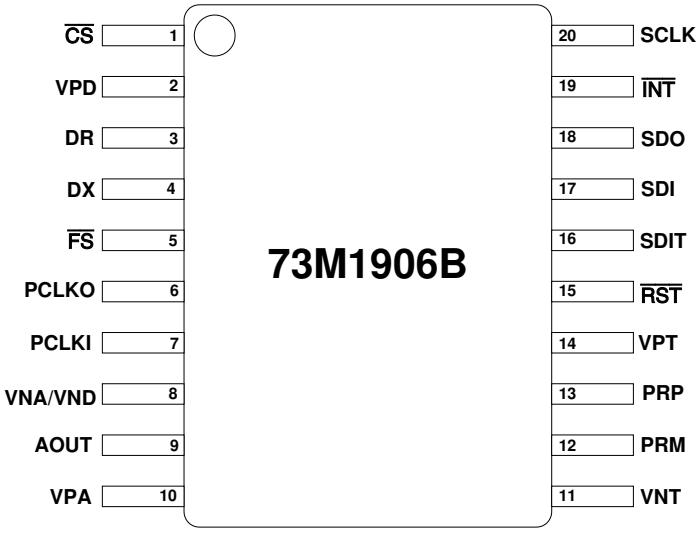

Figure 2: 73M1906B 20-Pin TSSOP Pinout

Table 1 describes the pin functions for the device. Decoupling capacitors on the power supplies should be included for each pair of supply pins.

Table 1: 73M1906B 20-Pin TSSOP Pin Definitions

Pin Number	Pin Name	Type	Description
1	$\overline{CS}$	I	SPI chip select (active low)
2	VPD	PWRI	Positive digital supply
3	DR	I	PCM transmit data sent to the D to A
4	DX	O	PCM received data from the A to D
5	$\overline{FS}$	I/O	PCM frame synchronization
6	PCLKO	O	PCM clock output
7	PCLKI	I	PCM clock in
8	VNA/VND	GND	Negative analog/digital ground
9	AOUT	O	Audio output – must be buffered for speaker
10	VPA	PWRI	Positive analog supply
11	VNT	GND	Negative transformer supply
12	PRM	I/O	Transformer primary minus
13	PRP	I/O	Transformer primary plus
14	VPT	PWRI	Positive transformer supply
15	$\overline{RST}$	I	Hardware reset (active low)
16	SDIT	O	SPI data out for daisy chain mode
17	SDI	I	SPI data in
18	SDO	O	SPI data out
19	$\overline{INT}$	O	Interrupt / ring detect (active low – open drain)
20	SCLK	I	SPI clock

2.2 73M1916 20-Pin TSSOP Pinout

Figure 3 shows the 73M1916 20-pin TSSOP pinout.

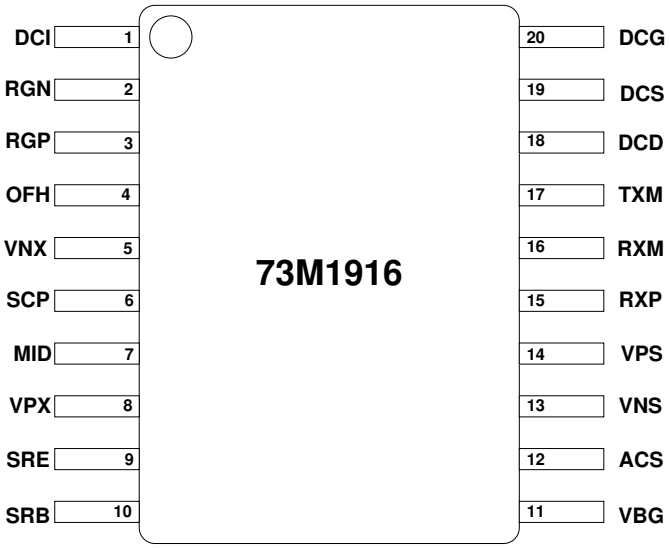

Figure 3: 73M1916 20-Pin TSSOP Pinout

Table 2 describes the pin functions for the device. Decoupling capacitors on the power supplies should be included for each pair of supply pins.

Table 2: 73M1916 20-Pin TSSOP Pin Definitions

Pin Number	Pin Name	Type	Description
1	DCI	I	DC loop input
2	RGN	I	Ring detect negative voltage input
3	RGP	I	Ring detect positive voltage input
4	OFH	O	Off-hook control
5	VNX	GND	Negative supply voltage (line side of the barrier)
6	SCP	I/O	Positive side of the secondary pulse transformer winding
7	MID	I/O	Charge pump midpoint
8	VPX	PWR	Supply from the barrier
9	SRE	I	Voltage regulator sense
10	SRB	O	Voltage regulator drive
11	VBG	O	VBG bypass, connect to 0.1 µF capacitor to VNS
12	ACS	I	AC current sense
13	VNS	GND	Analog negative supply voltage
14	VPS	PWRO	Analog positive supply voltage (output)
15	RXP	I	Receive plus – signal input
16	RXM	I	Receive minus – signal input
17	TXM	O	Transmit minus – transhybrid cancellation output
18	DCD	O	DC loop output
19	DCS	I	DC loop current sense
20	DCG	O	DC loop control

2.3 73M1906B 32-Pin QFN Pinout

Figure 4 shows the 73M1906B 32-pin QFN pinout.

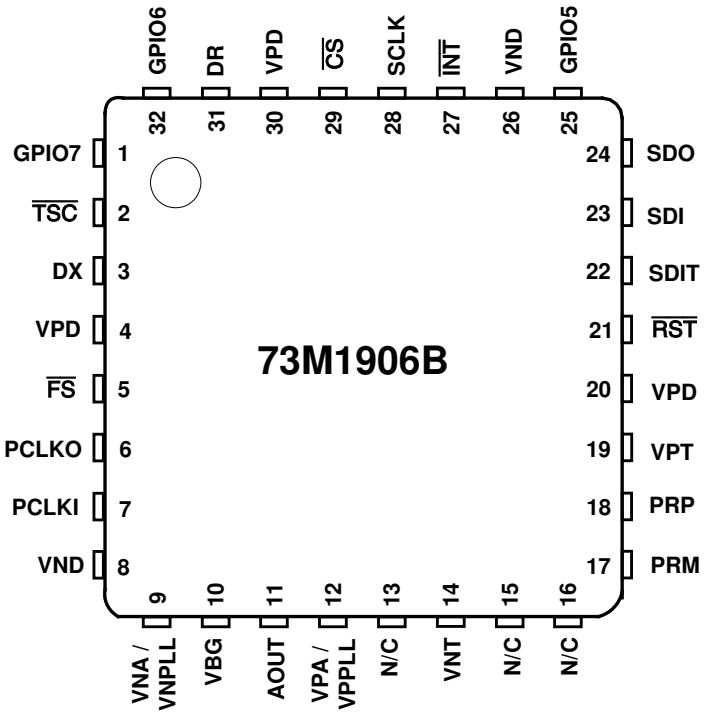

Figure 4: 73M1906B 32-Pin QFN Pinout

Table 3 describes the pin functions for the device. Decoupling capacitors on the power supplies should be included for each pair of supply pins.

Table 3: 73M1906B 32-Pin QFN Pin Definitions

Pin Number	Pin Name	Type	Description
1	GPIO7	I/O	Configurable input/output pin
2	$\overline{TSC}$	O	PCM time slot control (active low)
3	DX	O	PCM received data from the A to D
4	VPD	PWR	Positive digital supply
5	$\overline{FS}$	I/O	PCM frame synchronization
6	PCLKO	O	PCM clock output
7	PCLKI	I	PCM clock in
8	VND	GND	Negative digital ground
9	VNA/VNPLL	GND	Negative analog/PLL ground
10	VBG	O	Band gap voltage reference monitor
11	AOUT	O	Audio output – must be buffered for speaker
12	VPA/VPPLL	PWR	Positive analog/PLL supply
13	N/C	–	No connect
14	VNT	GND	Negative transformer supply
15	N/C	–	No connect
16	N/C	–	No connect

Pin Number	Pin Name	Type	Description
17	PRM	I/O	Transformer primary minus
18	PRP	I/O	Transformer primary plus
19	VPT	PWR	Positive transformer supply
20	VPD	PWR	Positive digital supply
21	$\overline{\text{RST}}$	I	Hardware reset (active low)
22	SDIT	O	SPI data out for daisy-chain mode
23	SDI	I	SPI data in
24	SDO	O	SPI data out
25	GPIO5	I/O	Configurable input/output pin
26	VND	GND	Negative digital ground
27	$\overline{\text{INT}}$	O	Interrupt / ring detect (active low – open drain)
28	SCLK	I	SPI clock
29	$\overline{\text{CS}}$	I	SPI chip select (active low)
30	VPD	PWR	Positive digital supply
31	DR	I	PCM transmit data sent to the D to A
32	GPIO6	I/O	Configurable input/output pin

2.4 73M1916 32-Pin QFN Pinout

Figure 5 shows the 73M1916 32-pin QFN pinout.

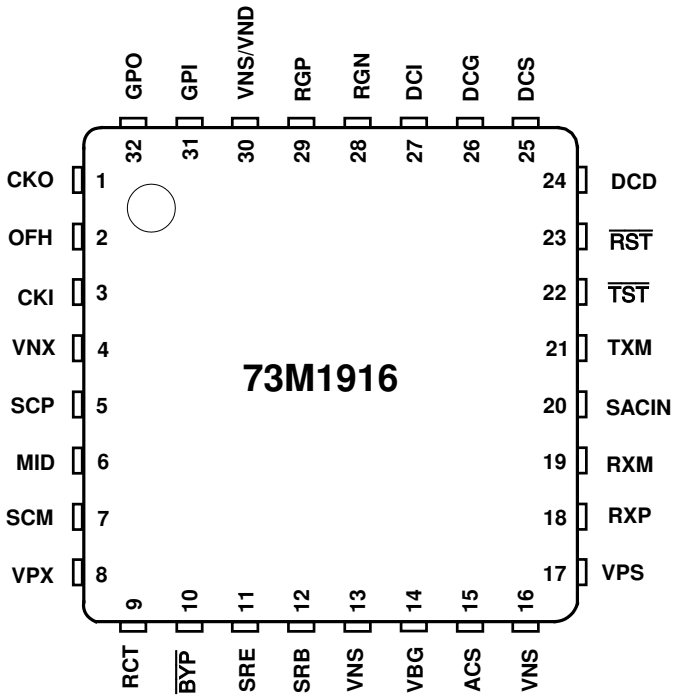

Figure 5: 73M1916 32-Pin QFN Pinout

Table 4 describes the pin functions for the device. Decoupling capacitors on the power supplies should be included for each pair of supply pins.

Table 4: 73M1916 32-Pin QFN Pin Definitions

Pin Number	Pin Name	Type	Description
1	CKO	O	Test point for recovered clock
2	OFH	O	Off-hook control
3	CKI	I	Test input for clock
4	VNX	GND	Negative supply voltage
5	SCP	I/O	Positive side of the secondary pulse transformer winding
6	MID	I/O	Charge pump midpoint
7	SCM	I/O	Negative side of the secondary pulse transformer winding
8	VPX	PWR	Supply from the barrier
9	RCT	I	External rectification – disables internal rectifier when low, leave open
10	$\overline{\text{BYP}}$	I	Test pin, leave open
11	SRE	I	Voltage regulator sense
12	SRB	O	Voltage regulator drive
13	VNS	GND	Digital negative supply voltage
14	VBG	O	VBG bypass, connect to 0.1µF capacitor to VNS
15	ACS	I	AC current sense

Pin Number	Pin Name	Type	Description
16	VNS	GND	Analog negative supply voltage
17	VPS	PWRO	Analog positive supply voltage (output)
18	RXP	I	Receive plus – signal input
19	RXM	I	Receive minus – signal input
20	SACIN	I	Caller ID mode AC impedance connection
21	TXM	O	Transmit Minus – transhybrid cancellation output
22	$\overline{\text{TST}}$	I	Factory test mode, leave open
23	$\overline{\text{RST}}$	I	Resets the control registers to default – weakly pulled high
24	DCD	O	DC loop output
25	DCS	I	DC loop current sense
26	DCG	O	DC loop control
27	DCI	I	DC loop input
28	RGN	I	Ring detect negative voltage input
29	RGP	I	Ring detect positive voltage input
30	VNS	GND	Negative supply voltage (line side of the barrier)
31	GPI	I	General purpose input (test pin)
32	GPO	O	General purpose output (test pin)

2.5 73M1866B Pinout

Figure 6 shows the 73M1866B 42-pin pinout.

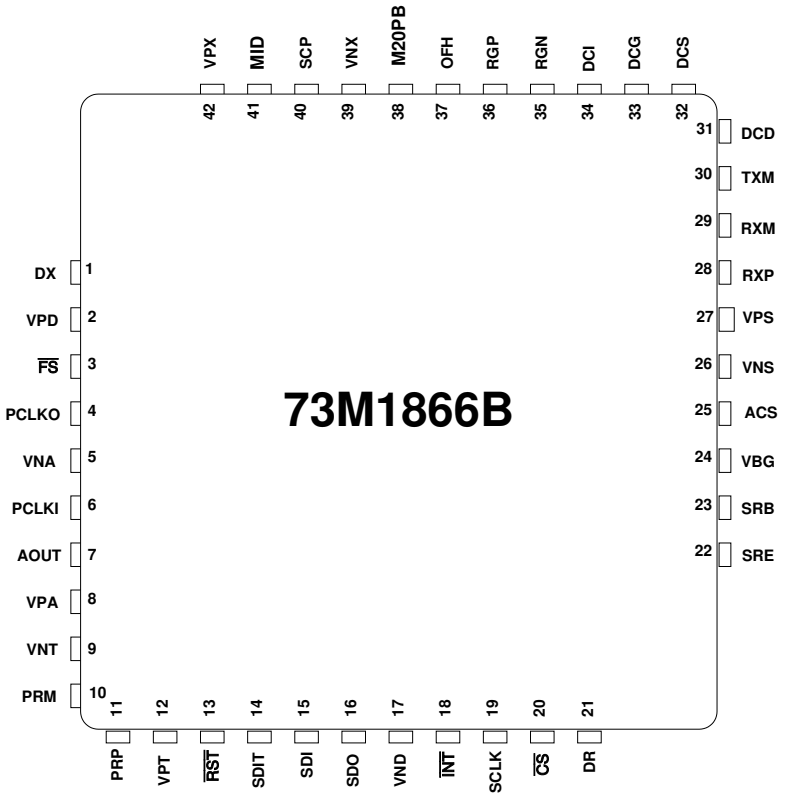

Figure 6: 73M1866B 42-Pin Pinout

Table 5 describes the pin functions for the device. Decoupling capacitors on the power supplies should be included for each pair of supply pins.

Table 5: 73M1866B Pin Definitions

Pin Number	Pin Name	Type	Description
1	DX	O	PCM received data from the A to D
2	VPD	PWR	Positive digital supply
3	$\overline{FS}$	I/O	PCM frame synchronization
4	PCLKO	O	PCM clock output
5	VNA	GND	Negative analog ground
6	PCLKI	I	PCM clock in
7	AOUT	O	Audio output – must be buffered for speaker
8	VPA	PWR	Positive analog supply
9	VNT	GND	Negative transformer supply
10	PRM	I/O	Transformer primary minus
11	PRP	I/O	Transformer primary plus
12	VPT	PWR	Positive transformer supply
13	$\overline{RST}$	I	Hardware reset (active low)
14	SDIT	O	SPI data out for daisy-chain mode
15	SDI	I	SPI data in
16	SDO	O	SPI data out

Pin Number	Pin Name	Type	Description
17	VND	GND	Negative digital ground
18	$\overline{INT}$	O	Interrupt / ring detect (active low – open drain)
19	SCLK	I	SPI clock
20	$\overline{CS}$	I	SPI chip select (active low)
21	DR	I	PCM transmit data sent to the D to A
22	SRE	I	Voltage regulator sense
23	SRB	O	Voltage regulator drive
24	VBG	O	VBG bypass, connect to 0.1µF capacitor to VNS
25	ACS	I	AC current sense
26	VNS	GND	Analog negative supply voltage
27	VPS	PWRO	Analog positive supply voltage (output)
28	RXP	I	Receive plus – signal input
29	RXM	I	Receive minus – signal input
30	TXM	O	Transmit Minus – transhybrid cancellation output
31	DCD	O	DC loop output
32	DCS	I	DC loop current sense
33	DCG	O	DC loop control
34	DCI	I	DC loop input
35	RGN	I	Ring detect negative voltage input
36	RGP	I	Ring detect positive voltage input
37	OFH	O	Off-hook control
38	M20PB	I	Test pin. Connect to VNX.
39	VNX	GND	Negative supply voltage
40	SCP	I/O	Positive side of the secondary pulse transformer winding
41	MID	I/O	Charge pump midpoint
42	VPX	PWR	Supply from the barrier

2.6 Requisite Use of Exposed Bottom Pad on 73M1866B and 73M1966B QFN Packages

The exposed bottom pad is not intended for thermal relief (heat dissipation) and should not be soldered to the PCB. Soldering of the exposed pad could also compromise electrical isolation/insulation requirements for proper voltage isolation. Avoid any PCB traces or through-hole vias on the PCB beneath the exposed pad area.

3 Electrical Characteristics and Specifications

3.1 Isolation Barrier Characteristics

Table 6 provides the characteristics of the 73M1x66B Isolation Barrier.

Table 6: Isolation Barrier Characteristics

Parameter	Rating
Barrier frequency	768 kHz
Data transfer rate across the barrier for the sampling rate of 8 kHz	1.536 Mbps

When 16 kHz sampling rate is selected, the frequency and data transfer rates are twice those shown above.

3.2 Electrical Specifications

This section provides the absolute maximum ratings, the recommended operating conditions and the DC characteristics.

3.2.1 Absolute Maximum Ratings

Table 7 lists the maximum operating conditions for the 73M1x66B. Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to the extremes of the absolute maximum rating for extended periods may affect device reliability.

Table 7: Absolute Maximum Device Ratings

Parameter	Min	Max	Unit
Supply voltage	-0.5	4.0	V
Pin input voltage (except OSCIN)	-0.5	6.0	V
Pin input voltage (OSCIN)	-0.5 to VDD	0.5	V

3.2.2 Recommended Operating Conditions

Function operation should be restricted to the recommended operating conditions specified in Table 8.

Table 8: Recommended Operating Conditions

Parameter	Min	Max	Unit
Supply voltage (VDD) with respect to VSS	3.0	3.6	V
Operating temperature	-40	85	°C

3.2.3 DC Characteristics

Table 9 lists the 73M1x66B DC characteristics.

Table 9: DC Characteristics

Parameter		Condition	Min	Nom	Max	Unit
Input low voltage	VIL	–	-0.5	–	0.2 * VDD	V
Input high voltage	VIH1	–	0.7 VDD	–	5.5	V
Output low voltage	VOL	IOL=4 mA	–	–	0.45	V
Output low voltage FSB,SCLK,	VOL	IOL=1 mA	–	–	0.45	V
Output high voltage	VOH	IOH=-4 mA	VDD - 0.45	–		V
Output high voltage FSB, FSBD, SCLK	VOH	IOH=-1 mA	VDD - 0.45	–		V
Input low leakage current	IIL1	VSS < Vin < VIL1	10	–	40	µA
Input high leakage current	IIH1	VIH1 < Vin < 5.5	–	–	1	µA
IDD current at 3.0 V – 3.6 V			**Nominal at 3.3 V**			
Active digital current	$IDD1_{dig}$	–	–	1.0	1.5	mA
Active PLL current	$IDD1_{pll}$	–	–	1.0	1.5	mA
Active analog current	$IDD1_{ana}$	–	–	12	17	mA
IDD total current*	IDD1	–	–	15	20	mA
IDD total current*	IDD2	–	–	20	30	mA
IDD current PWDN=1	IDD3	–	–	1.0	5	µA
IDD current SLEEP=1 (Ext Ref Clk)	IDD4	–	–	0.5	1.0	mA
IDD current ENFEH=0 (Ext Ref Clk)	IDD6	–	–	1.0	1.5	mA

*Note: IDD1 is with the secondary of the barrier left open.
IDD2 is with the secondary of the barrier connected to 73M1916 fully powered.

3.3 Interface Timing Specification

There are three interfaces associated with the 73M1x66B: the SPI interface, the PCM highway interface and the line interface. This section provides the timing specification for the SPI interface and the PCM highway interface.

3.3.1 SPI Interface

Table 10 lists the characteristics for the SPI interface.

Table 10: SPI Interface Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
SCLK cycle time[1]	t_{scy}	62.5	–	–	ns
SCLK rise time	t_{scr}	–	–	25	ns
SCLK fall time	t_{scf}	–	–	25	ns
$\overline{CS}$ setup time	t_{ics}	25	–	–	ns
$\overline{CS}$ hold time	t_{ich}	20	–	–	ns
SDI setup time	t_{ids}	25	–	–	ns
SDI hold time	t_{idh}	20	–	–	ns
SDO turn on delay	t_{odd}	–	–	20	ns
SDO turn off delay	t_{odo}	–	–	20	ns
SDO hold time	t_{odh}	–	–	20	ns
SDI to SDITHRU propagation delay	t_{idt}	–	6	–	ns

Note1: The minimal value of this parameter is for the case where only one 73M1906B is connected to the host. If the daisy chain mode is used, the minimum SCLK cycle time increases according to the number of slaves in the chain.

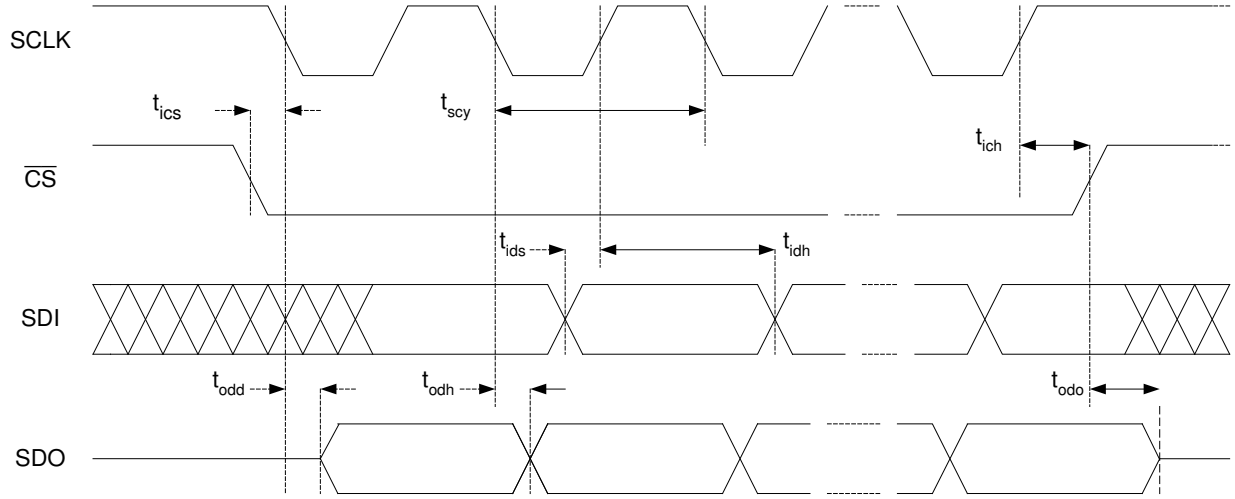

Figure 7: SPI Timing Diagram

3.3.2 PCM Highway Interface

Table 11: Switching Characteristics – PCM Interface (Slave Mode)

Parameter	Symbol	Min	Typ	Max	Unit
PCLK_IN cycle time	t_{pcy}	122	–	3906	ns
PCLK_IN rise time	t_{pcr}	–	–	25	ns
PCLK_IN fall time	t_{pcf}	–	–	25	ns
FS setup time	t_{ifs}	25	–	–	ns
FS hold time	t_{ifh}	20	–	–	ns
FS cycle time	t_{ifc}	–	125	–	µs
DR setup time	t_{ids}	25	–	–	ns
DR hold time	t_{idh}	20	–	–	ns
DX turn on delay	t_{odd}	–	–	20	ns
DX turn off delay	t_{odo}	–	–	20	ns
DX hold time	t_{odh}	–	–	20	ns

Table 12: Switching Characteristics – PCM Interface (Master Mode)

Parameter	Symbol	Min	Typ	Max	Unit
PCLK_OUT cycle time	t_{pcy}	–	488	–	ns
PCLK_OUT rise time	t_{pcr}	–	–	25	ns
PCLK_OUT fall time	t_{pcf}	–	–	25	ns
FS setup time	t_{ifs}	50	–	–	ns
FS hold time	t_{ifh}	50	–	–	ns
FS cycle time	t_{ifc}	–	125	–	µs
DR setup time	t_{ids}	25	–	–	ns
DR hold time	t_{idh}	20	–	–	ns
DX turn on delay	t_{odd}	–	–	20	ns
DX turn off delay	t_{odo}	–	–	20	ns
DX hold time	t_{odh}	–	–	20	ns

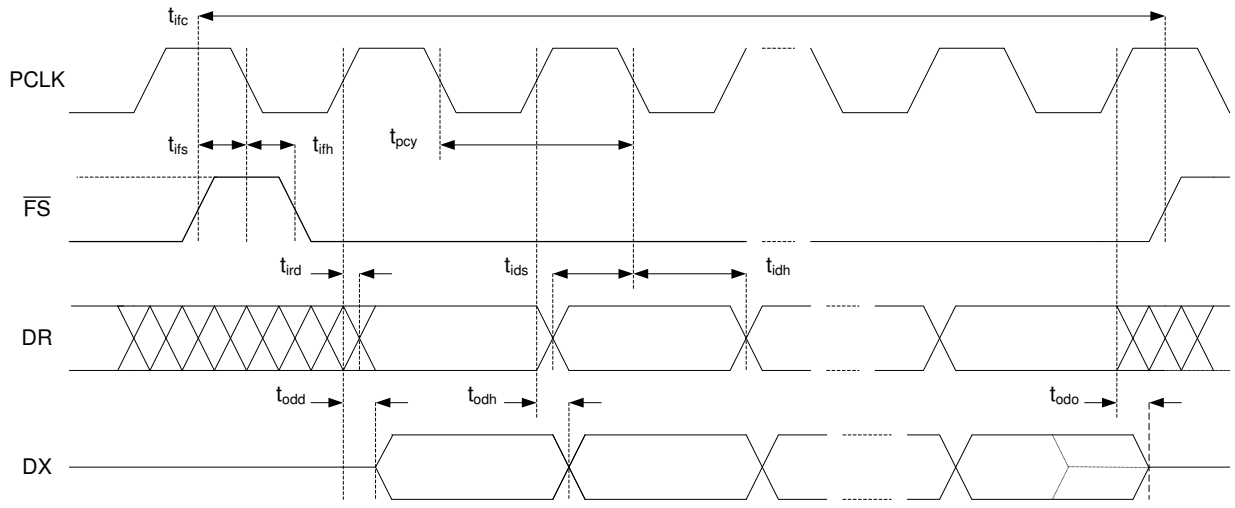

Figure 8: PCM Timing Diagram for Positive Edge Transmit Mode and Negative Edge Receive Mode

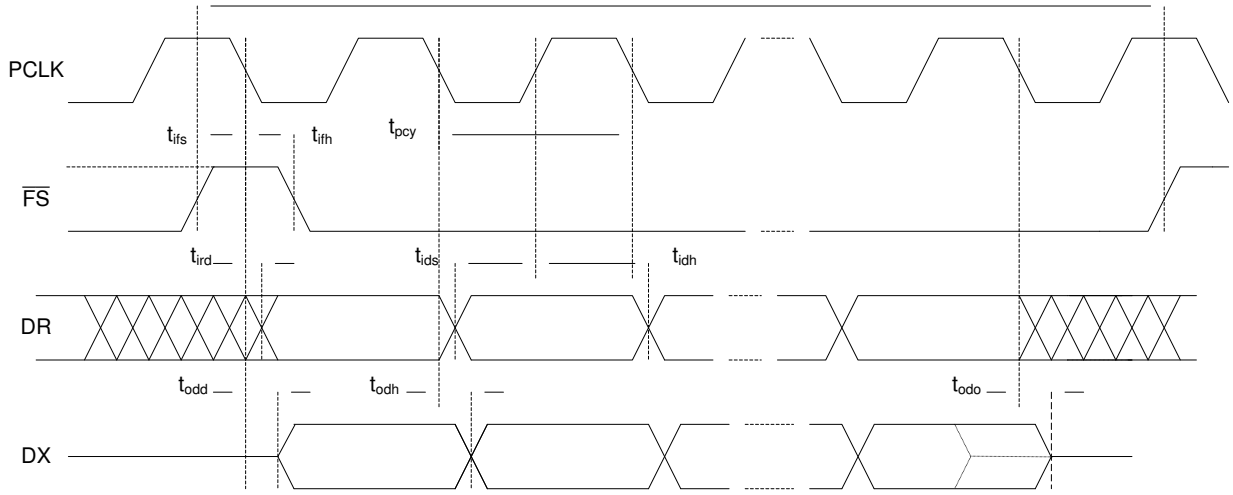

Figure 9: PCM Timing Diagram for Negative Edge Transmit Mode and Positive Edge Receive Mode

3.4 Analog Specifications

This section provides the electrical characterizations of the 73M1x66B analog circuitry.

3.4.1 DC Specifications

VBG is to be connected to an external bypass capacitor with a minimum value of 0.1 µF. This pin is not intended for any other external use.

Table 13: Reference Voltage Specifications

Parameter	Test Condition	Min	Nom	Max	Units
VBG	VDD=3.0 V – 3.6 V	0.9	1.19	1.4	V
VBG Noise	300 Hz – 3.3 kHz	–	-86	-80	dBm_{600}
VBG PSRR	300 Hz – 30 kHz	40	–	–	dB

3.4.2 Call Progress Monitor

The Call Progress Monitor monitors activities on the line. The audio output contains both transmit and receive data with a configurable level individually set by Register 10h.

Figure 10 shows the frequency response of the Call Progress Monitor Filter based upon the characteristics of the device plus the external circuitry as shown.

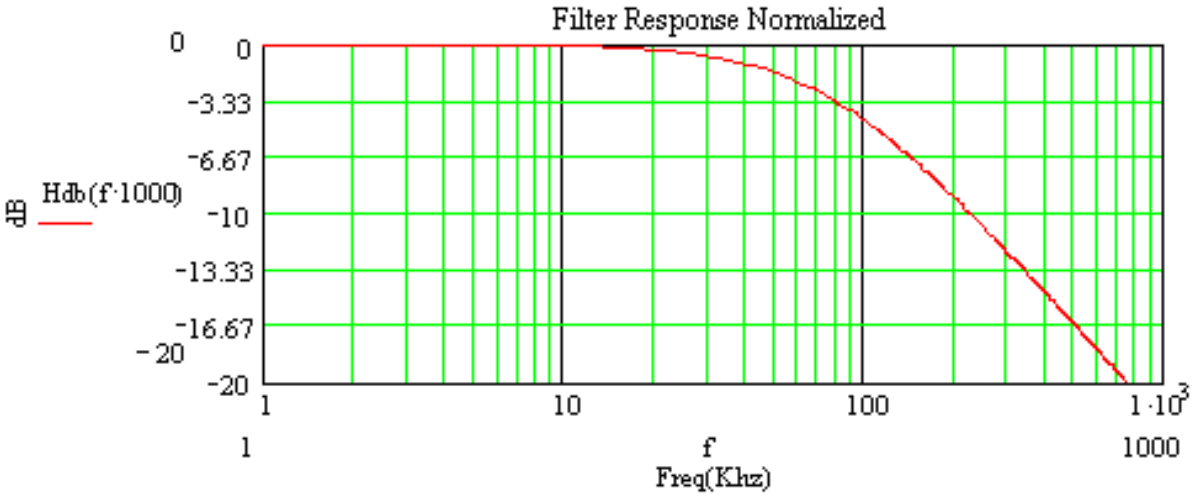

Figure 10: Frequency Response of the Call Progress Monitor Filter

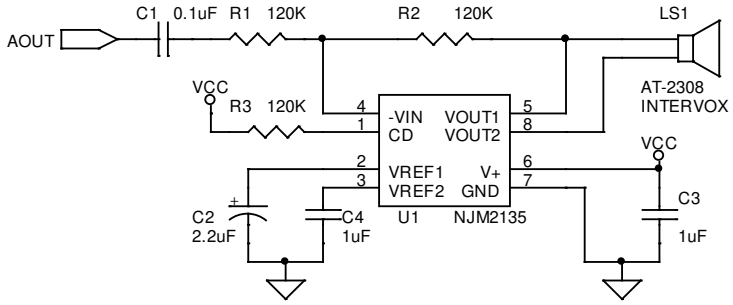

Figure 11: Demo Board Circuit Connecting AOUT to a Speaker

Table 14: Component Values for the Speaker Driver

Quantity	Reference	Part Description	Part
1	C1	Ceramic capacitor	0.1 µF
1	C2	Ceramic capacitor	2.2 µF (optional)
2	C3, C4	Ceramic capacitor	1 µF
1	LS1	Sound transducer	Speaker (Intervox)
3	R1, R2, R3	1/8 W resistor 0603	120 kΩ
1	U1	Audio amplifier	NJM2135 (New Japan Radio)

All measurements are at the AOUT pin with CMVSEL=0. Note that when CMVSEL=1, the peak signal at AOUT is increased to approximately 1.11 Vpk.

Table 15: Call Progress Monitor Specification

Parameter	Test Condition	Min	Nom	Max	Units
AOUT for transmit	1 kHz full swing code (ATX) CMRXG=11 (Mute) Observe AOUT pin	–	–	–	–
	CMTXG=00	–	0.98	–	Vpk
	CMTXG=01 relative to CMTXG=00	–	-6	–	dB
	CMTXG=10 relative to CMTXG=00	–	-12	–	dB
	CMTXG=11 (Mute)	–	Mute	–	dB
AOUT transmit THD	CMTXG=00	–	40	–	dB
AOUT for receive	1.0 Vpk, 1 kHz at the line or 0.5 Vpk at RXP/RXM with RXG=10 CMTXG=11 (Mute) Observe AOUT pin	–	–	–	–
	CMRXG=00	–	0.96	–	Vpk
	CMRXG=01 relative to CMRXG=00	–	-6	–	dB
	CMRXG=10 relative to CMRXG=00	–	-12	–	dB
	CMRXG=11 (Mute)	–	Mute	–	dB
AOUT receive THD	CMRXG=00	–	40	–	dB
AOUT output impedance		–	10	–	kΩ

3.5 73M1x66B Line-Side Electrical Specifications (73M1916)

Table 16 lists the absolute maximum ratings for the line side. Operation outside these rating limits may cause permanent damage to this device.

Table 16: Line-Side Absolute Maximum Ratings

Parameter	Min	Max	Unit
Pin input voltage from VPX to VNX	-0.5	6.0	V
Pin input voltage (all other pins) to VNS	-0.5	4.0	V

3.6 Reference and Regulation

Table 17 lists the VBG specifications. VBG should be connected to an external bypass capacitor with a minimum value of 0.1 µF. This pin is not intended for any other external use.

The following conditions apply: VPX=5 V; Barrier Powered Mode; Barrier Data Rate across the Barrier=1.5 Mbps; VBG connected to 0.1 µF external cap.

Table 17: VBG Specifications

Parameter	Test Condition	Min	Nom	Max	Units
VBG	See conditions above.	–	1.19	–	V
VBG noise	300 Hz – 3.3 kHz	–	-86*	-80	dBm_{600}
VBG PSRR	300 Hz – 30 kHz	40	–	–	dB
VPS	VPX=5.5 V	–	3.15	–	V
VPS PSRR	VPX=4.5 V to 5.5 V	–	40	–	dB

3.7 DC Transfer Characteristics

Table 18 lists the maximum DC transmit levels. All tests are driven at pin DCI and measured at pin DCS. DCEN=1. ILM=1.

Table 18: Maximum DC Transmit Levels

Parameter	Test Condition	Min	Nom	Max	Units
V_{DCON} (DC "On" Voltage)	DCIV=00	0.62	0.69	0.78	V
	DCIV=01	0.83	0.92	1.00	V
	DCIV=10	1.08	1.16	1.24	V
	DCIV=11	1.32	1.42	1.53	V
With ENAC=0	DCIV=XX	0.20	0.26	0.30	V
DC Gain	$V_{DCON}<V_{DCI}<0.4V+V_{DCON}$	-0.30	0 .0	+0.25	dB
I_{DCI} before ILIM	ILM=1 $V_{DCI}=0.28V+V_{DCON}$	–	–	10	µA
I_{DCI} after ILIM	ILM=1 $V_{DCI}=0.44V+V_{DCON}$	20	–	–	µA
Delta V_{DCS} / Delta I_{DCI}	$8.2*45mA< V_{DCS} < 8.2*60mA$	–	0.85	–	mA/V
*Noise	At the line with 300 Ω(ac) (0.15 - 4.0 kHz)	–	-85	-80	dBm

3.8 Transmit Path

Table 19 list the transmit path characteristics. A pattern for a sinusoid of 1 kHz, full scale (code word of +/- 32,767) from the 73M1x66B is forced and ACS is measured with R10=174 Ω. Unless stated otherwise, test conditions are: ACZ=0000 (600 Ω termination), THEN=1, ATEN=1, DAA=01, TXBST=0, sample rate=8kHz.

Table 19: Transmit Path

Parameter	Test Condition	Min	Nom	Max	Units
Offset voltage 8 and 16 kHz sample rate	50% 1's density relative to 1.4 V common mode.	–	25	–	mV
Tx gain, relative to DAA[1:0]=01	DAA=00	2.5	+3	3.5	dB
	DAA=01	-0.5	0	0.5	dB
	DAA=10	-4.5	-4	-3.5	dB
	DAA=11	-8.5	-8	-7.5	dB
AC swing (1 kHz sinusoid) 8 and 16 kHz sample rate	DAA=01	–	0.317	–	Vpk
	DAA=00	–	0.447	–	Vpk
	TXBST=1, DAA=xx	–	0.634	–	Vpk
	ACZ=0001	–	0.211	–	Vpk
	ACZ=0010	–	0.211	–	Vpk
	ACZ=0011	–	0.200	–	Vpk
	ACZ=0100	–	0.254	–	Vpk
	ACZ=0101	–	0.220	–	Vpk
	ACZ=0110	–	0.171	–	Vpk
	ACZ=0111	–	0.194	–	Vpk
	ACZ=1000	–	0.222	–	Vpk
	ACZ=1001	–	0.205	–	Vpk
	ACZ=1010	–	0.223	–	Vpk
	ACZ=1011	–	0.313	–	Vpk
	ACZ=1100	–	0.208	–	Vpk
	ACZ=1101	–	0.211	–	Vpk
	ACZ=1110	–	0.285	–	Vpk
	ACZ=1111	–	0.235	–	Vpk
Idle noise	300 Hz – 4 kHz	–	-80	–	dBm
THD	300 Hz – 4 kHz	–	-80	–	dB
Intermod distortion 1.0 kHz and 1.2 kHz summed	300 Hz – 4 kHz	–	-85	–	dB
Passband ripple	150 Hz – 3.3 kHz	-0.125	–	+0.125	dB
	Gain relative to 1 kHz	–	–	–	dB
	0.5 kHz	–	0.17	–	dB
	1.0 kHz	–	0	–	dB
	2.0 kHz	–	0.193	–	dB
	3.3 kHz	–	-0.12	–	dB
Aliased image	Fs +/- 1 kHz, relative to 1 kHz	–	-75	–	dB

3.9 Receive Path

Table 20 lists the receive path characteristics. All test inputs are driven through an AC coupling network shown in Figure 29. The receive bit stream is measured at the DX pin. RXEN=1.

Table 20: Receive Path

Parameter	Test Condition	Min	Nom	Max	Units
Differential input resistance	RXP/RXM	–	1000	–	kΩ
Input level	Differential, RXP/RXM	–	1.1	1.16	Vpk
Input level	Common mode, RXP/RXM	–	1.37	–	V
Overall sigma-delta ADC modulation gain inclusive of 73M1906B processing	Normalized to VBG=1.19 V. RXG=00 Divide Vrxp/m by PCM Output	–	47.3	–	µV/bit
Offset voltage	R6=17.4 kΩ, R8=52.3 kΩ, R9=21 kΩ. See Figure 12.	–	0	+/- 30	mV
Rx gain (See Note 1.)	RXG=00	-0.5	0	0.5	dB
	RXG=01	2.5	3	3.5	dB
	RXG=10	5.5	6	6.5	dB
	RXG=11	8.5	9	9.5	dB
	RXBST=1, RXG=00	18.3	19.3	20.3	dB
Overall receive frequency response inclusive of 73M1906B processing	Relative to 1 kHz	–	–	–	–
	0.3 kHz – 3.3 kHz	-0.25	0	+0.25	dB
	Fs (8 kHz)	–	-75	–	dB
Idle noise	300 Hz – 4 kHz	–	-80	–	dBm
THD	RXG=00	–	-85	–	dB
	RXBST=1	–	-60	–	
Intermod Dist 1.0 kHz and 1.2 kHz summed	300 Hz – 4 kHz	–	-85	–	dB
Crosstalk	1 Vpk 1 kHz sine wave at TXP; FFT on Rx ADC samples, first four harmonics reflected to the line.	–	-90	–	dBm
CMRR	RXP=RXM 1 Vpk	40	–	–	dB
PSRR	-30 dBm signal at VPX in Barrier Powered Mode; 300 Hz – 30 kHz.	–	–	40*	dB
On-Hook AC Impedance	300 Hz – 4 kHz, without EMI caps.	–	2	–	MΩ

Note 1: RXG controls the amount of gain or attenuation of the receiver analog gain element as specified in Table 20. The overall receiver channel gain has 6 dB of attenuation and the net effect of the RXG bits on the receiver channel gain is defined in Table 36.