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**Simplifying System Integration™**

**DS_8010R_022**

**August 2009**

**ISO/IEC 7816-3**

## DESCRIPTION

The Teridian 73S8010R is a single smart card interface IC that provides full electrical compliance with ISO-7816-3 and EMV 4.0 (EMV2000) specifications.

Interfacing with the host is done through the two-wire $I^2C$ bus and one interrupt output to inform the system controller of the card presence and faults. The card clock signal can be generated by an on-chip oscillator using an external crystal, or by connection to a clock signal.

The Teridian 73S8010R incorporates an ISO-7816-3 activation/deactivation sequencer that controls the card signals. Level-shifters drive the card signals with the selected card voltage (3 V or 5 V), coming from an internal Low Drop-Out (LDO) voltage regulator. This LDO regulator is powered by a dedicated power supply input, $V_{PC}$. Digital circuitry is separately powered by a digital power supply, $V_{DD}$.

With its embedded LDO regulator, the Teridian 73S8010R is a cost-effective solution for any application where a 5 V (typically -5% +10%) power supply is available. Hardware support for auxiliary I/O lines, C4 / C8 contacts is provided.

Emergency card deactivation is initiated upon card extraction or upon any fault generated by the protection circuitry. The fault can be a card over-current, a $V_{DD}$ (digital power supply), a $V_{PC}$ (regulator power supply), a $V_{CC}$ (card power supply) or an over-heating fault.

The card over-current circuitry is a true current detect function, as opposed to $V_{CC}$ voltage drop detection, as usually implemented in ICC interface ICs.

The $V_{DD}$ voltage fault has a threshold voltage that can be adjusted with an external resistor or resistor network. It allows automated card deactivation at a customized $V_{DD}$ voltage threshold value. It can be used, for instance, to match the system controller operating voltage range.

## APPLICATIONS

- Set-Top-Box Conditional Access and Pay-per-View
- Point of Sales & Transaction Terminals
- Control Access & Identification
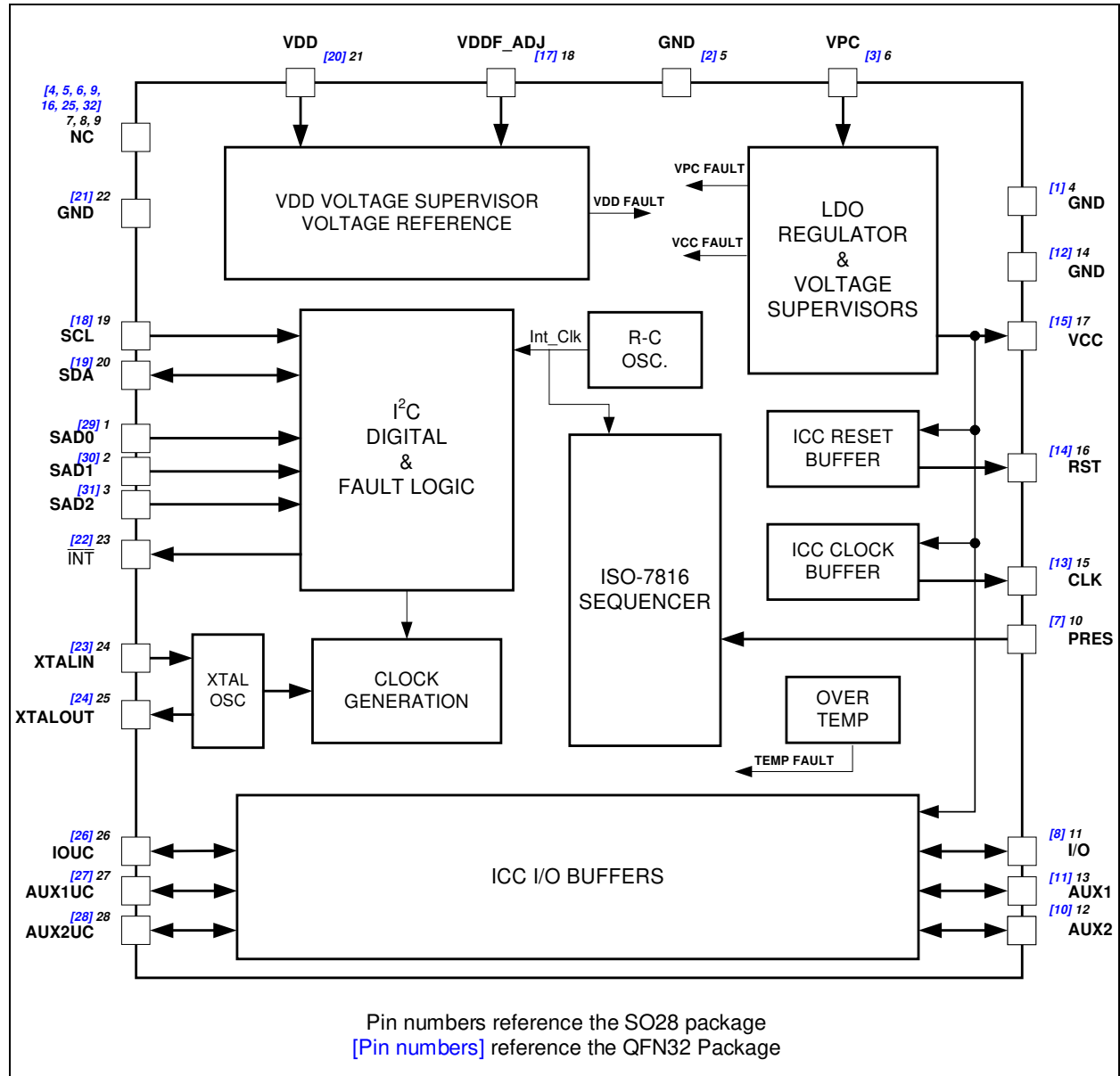- Multiple card and SAM reader configurations

## ADVANTAGES

- Single smart card interface
- IC firmware compatible with TDA8020
- Traditional step-up converter is replaced by an LDO regulator
  - → Greatly reduced power dissipation
  - → Fewer external components are required
  - → Better noise performance
  - → High current capability (90 mA supplied to the card)
- Small format (5x5x0.8 mm) QFN32 package option
- True card over-current detection

## FEATURES

- Card Interface
  - Complies with ISO-7816-3 and EMV 4.0
  - An LDO voltage regulator provides 3 V / 5 V to the card from an external power supply input
  - ISO-7816-3 Activation / Deactivation sequencer with emergency automated deactivation on card removal or fault detected by the protection circuitry
  - Protection includes 3 voltage supervisors that detect voltage drops on $V_{CC}$ card and on power supplies $V_{DD}$ and $V_{PC}$
  - Over-current detection 150 mA max
  - 1 card detection input
  - Auxiliary I/O lines, for C4 / C8 contact signals
- Host Interface
  - Fast mode, 400 kbps $I^2C$ slave bus
  - 8 possible devices in parallel
  - One control register and one status register
  - Interrupt output to the host for fault detection
  - Crystal oscillator or host clock, up to 27 MHz
- 6 kV ESD protection on the card interface
- SO28 or QFN32 package

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## FUNCTIONAL DIAGRAM



**Figure 1: 73S8010R Block Diagram**

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## Figures

## Tables

# 1  Pinout

The 73S8010R is supplied as a 32-pin QFN package and as a 28-pin SO package.
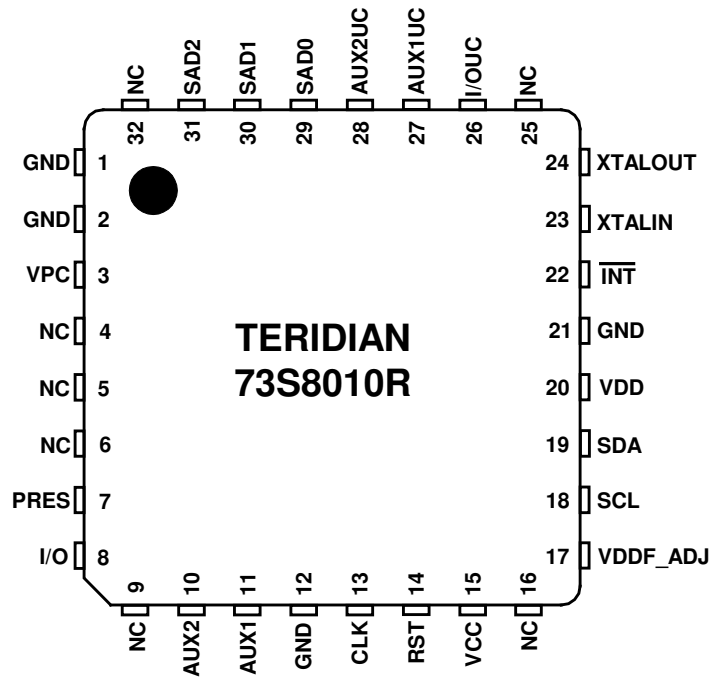


**Figure 2: 73S8010R 32-Pin QFN Pinout**
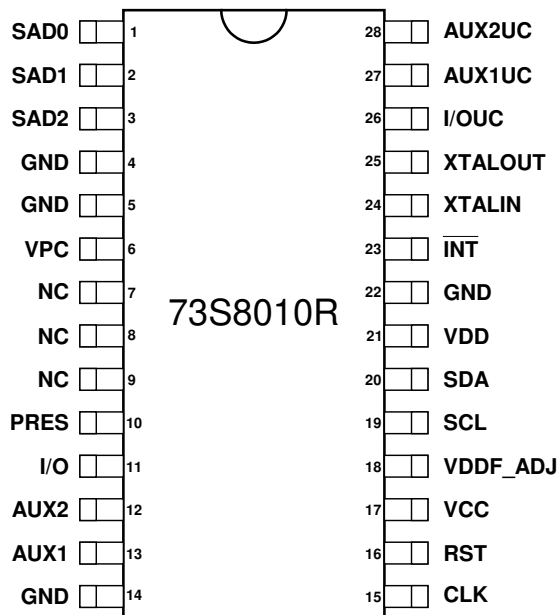


**Figure 3: 73S8010R 28-Pin SO Pinout**

Table 1 describes the pin functions for the device.

**Table 1: 73S8010R Pin Definitions**

| Pin Name | Pin (SO28) | Pin (QFN32) | Type | Description |
|---|---|---|---|---|
| **Card Interface** | | | | |
| I/O | 11 | 8 | IO | Card I/O: Data signal to/from card.  Includes a pull-up resistor to $V_{CC}$. |
| AUX1 | 13 | 11 | IO | AUX1: Auxiliary data signal to/from card.  Includes a pull-up resistor to $V_{CC}$. |
| AUX2 | 12 | 10 | IO | AUX2: Auxiliary data signal to/from card.  Includes a pull-up resistor to $V_{CC}$. |
| RST | 16 | 14 | O | Card reset: provides reset (RST) signal to card. |
| CLK | 15 | 13 | O | Card clock: provides clock signal (CLK) to card.  The crystal oscillator frequency and CLKSEL bits in the control register determine the rate of this clock. |
| PRES | 10 | 7 | I | Card Presence switch: active high indicates card is present.  Includes a pull-down resistor. |
| VCC | 17 | 15 | PSO | Card power supply – logically controlled by the sequencer, output of LDO regulator.  Requires an external filter capacitor to GND. |
| GND | 14 | 12 | GND | Card ground. |
| **Miscellaneous Inputs and Outputs** | | | | |
| XTALIN | 24 | 23 | I | Crystal oscillator input: can be connected to crystal or driven as a source for the card clock. |
| XTALOUT | 25 | 24 | O | Crystal oscillator output: connected to crystal.  Left open if XTALIN is being used as an external clock input. |
| VDDF_ADJ | 18 | 17 | I | $V_{DD}$ threshold adjustment input: this pin can be used to overwrite a higher VDDF value (that controls deactivation of the card).  Must be left open if unused. |
| NC | 7, 8, 9 | 4,5,6,9, 16,25,32 | – | Non-connected pin. |
| **Power Supply and Ground** | | | | |
| VDD | 21 | 20 | | System interface supply voltage and supply voltage for internal circuitry. |
| VPC | 6 | 3 | | LDO regulator power supply source. |
| GND | 4 | 1 | GND | LDO regulator ground. |
| GND | 14 | 12 | GND | Smart card I/O ground. |
| GND | 5, 22 | 2,21 | GND | Digital ground. |

| Pin Name | Pin (SO28) | Pin (QFN32) | Type | Description |
|---|---|---|---|---|
| **Microcontroller Interface** | | | | |
| $\overline{\text{INT}}$ | 23 | 22 | O | Interrupt output signal (negative assertion) to the processor. A 20 k$\Omega$ pull up to $V_{DD}$ is provided internally. |
| SAD0 SAD1 SAD2 | 1 2 3 | 29 30 31 | I I I | Serial device address bits. Digital inputs for address selection that allows for the connection of up to 8 devices in parallel. Address selections is as follows: <br><br> Pins SAD0 and SAD1 are internally pulled down and SAD2 is internally pulled up. The default address when unconnected is 0x48. |
| SCL | 19 | 18 | I | I$^2$C clock signal input. |
| SDA | 20 | 19 | I/O | I$^2$C bi-directional serial data signal. |
| I/OUC | 26 | 26 | IO | System controller data I/O to/from the card. Includes an internal pull-up resistor to $V_{DD.}$ |
| AUX1UC | 27 | 27 | IO | System controller auxiliary data I/O to/from the card. Includes an internal pull-up resistor to $V_{DD.}$ |
| AUX2UC | 28 | 28 | IO | System controller auxiliary data I/O to/from the card. Includes an internal pull-up resistor to $V_{DD.}$ |

| SAD2 | SAD1 | SAD0 | (7 bit) I$^2$C Address |
|---|---|---|---|
| 0 | 0 | 0 | 0x40 |
| 0 | 0 | 1 | 0x42 |
| 0 | 1 | 0 | 0x44 |
| 0 | 1 | 1 | 0x46 |
| 1 | 0 | 0 | 0x48 |
| 1 | 0 | 1 | 0x4A |
| 1 | 1 | 0 | 0x4C |
| 1 | 1 | 1 | 0x4E |

# 2   Electrical Specifications

This section provides the following:

- Absolute Maximum Ratings
- Recommended Operating Conditions
- Smart Card Interface Requirements
- Digital Signals Characteristics
- DC Characteristics
- I2C Interface Characteristics
- Voltage / Temperature Fault Detection Circuits

## 2.1   Absolute Maximum Ratings

Table 2 lists the maximum operating conditions for the 73S8010R.  Permanent device damage may occur if absolute maximum ratings are exceeded.  Exposure to the extremes of the absolute maximum rating for extended periods may affect device reliability.

**Table 2: Absolute Maximum Device Ratings**

| Parameter | Rating |
|---|---|
| Supply voltage $V_{DD}$ | -0.5 to 6.0 VDC |
| Supply voltage $V_{PC}$ | -0.5 to 6.0 VDC |
| Input voltage for digital inputs | -0.3 to ($V_{DD}$ +0.5) VDC |
| Storage temperature | -60 °C to +150 °C |
| Pin voltage (except card interface) | -0.3 to ($V_{DD}$ + 0.5) VDC |
| Pin voltage (card interface) | -0.3 to ($V_{CC}$ + 0.5) VDC |
| ESD tolerance – Card interface pins | +/- 6 kV |
| ESD tolerance – Other pins | +/- 2 kV |

Note: ESD testing on smart card pins is HBM condition, 3 pulses, each polarity referenced to ground.

## 2.2   Recommended Operating Conditions

Function operation should be restricted to the recommended operating conditions specified in Table 3.

**Table 3: Recommended Operating Conditions**

| Parameter | Rating |
|---|---|
| Supply voltage $V_{DD}$ | 2.7 to 5.5 VDC |
| Supply voltage $V_{PC}$ | 4.75 to 5.5 VDC |
| Ambient operating temperature | -40 °C to +85 °C |
| Input voltage for digital inputs | 0 V to $V_{DD}$ to +0.3 V |

## 2.3   Smart Card Interface Requirements

Table 4 lists the 73S8010R Smart Card interface requirements.

**Table 4: DC Smart Card Interface Requirements**

| Symbol | Parameter | Condition | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| **Card Power Supply (V$_{CC}$) Regulator** <br> **General Conditions: -40 °C < T < 85 °C, 4.75 V < V$_{PC}$ < 5.5 V, 2.7 V < V$_{DD}$ < 5.5 V** | | | | | | |
| V$_{CC}$ | Card supply voltage including ripple and noise | Inactive mode | -0.1 | – | 0.1 | V |
| | | Inactive mode I$_{CC}$ = 1 mA | -0.1 | – | 0.4 | V |
| | | Active mode; I$_{CC}$ < 65 mA; 5 V | 4.60 | – | 5.25 | V |
| | | Active mode; I$_{CC}$ < 90 mA; 5 V | 4.55 | – | | V |
| | | Active mode; I$_{CC}$ < 90 mA; 3 V | 2.80 | – | 3.2 | V |
| | | Active mode; single pulse of 100 mA for 2 µs; 5 V, fixed load = 25 mA | 4.6 | – | 5.25 | V |
| | | Active mode; single pulse of 100 mA for 2 µs; 3 V, fixed load = 25 mA | 2.76 | – | 3.2 | V |
| | | Active mode; current pulses of 40 nAs with peak |I$_{CC}$ | < 200 mA, t < 400 ns; 5 V | 4.6 | – | 5.25 | V |
| | | Active mode; current pulses of 40 nAs with peak |I$_{CC}$ | < 200 mA, t <400 ns; 3 V | 2.76 | – | 3.2 | V |
| I$_{CCmax}$ | Maximum supply current to the card | Static load current, V$_{CC}$>4.6 or 2.7 volts as selected | 90 | – | – | mA |
| I$_{CCF}$ | I$_{CC}$ fault current | | 100 | – | 150 | mA |
| V$_{SR}$ | Vcc slew rate, rise rate on activate | C$_F$ = 3.3 µF on V$_{CC}$ | 0.02 | 0.05 | 0.08 | V/µs |
| V$_{SF}$ | Vcc slew rate, fall rate on de-activate | C$_F$ = 3.3 µF on V$_{CC}$ | 0.025 | 0.06 | 0.08 | V/µs |
| C$_F$ | External filter capacitor (V$_{CC}$ to GND) | | 1 | 3.3 | 5 | µF |

| Symbol | Parameter | Condition | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| **Interface Requirements – Data Signals: I/O, AUX1, AUX2, and host interfaces: I/OUC, AUX1UC, AUX2UC. $I_{SHORTL}$, $I_{SHORTH}$, and $V_{INACT}$ requirements do not pertain to I/OUC, AUX1UC, AUX2UC.** | | | | | | |
| $V_{OH}$ | Output level, high (I/O, AUX1, AUX2) | $I_{OH} = 0$ μA | $0.9 * V_{CC}$ | – | $V_{CC}+0.1$ | V |
| | | $I_{OH} = -40$ μA | $0.75 * V_{CC}$ | – | $V_{CC}+0.1$ | V |
| $V_{OH}$ | Output level, high (I/OUC, AUX1UC, AUX2UC) | $I_{OH} = 0$ μA | $0.9 * V_{CC}$ | – | $V_{DD}+0.1$ | V |
| | | $I_{OH} = -40$ μA | $0.75 * V_{CC}$ | – | $V_{DD}+0.1$ | V |
| $V_{OL}$ | Output level, low | $I_{OL} = 1$ mA | – | – | 0.3 | V |
| $V_{IH}$ | Input level, high (I/O, AUX1, AUX2) | | 1.8 | – | $V_{CC}+0.30$ | V |
| $V_{IH}$ | Input level, high (I/OUC, AUX1UC, AUX2UC) | | 1.8 | – | $V_{CC}+0.30$ | V |
| $V_{IL}$ | Input level, low | | -0.3 | – | 0.8 | V |
| $V_{INACT}$ | Output voltage when outside of session | $I_{OL} = 0$ | – | – | 0.1 | V |
| | | $I_{OL} = 1$ mA | – | – | 0.3 | V |
| $I_{LEAK}$ | Input leakage | $V_{IH} = V_{CC}$ | – | – | 10 | μA |
| $I_{IL}$ | Input current, low | $V_{IL} = 0$ | – | – | 0.65 | mA |
| $I_{SHORTL}$ | Short circuit output current | For output low, shorted to $V_{CC}$ through 33 Ω | – | – | 15 | mA |
| $I_{SHORTH}$ | Short circuit output current | For output high, shorted to ground through 33 Ω | – | – | 15 | mA |
| $t_R$, $t_F$ | Output rise time, fall time | For I/O, AUX1, AUX2, $C_L = 80$ pF, 10% to 90%. For I/OUC, AUX1UC, AUX2UC, CL=50 pF, 10% to 90%. | – | – | 100 | ns |
| $t_{IR}$, $t_{IF}$ | Input rise, fall times | | – | – | 1 | μs |
| $R_{PU}$ | Internal pull-up resistor | Output stable for >200 ns | 8 | 11 | 14 | kΩ |
| $FD_{MAX}$ | Maximum data rate | | – | – | 1 | MHz |
| $T_{FDIO}$ | Delay, I/O to I/OUC, I/OUC to I/O, AUX1 to AUX1UC, AUX1UC to AUX1, AUX2 to AUX2UC, AUX2UC to AUX2 | Falling edge from master to slave measured at 50% point | 60 | 100 | 200 | ns |
| $T_{RDIO}$ | Delay, I/O to I/OUC, I/OUC to I/O, AUX1 to AUX1UC, AUX1UC to AUX1, AUX2 to AUX2UC, AUX2UC to AUX2 | Rising edge from master to slave measured at 50% point | – | 25 | 90 | ns |
| $C_{IN}$ | Input capacitance | | – | – | 10 | pF |

| Symbol | Parameter | Condition | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| **Reset and Clock for card interface, RST, CLK** | | | | | | |
| $V_{OH}$ | Output level, high | $I_{OH}$ = -200 μA | $0.9 * V_{CC}$ | – | $V_{CC}$ | V |
| $V_{OL}$ | Output level, low | $I_{OL}$ = 200 μA | 0 | – | 0.3 | V |
| $V_{INACT}$ | Output voltage when outside of session | $I_{OL}$ = 0 | – | – | 0.1 | V |
| | | $I_{OL}$ = 1 mA | – | – | 0.3 | V |
| $I_{RST\_LIM}$ | Output current limit, RST | | – | – | 30 | mA |
| $I_{CLK\_LIM}$ | Output current limit, CLK | | – | – | 70 | mA |
| $t_R$, $t_F$ | Output rise time, fall time | $C_L$ = 35 pF for CLK, 10% to 90% | – | – | 8 | ns |
| | | $C_L$ = 200 pF for RST, 10% to 90% | – | – | 100 | ns |
| δ | Duty cycle for CLK | $C_L$ =35 pF, $F_{CLK} \leq$ 20MHz | 45 | – | 55 | % |

## 2.4 Digital Signals Characteristics

Table 5 lists the 73S8010R digital signals characteristics.

**Table 5: Digital Signals Characteristics**

| Symbol | Parameter | Condition | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| **Digital I/O except for OSC I/O** | | | | | | |
| $V_{IL}$ | Input low voltage | | -0.3 | – | 0.8 | V |
| $V_{IH}$ | Input high voltage | | $0.7 * V_{DD}$ | – | $V_{DD}$+0.3 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 2 mA | | – | 0.45 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = -1 mA | $V_{DD}$-0.45 | – | | V |
| $R_{OUT}$ | Pull-up resistor; $\overline{INT}$ | | – | 20 | – | kΩ |
| $|I_{IL1}|$ | Input leakage current | GND < $V_{IN}$ < $V_{DD}$ | -5 | – | 5 | μA |
| **Oscillator (XTALIN) I/O** | | | | | | |
| $V_{ILXTAL}$ | Input low voltage - XTALIN | | -0.3 | – | 0.5 | V |
| $V_{IHXTAL}$ | Input high voltage - XTALIN | | $0.7*V_{DD}$ | – | $V_{DD}$+0.3 | V |
| $I_{ILXTAL}$ | Input current - XTALIN | GND < $V_{IN}$ < $V_{DD}$ | -30 | – | 30 | μA |

## 2.5 DC Characteristics

Table 6 lists the DC characteristics.

**Table 6: DC Characteristics**

| Symbol | Parameter | Condition | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current on $V_{DD}$ | | – | 1.5 | 3.0 | mA |
| $I_{PC}$ | Supply current on $V_{PC}$ | $V_{CC}$ on, $I_{CC}$ = 0 I/O, AUX1, AUX2 = high | – | 0.45 | 0.65 | mA |

## 2.6   I²C Interface Characteristics

Table 7 lists the I²C Interface characteristics.

**Table 7: I²C Characteristics**

| Symbol | Parameter | Condition | Min | Nom | Max | Unit |
|--------|-----------|-----------|-----|-----|-----|------|
| $V_{IL}$ | Input low voltage | | -0.3 | – | $0.3 * V_{DD}$ | V |
| $V_{IH}$ | Input high voltage | | $0.7 * V_{DD}$ | – | $V_{DD}+0.3$ | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 3 mA | – | – | 0.40 | V |
| $C_{IN}$ | Pin capacitance | | – | – | 10 | pF |
| $I_{IN}$ | Output high voltage | $I_{OH}$ = -1 mA | $V_{DD}$ - 0.45 | – | | V |
| $T_F$ | Output fall time | $C_L$ = 0 to 400 pF | $20 + 0.1*C_L$ | – | 250 | ns |
| $T_{SP}$ | Pulse width of spikes that are suppressed | Transition from valid logic level to opposite level | – | – | 50 | ns |

## 2.7   Voltage / Temperature Fault Detection Circuits

Table 8 lists the voltage / temperature fault detection circuits.

**Table 8: Voltage / Temperature Fault Detection Circuits**

| Symbol | Parameter | Condition | Min | Nom | Max | Unit |
|--------|-----------|-----------|-----|-----|-----|------|
| $V_{DDF}$ | $V_P$ over-current fault | No external resistor on VDDF_ADJ pin | 2.15 | – | 2.4 | V |
| $V_{PCF}$ | $V_{PC}$ fault ($V_{PC}$ Voltage Supervisor threshold) | $V_{PC} < V_{CC}$, a transient event | – | $V_{CC}$ - 0.2 | – | V |
| $V_{CCF}$ | $V_{CC}$ fault ($V_{CC}$ Voltage Supervisor threshold) | $V_{CC}$ = 5 V | 4.20 | – | 4.55 | V |
| | | $V_{CC}$ = 3 V | 2.5 | – | 2.7 | V |
| $T_F$ | Die over temperature fault | | 115 | – | 145 | °C |

# 3 Applications Information

This section provides general usage information for the design and implementation of the 73S8010R.

## 3.1 Example 73S8010R Schematics

Figure 4 shows a typical application schematic for the implementation of the 73S8010R. Note that minor changes may occur to the reference material from time to time and the reader is encouraged to contact Teridian for the latest information
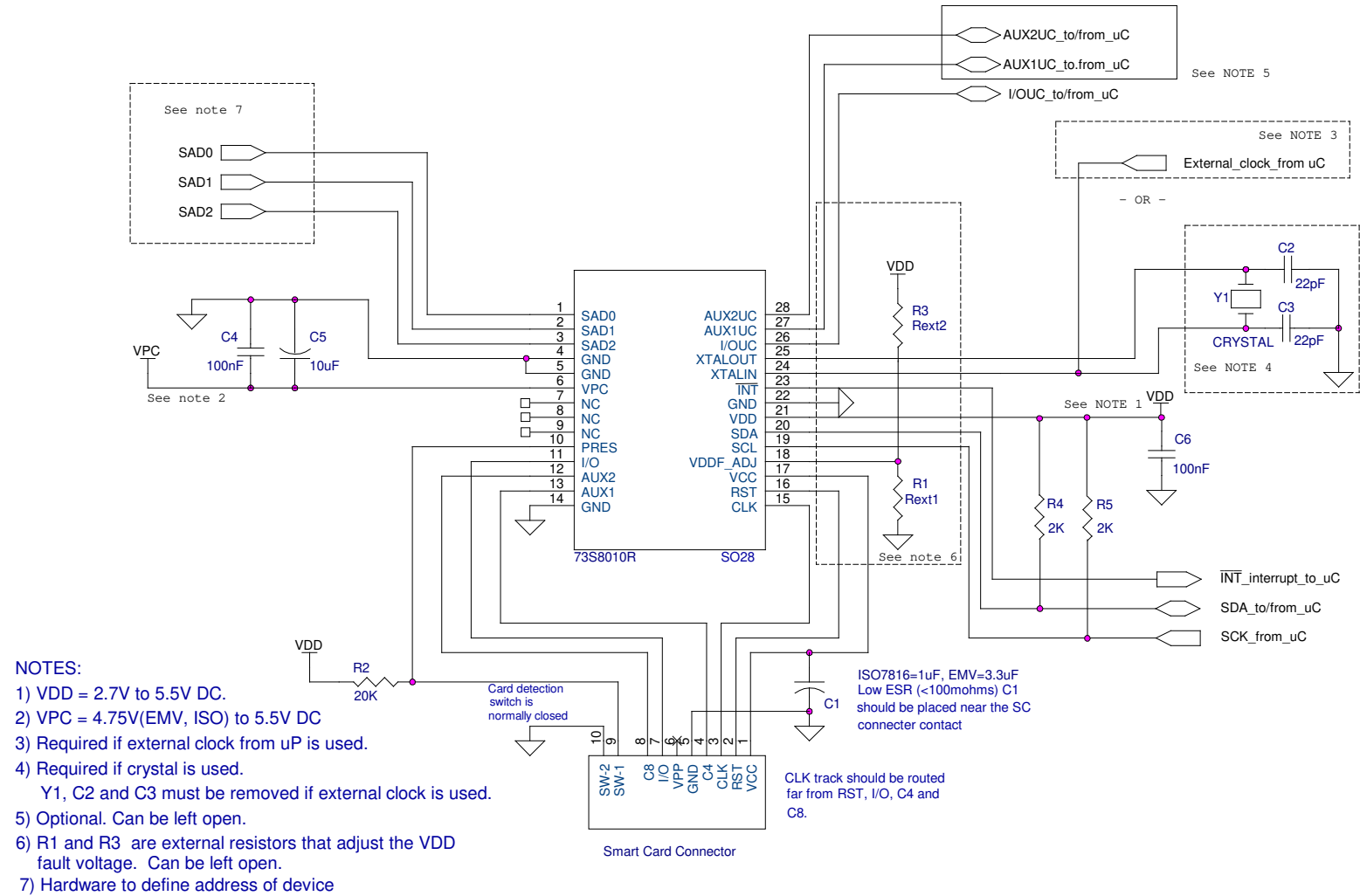
AUX2UC_to/from_uC
AUX1UC_to.from_uC
I/OUC_to/from_uC
See NOTE 5

See NOTE 3
External_clock_from uC
– OR –

See note 7
SAD0
SAD1
SAD2

C2 22pF
Y1
C3 22pF
CRYSTAL
See NOTE 4

VPC
C4 100nF
C5 10uF
See note 2

VDD
R3 Rext2

| | | 73S8010R SO28 | | |
|---|---|---|---|---|
| 1 | SAD0 | AUX2UC | 28 | |
| 2 | SAD1 | AUX1UC | 27 | |
| 3 | SAD2 | I/OUC | 26 | |
| 4 | GND | XTALOUT | 25 | |
| 5 | GND | XTALIN | 24 | |
| 6 | VPC | INT | 23 | |
| 7 | NC | GND | 22 | |
| 8 | NC | VDD | 21 | |
| 9 | NC | SDA | 20 | |
| 10 | PRES | SCL | 19 | |
| 11 | I/O | VDDF_ADJ | 18 | |
| 12 | AUX2 | VCC | 17 | |
| 13 | AUX1 | RST | 16 | |
| 14 | GND | CLK | 15 | |

See NOTE 1
VDD
C6 100nF

R1 Rext1
See note 6

R4 2K
R5 2K

INT_interrupt_to_uC
SDA_to/from_uC
SCK_from_uC

VDD
R2 20K

Card detection switch is normally closed

C1

ISO7816=1uF, EMV=3.3uF
Low ESR (<100mohms) C1
should be placed near the SC
connecter contact

Smart Card Connector

10 SW-2
9 SW-1
8 C8
7 I/O
6 VPP
5 GND
4 C4
3 CLK
2 RST
1 VCC

CLK track should be routed
far from RST, I/O, C4 and
C8.

NOTES:
1) VDD = 2.7V to 5.5V DC.
2) VPC = 4.75V(EMV, ISO) to 5.5V DC
3) Required if external clock from uP is used.
4) Required if crystal is used.
   Y1, C2 and C3 must be removed if external clock is used.
5) Optional. Can be left open.
6) R1 and R3 are external resistors that adjust the VDD
   fault voltage. Can be left open.
7) Hardware to define address of device

**Figure 4: Typical 73S8010R Application Schematic**

## 3.2   System Controller Interface (I²C Bus)

A fast-mode 400 kHz I²C bus slave interface is used for controlling the 73S8010R device and reading the status of the device via the data pin SDA and clock pin SCL.  The bus has 3 address select pins, SAD0, SAD1, and SAD2.  This allows up to 8 devices to be connected in parallel.  Table 9 lists the device address selections for the SAD2:0 settings.

**Table 9: Device Address Selection**

| SAD2 | SAD1 | SAD0 | (7 bit) I²C Address |
|------|------|------|---------------------|
| 0 | 0 | 0 | 0x40 |
| 0 | 0 | 1 | 0x42 |
| 0 | 1 | 0 | 0x44 |
| 0 | 1 | 1 | 0x46 |
| 1 | 0 | 0 | 0x48 |
| 1 | 0 | 1 | 0x4A |
| 1 | 1 | 0 | 0x4C |
| 1 | 1 | 1 | 0x4E |

Bit 0 of the I²C address is the R/W bit.  Refer to Figure 5 and Figure 6 for usage.

Table 10 describes the Control Register Bits.

**Table 10: Control Register Description**
**Power-on-reset value = 0x00**

| Name | Bit | Description |
|------|-----|-------------|
| Start/Stop | 0 | When set, initiates an activation and a cold reset procedure; when reset, initiates a deactivation sequence. |
| Warm reset | 1 | When set, initiates a warm reset procedure; automatically reset by hardware when the card starts answering or when the card is declared mute. |
| 5 V and 3 V | 2 | When set, $V_{CC}$ = 3 V; when reset, $V_{CC}$ = 5 V.  When de-activating (setting bit 0 = 0) and operating with 3 V (bit 2 =1), do not simultaneously set bit 2 =0. |
| Clock Stop | 3 | When set, the card clock is stopped.  Bit 4 determines the card clock stop level. |
| Clock Stop Level | 4 | When set, card clock stops high; when reset card clock stops low. |
| Clksel1 | 5 | Bits 5 and 6 determine the clock rate to the card.  See Table 11 for more details. |
| Clksel2 | 6 | |
| I/O enable | 7 | I/O enable bit.  When set, I/O is transferred on I/OUC; when reset I/O to I/OUC is high impedance. |

**Table 11: Card Clock Rate Selection**

| Bit Clksel2 | Bit Clksel1 | Card Clock |
|-------------|-------------|------------|
| 0 | 0 | Clkin/8 |
| 0 | 1 | Clkin/4 |
| 1 | 0 | Clkin/2 |
| 1 | 1 | Clkin (Xtalin) |

## I²C-bus Write to Control Register

The I²C-bus Write command to the control register follows the format shown in Figure 5.  After the START condition, the master sends a slave address.  This address is seven bits long followed by an eighth bit which is an opcode bit (R/W) – a 'zero' indicates the master will write data to the control register.  After the R/W bit, the 'zero' ACK bit is sent to the master by the device.  The master now starts sending the 8 bits of data to the control register during the DATA bits.  After the DATA bits, the 'zero' ACK bit is sent to the master by the device.  The master should send the STOP condition after receiving this ACK bit.
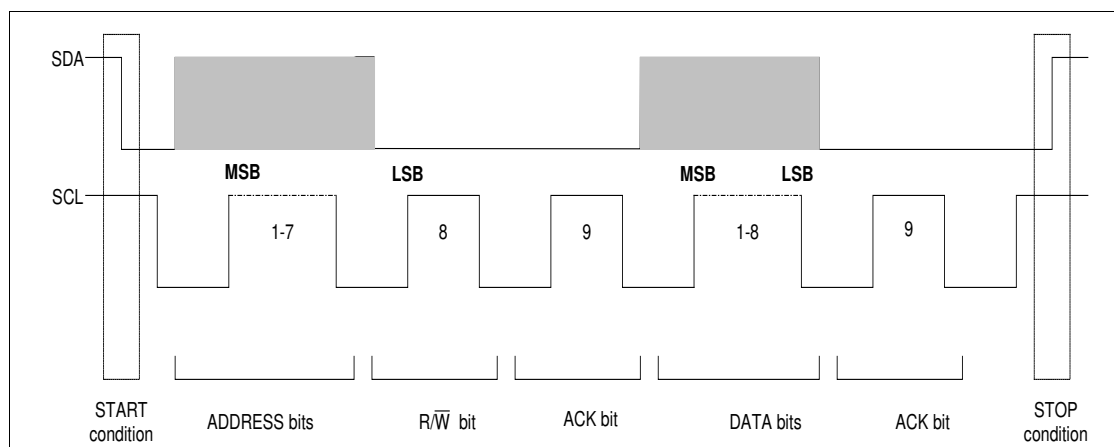


**Figure 5: I²C Bus Write Protocol**

Table 12 describes the Status Register bits.

**Table 12: Status Register Description**
**Power On Reset = 0x04**

| Name | Bit | Description |
|------|-----|-------------|
| PRES | 0 | Set when the card is present (pin PRES is high); reset when the card is not present. |
| PRESL | 1 | Set when the PRES pin changes state (rising/falling edge); reset when the status register is read.  Generates an interrupt when set. |
| I/O | 2 | Set when I/O is high; reset when I/O is low. |
| SUPL | 3 | Set when a voltage fault is detected; reset when the status register is read. Generates an interrupt when set. |
| PROT | 4 | Set when an over-current or over-heating fault has occurred during a card session; reset when the status register is read.  Generates an interrupt when set. |
| MUTE | 5 | Set during ATR when the card has not answered during the ISO 7816-3 time window (40000 card clock cycles); reset when the next session begins. |
| EARLY | 6 | Set during ATR when the card has answered before 400 card clock cycles; reset when the next session begins. |
| ACTIVE | 7 | Set when the card is active ($V_{CC}$ is on); reset when the card is inactive. |

## I²C-bus Read from Status Register

The I²C-bus Read Command from the Status Register follows the format shown in Figure 6.  After the START condition, the master sends a slave address.  This address is seven bits long followed by an eighth bit which is an opcode bit (R/W) – a 'one' indicates the master will read data from the status register.  After the R/W bit, the 'zero' ACK bit is sent to the master by the device.  The device now starts sending the 8-bit status register data to the control register during the DATA bits.  After the DATA bits, the 'one' ACK bit is sent to the device by the master.  The master should send the STOP condition after receiving the ACK bit.
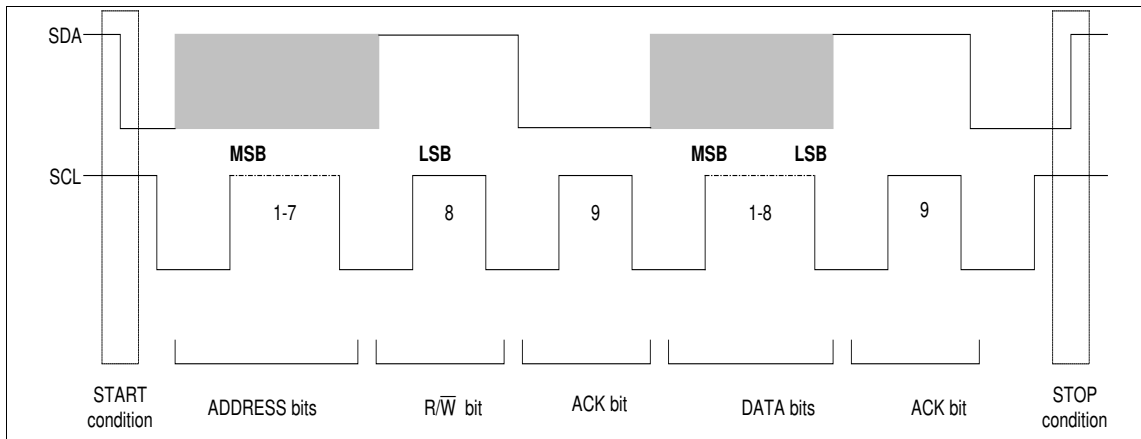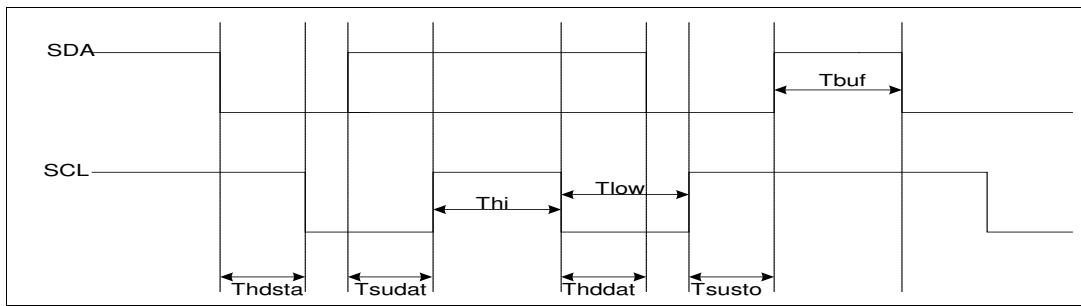
**Figure 6: I²C Bus Read Protocol**



**Figure 7: I²C Bus Timing Diagram**

**Table 13: I2C Bus Timing Parameters**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|-----------|------|------|------|------|
| Fsclk | Clock frequency | – | – | 400 | kHz |
| Tlow | Clock low | 1.3 | – | – | μs |
| Thi | Clock high | 0.6 | – | – | μs |
| Thdsta | Hold time START condition | 0.6 | – | – | μs |
| Tsudat | Data setup time | 100 | – | – | ns |
| Thddat | Data hold time | 5 | – | 900 | ns |
| Tsusto | Set up time STOP condition | 0.6 | – | – | μs |
| Tbuf | Bus free time between a STOP and START condition | 1.3 | – | – | μs |

## 3.3   Power Supply and Voltage Supervision

The Teridian 73S8010R smart card interface IC incorporates a LDO voltage regulator.  The voltage output is controlled by the digital input $5V/\overline{3V}$.  This regulator is able to provide either 3 V or 5 V card voltage from the power supply applied on the VPC pin.

Digital circuitry is powered by the power supply applied on the VDD pin.  $V_{DD}$ also defines the voltage range to interface with the system controller.

Three voltage supervisors constantly check the presence of the voltages $V_{DD}$, $V_{PC}$ and $V_{CC}$.  A card deactivation sequence is forced upon fault of any of these voltage supervisors.  The two voltage supervisors for $V_{PC}$ and $V_{CC}$ are linked so that a fault is generated to activate a deactivation sequence when the voltage $V_{PC}$ becomes lower than $V_{CC}$.  This allows the 73S8010R to operate at lower $V_{PC}$ voltage when using 3 V cards only.

The voltage regulator can provide a current of at least 90 mA on $V_{CC}$ which easily complies with the EMV 4.0 specification.  The $V_{PC}$ voltage supervisor threshold values are defined from the EMV 4.0 standard.  A third voltage supervisor monitors the $V_{DD}$ voltage.  It is used to initialize the ISO-7816-3 sequencer at power-on, and to deactivate the card at power-off or upon a fault.  The voltage threshold of the $V_{DD}$ voltage supervisor is internally set by default to 2.3 V nominal.  However, it may be desirable in some applications to modify this threshold value.  The pin VDDF_ADJ (pin 18 in the SO package, pin 17 in the QFN package) is used to connect an external resistor $R_{EXT}$ to ground to raise the $V_{DD}$ fault voltage to another value $V_{DDF}$.  The resistor value is defined as follows:

$$R_{EXT} = 56 \text{ k}\Omega / (V_{DDF} - 2.33)$$

An alternative (more accurate) method of adjusting the $V_{DD}$ fault voltage is to use a resistive network of R3 from the pin to supply and R1 from the pin to ground (see Figure 4).  In order to set the new threshold voltage, the equivalent resistance must be determined.  This resistance value will be designated Kx.  Kx is defined as R1/(R1+R3).  Kx is calculated as:

Kx = (2.789 / $V_{TH}$) - 0.6125 where $V_{TH}$ is the desired new threshold voltage.

To determine the values of R1 and R3, use the following formulas.

R3 = 24000 / Kx            R1 = R3*(Kx / (1 – Kx))

Taking the example above, where a $V_{DD}$ fault threshold voltage of 2.7 V is desired, solving for Kx gives:
        → Kx = (2.789 / 2.7) - 0.6125 = 0.42046.
Solving for R3 gives:       → R3 = 24000 / 0.42046 = 57080.
Solving for R1 gives:       → R1 = 57080 *(0.42046 / (1 – 0.42046)) = 41412.
Using standard 1 % resistor values gives R3 = 57.6 KΩ and R1 = 42.4 KΩ.
These values give an equivalent resistance of Kx = 0.4228, a 0.6% error.

If the 2.3 V default threshold is used, this pin must be left unconnected.

## 3.4  Card Power Supply

The card power supply is provided by the LDO regulator, and controlled by the digital ISO-7816-3 sequencer.  Card voltage selection is carried out by bit 2 of the control register.

**Choice of the $V_{CC}$ capacitor:**

Depending on the application, the requirements in terms of both the $V_{CC}$ minimum voltage and the transient currents that the interface must be able to provide to the card are different.  An external capacitor must be connected between the VCC pin and the card ground in order to guarantee stability of the LDO regulator, and to handle the transient requirements.  The type and value of this capacitor can be optimized to meet the desired specification.  Table 14 shows the recommended capacitors for each $V_{PC}$ power supply configuration and applicable specification.

### Table 14: Choice of VCC Pin Capacitor

| Specification Requirements | | | System Requirements | | |
|---|---|---|---|---|---|
| Specification | Min $V_{CC}$ Voltage allowed during transient current | Max Transient Current Charge | Min $V_{PC}$ Power Supply required | Capacitor Type | Capacitor Value |
| EMV 4.0 | 4.6 V | 30 nA·s | 4.75 V | X5R/X7R with ESR<100 mΩ | 3.3 ΩF |
| ISO-7816-3 | 4.5 V | 20 nA·s | 4.75 V | | 1 ΩF |

## 3.5  Over-temperature Monitor

A built-in detector monitors die temperature.  When an over-temperature condition occurs (resulting from a heavily loaded card interface, including short circuits, for example), a card deactivation sequence is initiated, and a fault condition is reported to the system controller (bit 4 of the status register is set and an interrupt is generated).

## 3.6  On-chip Oscillator and Card Clock

The Teridian 73S8010R device has an on-chip oscillator that can generate the smart card clock using an external crystal connected between the XTALIN and XTALOUT pins to set the oscillator frequency. When the card clock signal is available from another source, it can be connected to the pin XTALIN, and in this case, the XTALOUT pin should be left unconnected.

The card clock frequency may be chosen from 4 different division rates, defined by the Clksel2 and Clksel1 bits (bits 5 and 6) of the I$^2$C Control register, as listed in Table 15.

### Table 15: Card Clock Divisor Options

| Clksel2 | Clksel1 | Card Clock |
|---|---|---|
| 0 | 0 | Clkin / 8 |
| 0 | 1 | Clkin / 4 |
| 1 | 0 | Clkin / 2 |
| 1 | 1 | Clkin (Xtalin) |

## 3.7   Activation Sequence

After Power on Reset, the signal $\overline{INT}$ is low until the $V_{DD}$ is stable.  When $V_{DD}$ has been stable for approximately 10 ms and the signal $\overline{INT}$ is high, the system controller may read the status register to see if the card is present.  If all the status bits are satisfied, the system controller can initiate the activation sequence by writing a '1' to the Start/Stop bit (bit 0) of the control register.

The following steps and Figure 8 show the activation sequence and the timing of the card control signals when the system controller initiates the Start/Stop bit (bit 0) of the control register:

1.   Voltage $V_{CC}$ to the card should be valid by the end of $t_1$.  If $V_{CC}$ is not valid for any reason, then the session is aborted.
2.   Turn I/O to reception mode at the end of $t_1$.
3.   CLK is applied to the card at the end of $t_2$.
4.   RST (to the card) is set high at the end of $t_3$.



$t_1$ = 0.510 ms (timing by 1.5MHz internal Oscillator), I/O in reception mode
$t_2$ =1.5 µs, CLK starts
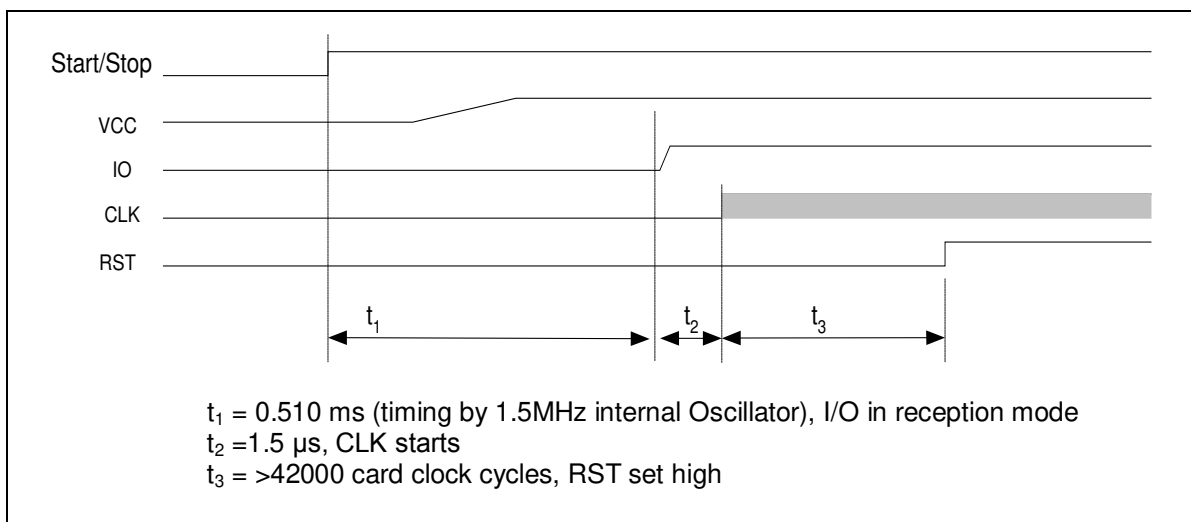$t_3$ = >42000 card clock cycles, RST set high

**Figure 8: Activation Sequence**

## 3.8   Deactivation Sequence

Deactivation is initiated either by the system controller by resetting the Start/Stop bit, or automatically in the event of hardware faults.  Hardware faults are over-current, over-temperature, $V_{DD}$ fault, $V_{PC}$ fault, $V_{CC}$ fault, and card extraction during the session.

The following steps and Figure 9 show the deactivation sequence and the timing of the card control signals when the system controller clears the start/stop bit:

1.   RST goes low at the end of $t_1$.
2.   CLK goes low at the end of $t_2$.
3.   I/O goes low at the end of $t_3$.  Out of reception mode.
4.   Shut down $V_{CC}$ at the end of time $t_4$.

$t_1 = > .5$ µs        $t_2 = > 7.5$ µs
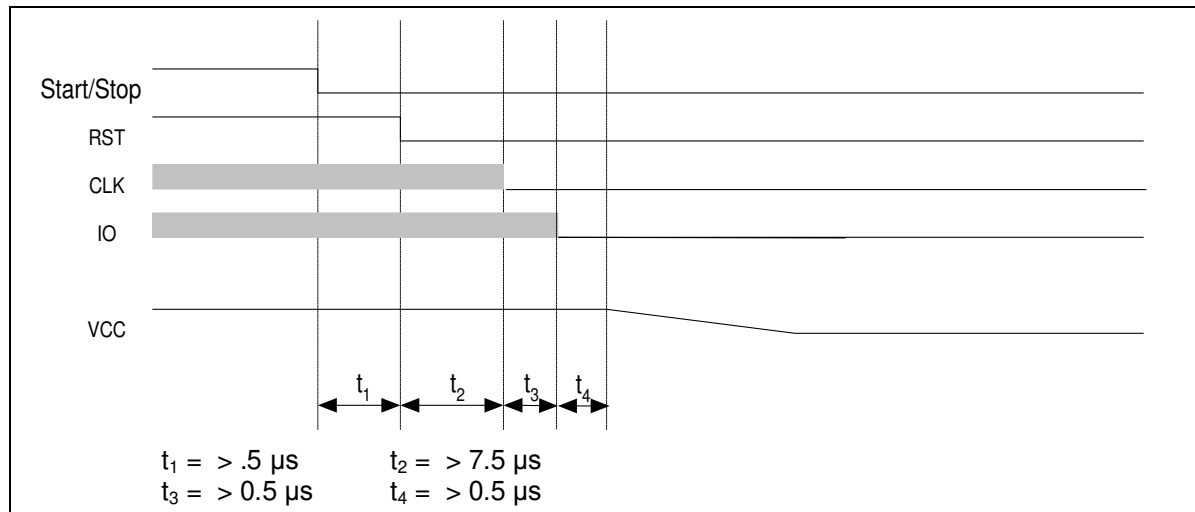$t_3 = > 0.5$ µs       $t_4 = > 0.5$ µs

**Figure 9: Deactivation Sequence**

## 3.9    Interrupt

The Interrupt is an active low interrupt.  It is set low if any of the following internal faults are detected:

- $V_{CC}$ fault
- $V_{DD}$ fault
- $V_{PC}$ fault

The interrupt will also be set if one of the following status bit conditions is detected:

- Early ATR
- Mute ATR
- Card insert or card extract
- Protection status from Over-current or Over-heating

When the interrupt is set low by the detection of one of the status bits, it is set high when the status bits are read.  (READ STATUS DONE)  Figure 10 shows the interrupt operation resulting from the fault or status bit conditions.
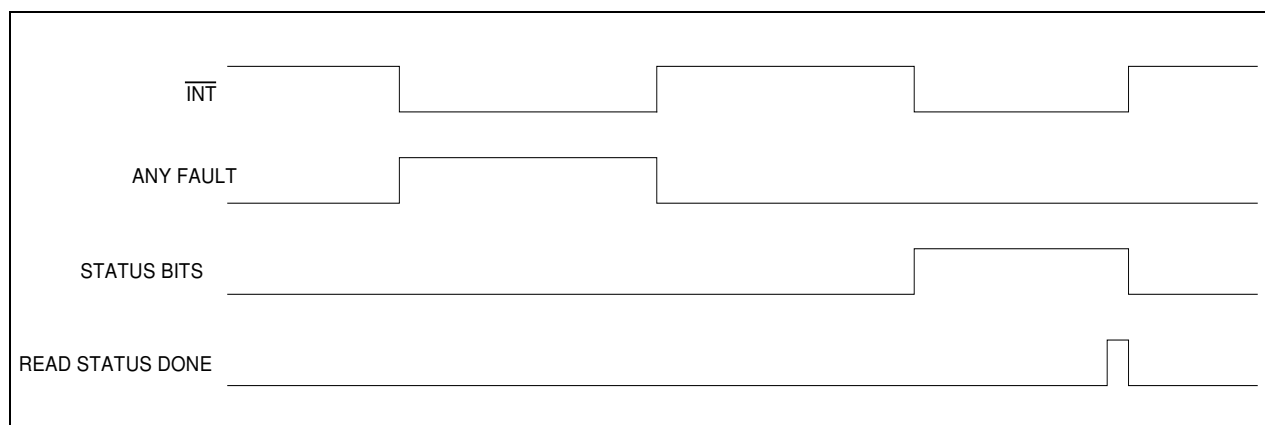


**Figure 10: Interrupt operation due to Fault and Status Conditions**

A power-on-reset event will reset all of the control and status registers to their default states.  A $V_{DD}$ fault event does not reset these registers, but it will signal an interrupt condition and by the action of the timer that creates the interval "$t_1$," not clearing the interrupt until $V_{DD}$ is valid for at least $t_1$.  A $V_{DD}$ fault can be considered valid for $V_{DD}$ as low as 1.5 to 1.8 volts.  At the lower range of $V_{DD}$ fault, POR will be asserted.

## 3.10  Warm Reset

The 73S8010R automatically asserts a warm reset to the card when instructed through bit 1 of the I$^2$C Control register (bit Warm Reset).  The warm reset length is automatically defined as 42,000 card clock cycles.  The Warm Reset bit is automatically reset when the card starts answering or when the card is declared mute.
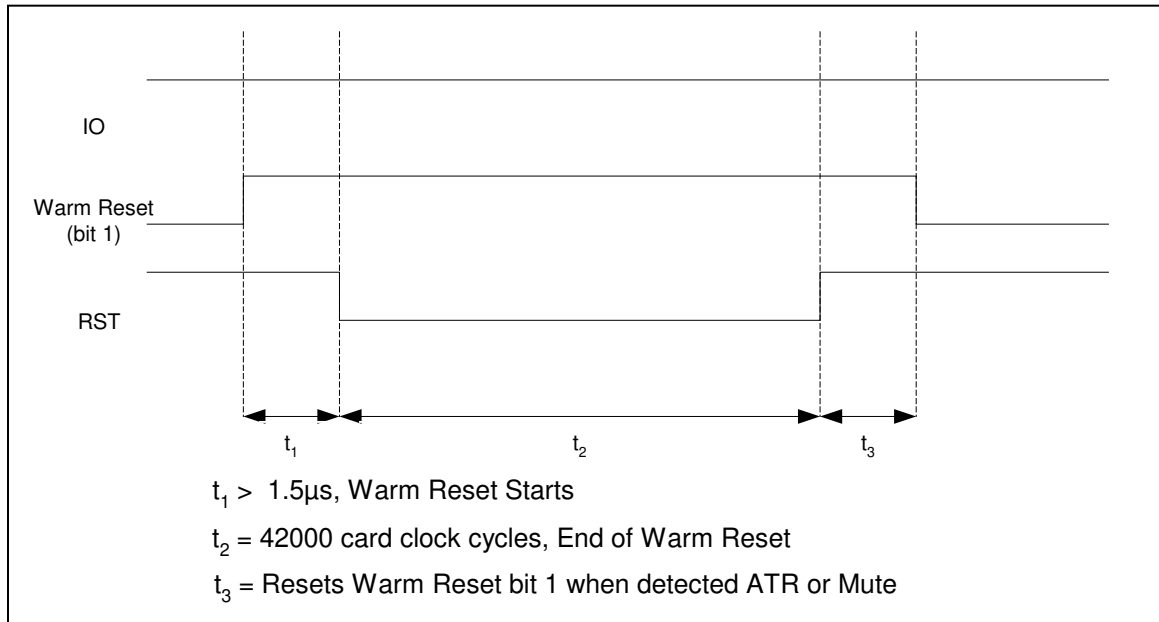


$t_1 >$  1.5µs, Warm Reset Starts

$t_2$ = 42000 card clock cycles, End of Warm Reset

$t_3$ = Resets Warm Reset bit 1 when detected ATR or Mute

**Figure 11: Warm Reset Operation**

## 3.11  I/O Circuitry and Timing

The states of the I/O, AUX1, and AUX2 pins are low after power-on-reset and they are high when the activation sequencer enables the I/O reception state.  See Section 3.7 Activation Sequence for more details on when the I/O reception is enabled.  The states of the I/OUC, AUX1UC, and AUX2UC are high after power on reset.

When the control I/O enable bit (bit 7) of the control register is set, the first I/O line on which a falling edge is detected becomes the input I/O line and the other becomes the output I/O line.  When the input I/O line rising edge is detected, then both I/O lines return to their neutral state.  The delay between these signals is shown in Figure 12.
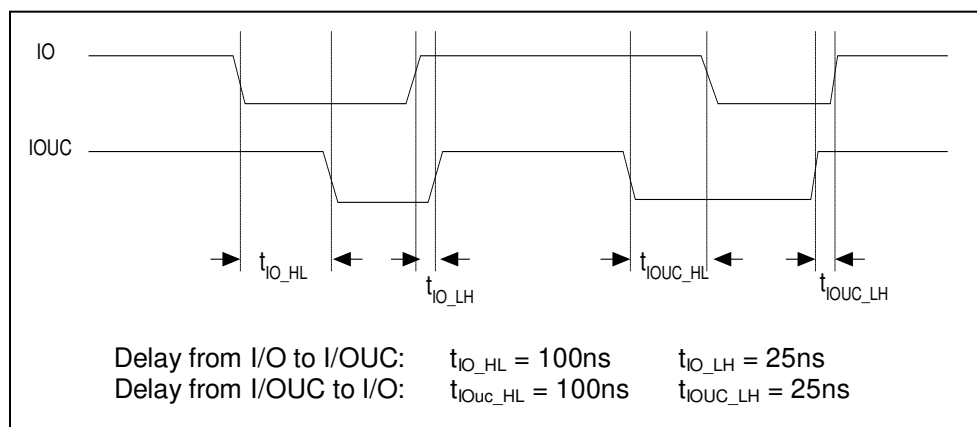


Delay from I/O to I/OUC:        $t_{IO\_HL}$ = 100ns        $t_{IO\_LH}$ = 25ns
Delay from I/OUC to I/O:        $t_{IOuc\_HL}$ = 100ns        $t_{IOUC\_LH}$ = 25ns

**Figure 12: I/O Timing Diagram**

# 4   Mechanical Drawings

## 4.1   32-pin QFN



**Figure 13: 32-pin QFN Package Dimensions**
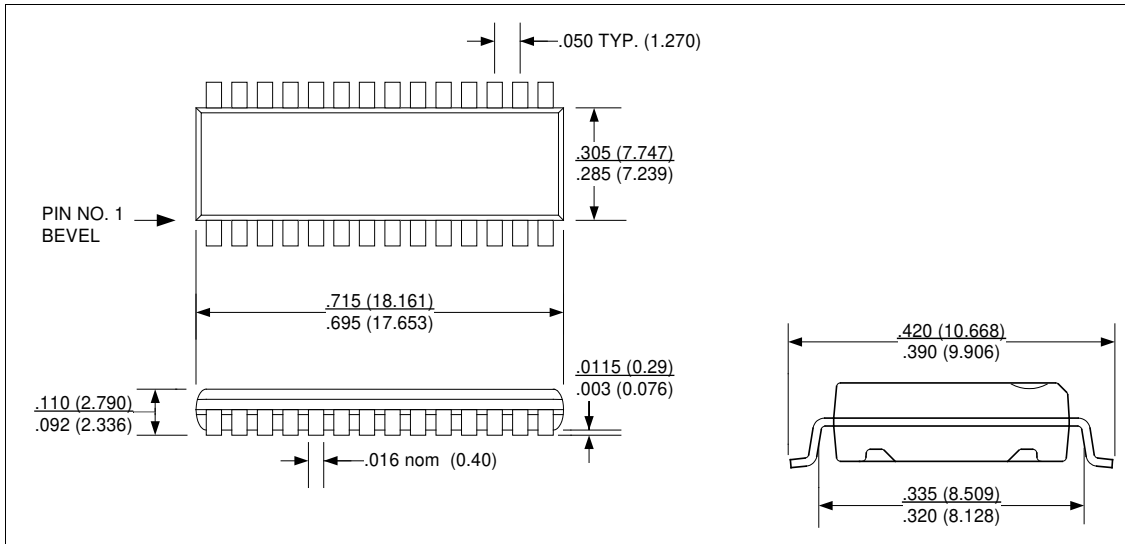
## 4.2 28-Pin SO



**Figure 14: 28-Pin SO Package Dimensions**

# 5    Ordering Information

Table 16 lists the order numbers and packaging marks used to identify 73S8010R products.

**Table 16: Order Numbers and Packaging Marks**

| Part Description | Order Number | Packaging Mark |
|---|---|---|
| 73S8010R–SOL, 28-pin Lead-Free SO | 73S8010R -IL/F | 73S8010R -IL |
| 73S8010R–SOL, 28-pin Lead-Free SO Tape / Reel | 73S8010R -ILR/F | 73S8010R -IL |
| 73S8010R–QFN, 32-pin Lead-Free QFN | 73S8010R -IM/F | 73S8010R |
| 73S8010R–QFN, 32-pin Lead-Free QFN Tape / Reel | 73S8010R -IMR/F | 73S8010R |

# 6    Related Documentation

The following 73S8010R documents are available from Teridian Semiconductor Corporation:

*73S8010R 28SO Demo Board User's Guide*

# 7    Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73S8010R, contact us at:

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For a complete list of worldwide sales offices, go to http://www.teridian.com.

## Revision History

| Revision | Date | Description |
|----------|------|-------------|
| 1.0 | 7/1/2004 | First publication. |
| 1.1 | 11/10/2004 | Make revisions to all references of "I/O" as it relates to the pins for the smart card and microcontroller interfaces, i.e. IO -> I/O and IOUC -> I/OUC. This is done to insure consistency and follow the designations used in ISO 7816.<br>Remove the MLP pin numbering in the pin description.<br>Correct the clock division table under CARD CLOCK.<br>Change the value of R2 on the typical application schematic. The original value is 100 KΩ and the updated value is 10 KΩ. The PRES input has a high impedance pull down resistor and the 100 KΩ for R2 is too high to insure a valid logic level on this input. |
| 1.3 | 10/26/2005 | Remove NDS references in application schematic. |
| 1.5 | 1/21/2008 | Removed leaded package option, replaced 32QFN punched with SAWN, updated 28SO dimension.<br>Changed dimension of bottom exposed pad on 32QFN mechanical package figure. |
| 1.6 | 8/28/2009 | Added Section 6, Related Documentation and Section 7, Contact Information.<br>Formatted to the corporate style. Added document number.<br>Miscellaneous editorial changes. |

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