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## **74ABT08**

# Quad 2-input AND gate Rev. 3 — 20 November 2015

**Product data sheet** 

#### 1. **General description**

The 74ABT08 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT08 is a quad 2-input AND gate.

#### 2. **Features and benefits**

- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C

#### **Ordering information** 3.

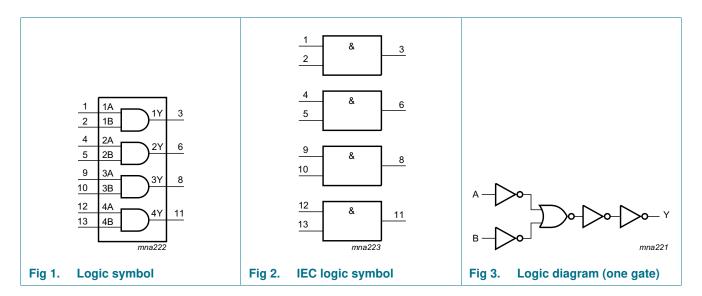
Table 1. **Ordering information** 

	Package											
	Temperature range	Name	Description	Version								
74ABT08D	–40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1								
74ABT08DB	–40 °C to +85 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1								
74ABT08PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1								



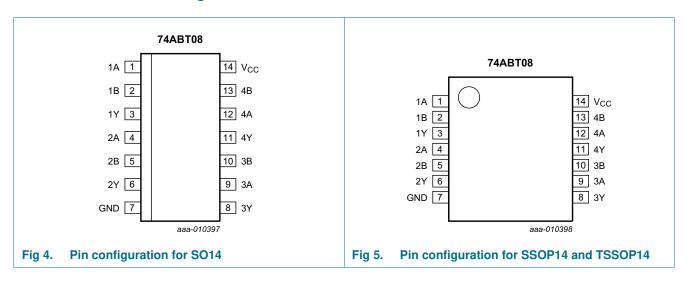
**Quad 2-input AND gate** 

## 4. Functional diagram



## 5. Pinning information

#### 5.1 Pinning



**Quad 2-input AND gate** 

## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 4A	1, 4, 9, 12	data input
1B to 4B	2, 5, 10, 13	data input
1Y to 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

Table 3. Function table[1]

Input		Output
nA	nB	nY
L	X	L
Х	L	L
Н	Н	Н

<sup>[1]</sup> H = HIGH voltage level; L = LOW voltage level; X = don't care.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7.0	V
VI	input voltage		[1]	-1.2	+7.0	V
Vo	output voltage	output HIGH or LOW	[1]	-0.5	+5.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V		-18	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V		-50	-	mA
Io	output current	output in LOW-state		-	40	mA
Tj	junction temperature		[2]	-	150	°C
T <sub>stg</sub>	storage temperature			-65	+150	°C

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>[2]</sup> The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

**Quad 2-input AND gate** 

## 8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CC</sub>	supply voltage		4.5	-	5.5	V
VI	input voltage		0	-	V <sub>CC</sub>	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
I <sub>OH</sub>	HIGH-level output current		-15	-	-	mA
I <sub>OL</sub>	LOW-level output current		-	-	20	mA
Δt/ΔV	input transition rise and fall rate		0	-	5	ns/V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C

## 9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions			25 °C		–40 °C t	o +85 °C	Unit
				Min	Тур	Max	Min	Max	
V <sub>IK</sub>	input clamping voltage	$V_{CC} = 4.5 \text{ V}; I_{IK} = -18 \text{ mA}$		-1.2	-0.9	-	-1.2	-	٧
V <sub>OH</sub>	HIGH-level output voltage	$V_{CC} = 4.5 \text{ V}; I_{OH} = -15 \text{ mA};$ $V_I = V_{IL} \text{ or } V_{IH}$		2.5	2.9	-	2.5	-	V
V <sub>OL</sub>	LOW-level output voltage	$V_{CC}$ = 4.5 V; $I_{OL}$ = 20 mA; $V_I$ = $V_{IL}$ or $V_{IH}$		-	0.35	0.5	-	0.5	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V		-	±0.01	±1.0	-	±1.0	μΑ
I <sub>OFF</sub>	power-off leakage current	$V_{CC} = 0 \text{ V}; \text{ V}_{I} \text{ or } \text{V}_{O} \le 4.5 \text{ V}$		-	±5.0	±100	-	±100	μΑ
I <sub>CEX</sub>	output high leakage current	HIGH-state; $V_O = 5.5 \text{ V}$ ; $V_{CC} = 5.5 \text{ V}$ ; $V_I = \text{GND or } V_{CC}$		-	5.0	50	-	50	μΑ
Io	output current	$V_{CC} = 5.5 \text{ V}; V_{O} = 2.5 \text{ V}$	<u>[1]</u>	-50	-75	-180	-50	-180	mA
I <sub>CC</sub>	supply current	$V_{CC} = 5.5 \text{ V}; V_I = \text{GND or } V_{CC}$		-	2	50	-	50	μΑ
Δl <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 5.5 V; one input at 3.4 V; other inputs at V <sub>CC</sub> or GND	[2]	-	0.25	500	-	500	μΑ
C <sub>I</sub>	input capacitance	V <sub>I</sub> = 0 V or V <sub>CC</sub>		-	3	-	-	-	pF

<sup>[1]</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>[2]</sup> This is the increase in supply current for each input at 3.4 V.

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## 10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; for test circuit, see Figure 7.

Symbol	Parameter	Conditions	25 °C	; V <sub>CC</sub> =	5.0 V	-40 °C to V <sub>CC</sub> = 5.0	Unit	
			Min	Тур	Max	Min	Max	
t <sub>PLH</sub>	LOW to HIGH propagation delay	nA, nB to nY; see Figure 6	1.0	2.4	3.4	1.0	4.0	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	nA, nB to nY; see Figure 6	1.0	1.9	2.8	1.0	3.0	ns
t <sub>sk(o)</sub>	output skew time	[1]	-	0.4	0.5	-	0.5	ns

<sup>[1]</sup> Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

#### 11. Waveforms

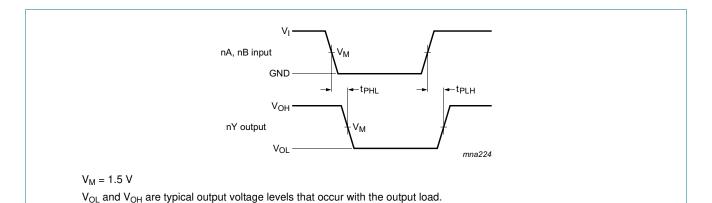
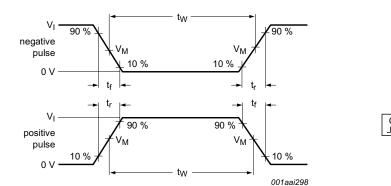
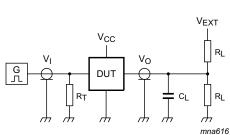


Fig 6. Propagation delay input (nA, nB) to output (nY) and output skew time

#### **Quad 2-input AND gate**





b. Test circuit

a. Input pulse definition

Test data is given in Table 8.

 $R_L$  = Load resistance.

 $C_L$  = Load capacitance including jig and probe capacitance.

 $R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

 $V_{\text{EXT}}$  = External voltage for measuring switching times.

Fig 7. Test circuit for measuring switching times

Table 8. Test data

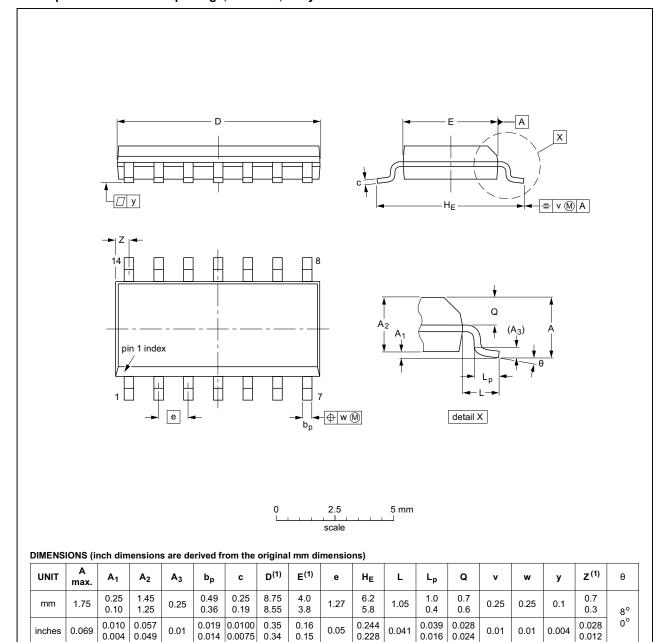
Input			Load	V <sub>EXT</sub>		
VI	f <sub>i</sub>	t <sub>W</sub>	t <sub>r</sub> , t <sub>f</sub>	CL	RL	t <sub>PHL</sub> , t <sub>PLH</sub>
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open

**Quad 2-input AND gate** 

## 12. Package outline

#### SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



#### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012				<del>99-12-27</del> 03-02-19

Fig 8. Package outline SOT108-1 (SO14)

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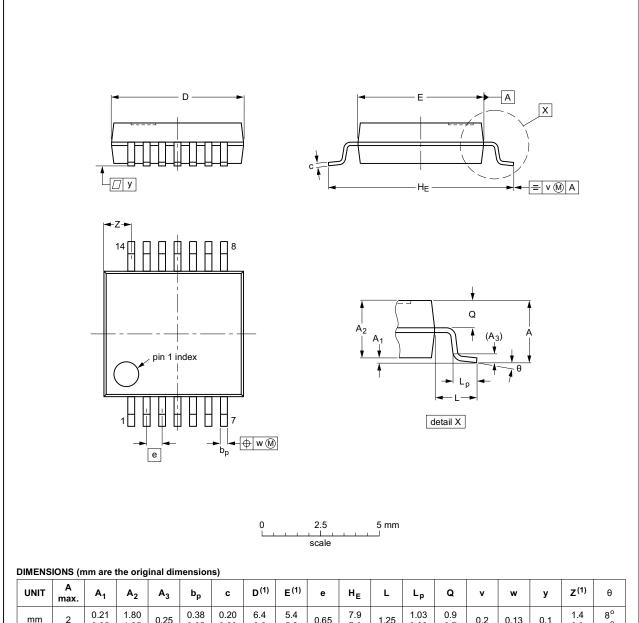
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**Quad 2-input AND gate** 

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	b <sub>p</sub>	C	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	<b>v</b>	w	у	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

#### Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT337-1		MO-150			<del>99-12-27</del> 03-02-19

Fig 9. Package outline SOT337-1 (SSOP14)

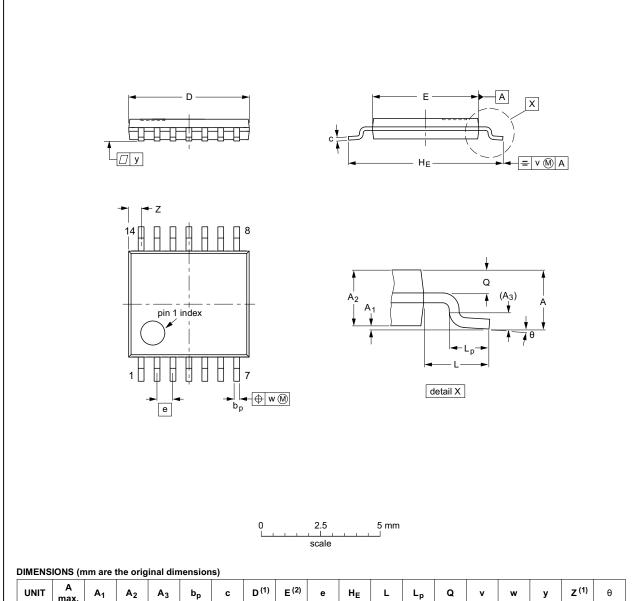
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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	bp	С	D <sup>(1)</sup>	E (2)	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

ISSUE DATE	EUROPEAN	RENCES	REFER		OUTLINE	
ISSUE DATE	PROJECTION	JEITA	JEDEC	IEC	VERSION	
<del>99-12-27</del> 03-02-18			MO-153		SOT402-1	
			MO-153		SOT402-1	

Fig 10. Package outline SOT402-1 (TSSOP14)

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## 13. Abbreviations

#### Table 9. Abbreviations

Acronym	Description	
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor	
DUT	Device Under Test	
ESD	ElectroStatic Discharge	
HBM	Human Body Model	
MM	Machine Model	

## 14. Revision history

#### Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT08 v.3	20151120	Product data sheet	-	74ABT08 v.2
Modifications:	Type number 74ABT08N (SOT27-1) removed.			
74ABT08 v.2	20140314	Product data sheet	-	74ABT08 v.1
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> </ul>			
	Legal texts have been adapted to the new company name where appropriate.			
74ABT08 v.1	19950918	Product specification	-	-

**Quad 2-input AND gate** 

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#### 15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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