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74ABT162244

16-Bit Buffer/Line Driver with 25Ω Series Resistors in the Outputs

General Description

The ABT162244 contains sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual 3-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

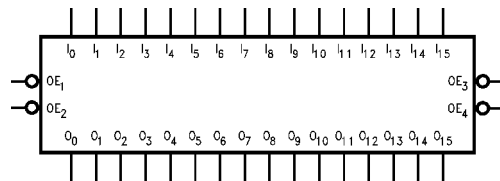
Features

- Separate control logic for each nibble
- 16-bit version of the ABT2244
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

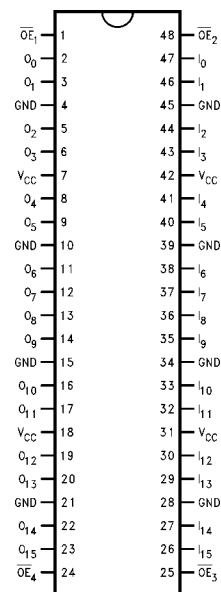
Ordering Code:

Order Number	Package Number	Package Description
74ABT162244CSSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ABT162244CSSX	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ABT162244CMTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
74ABT162244MTDX	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
I_0-I_{15}	Inputs
O_0-O_{15}	Outputs

74ABT162244 16-Bit Buffer/Line Driver with 25Ω Series Resistors in the Outputs

Truth Tables

Inputs		Outputs
\overline{OE}_1	I_0-I_3	O_0-O_3
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_3	I_8-I_{11}	O_8-O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_2	I_4-I_7	O_4-O_7
L	L	L
L	H	H
H	X	Z

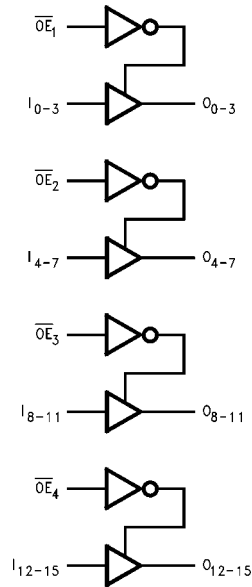
Inputs		Outputs
\overline{OE}_4	$I_{12}-I_{15}$	$O_{12}-O_{15}$
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

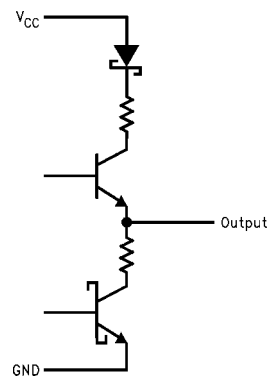
Functional Description

The ABT162244 contains sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Logic Diagram



Schematic of each Output



Absolute Maximum Ratings(Note 1)

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +150°C
V _{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	–0.5V to 5.5V
in the HIGH State	–0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current	–500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	–40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			–1.2	V	Min	I _{IN} = –18 mA
V _{OH}	Output HIGH Voltage	2.5			V	Min	I _{OH} = –3 mA
		2.0			V	Min	I _{OH} = –32 mA
V _{OL}	Output LOW Voltage			0.8	V	Min	I _{OL} = 12 mA
I _{IH}	Input HIGH Current			1	μA	Max	V _{IN} = 2.7V (Note 3)
				1	μA	Max	V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			–1	μA	Max	V _{IN} = 0.5V (Note 3)
				–1	μA	Max	V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OZH}	Output Leakage Current			10	μA	0 – 5.5V	V _{OUT} = 2.7V; \overline{OE}_n = 2.0V
I _{OZL}	Output Leakage Current			–10	μA	0 – 5.5V	V _{OUT} = 0.5V; \overline{OE}_n = 2.0V
I _{OS}	Output Short-Circuit Current	–100		–275	mA	Max	V _{OUT} = 0.0V
I _{CEx}	Output High Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test			100	μA	0.0	V _{OUT} = 5.5V; All Others GND
I _{CCH}	Power Supply Current			2.0	mA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current			60	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current			2.0	mA	Max	\overline{OE}_n = V _{CC} All Others at V _{CC} or GND
I _{CCT}	Additional I _{CC} /Input			3.0	mA		V _I = V _{CC} – 2.1V
	Outputs Enabled			3.0	mA	Max	Enable Input V _I = V _{CC} – 2.1V
	Outputs 3-STATE			3.0	mA		Data Input V _I = V _{CC} – 2.1V
	Outputs 3-STATE			50	μA		All Others at V _{CC} or GND
I _{CCD}	Dynamic I _{CC} (Note 3)			0.1	mA/ MHz	Max	Outputs OPEN \overline{OE}_n = GND One Bit Toggling, 50% Duty Cycle

Note 3: Guaranteed, but not tested.

AC Electrical Characteristics

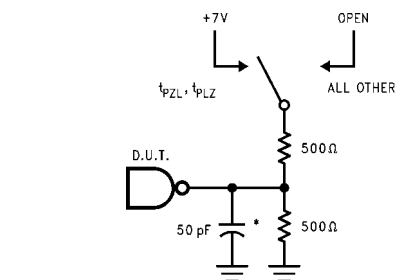
Symbol	Parameter	T _A = +25°C V _{CC} = +5V C _L = 50 pF			T _A = -40°C to +85°C V _{CC} = 4.5V–5.5V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t _{PLH}	Propagation	1.0	2.4	3.9	1.0	3.9	ns
t _{PHL}	Delay Data to Outputs	1.0	3.2	4.7	1.0	4.7	
t _{PZH}	Output	1.5	3.5	6.3	1.5	6.3	ns
t _{PZL}	Enable Time	1.5	4.2	6.9	1.5	6.9	
t _{PHZ}	Output	1.0	4.2	6.7	1.0	6.7	ns
t _{PLZ}	Disable Time	1.0	3.8	6.7	1.0	6.7	

Capacitance

Symbol	Parameter	Typ	Units	Conditions T _A = 25°C
C _{IN}	Input Capacitance	5.0	pF	V _{CC} = 0.0V
C _{OUT} (Note 4)	Output Capacitance	9.0	pF	V _{CC} = 5.0V

Note 4: C_{OUT} is measured at frequency f = 1 MHz per MIL-STD-883, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

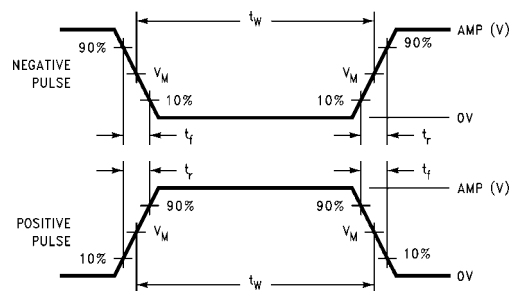


FIGURE 2. Input Pulse Requirements
 $V_M = 1.5V$

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

AC Waveforms

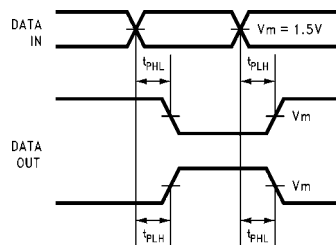


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

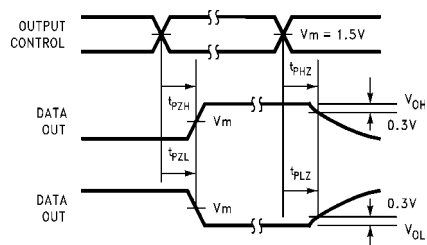


FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times

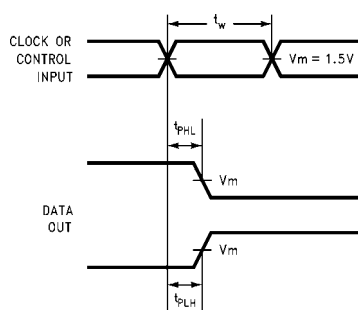


FIGURE 5. Propagation Delay, Pulse Width Waveforms

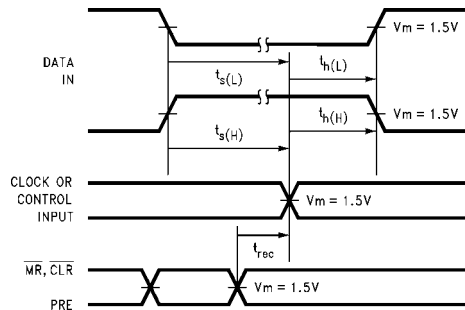
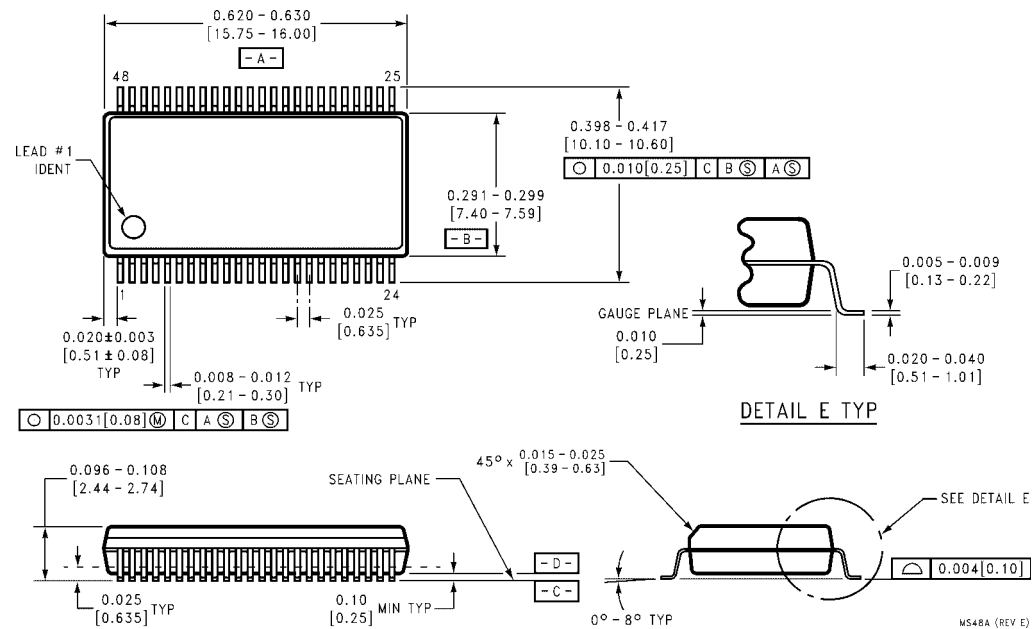
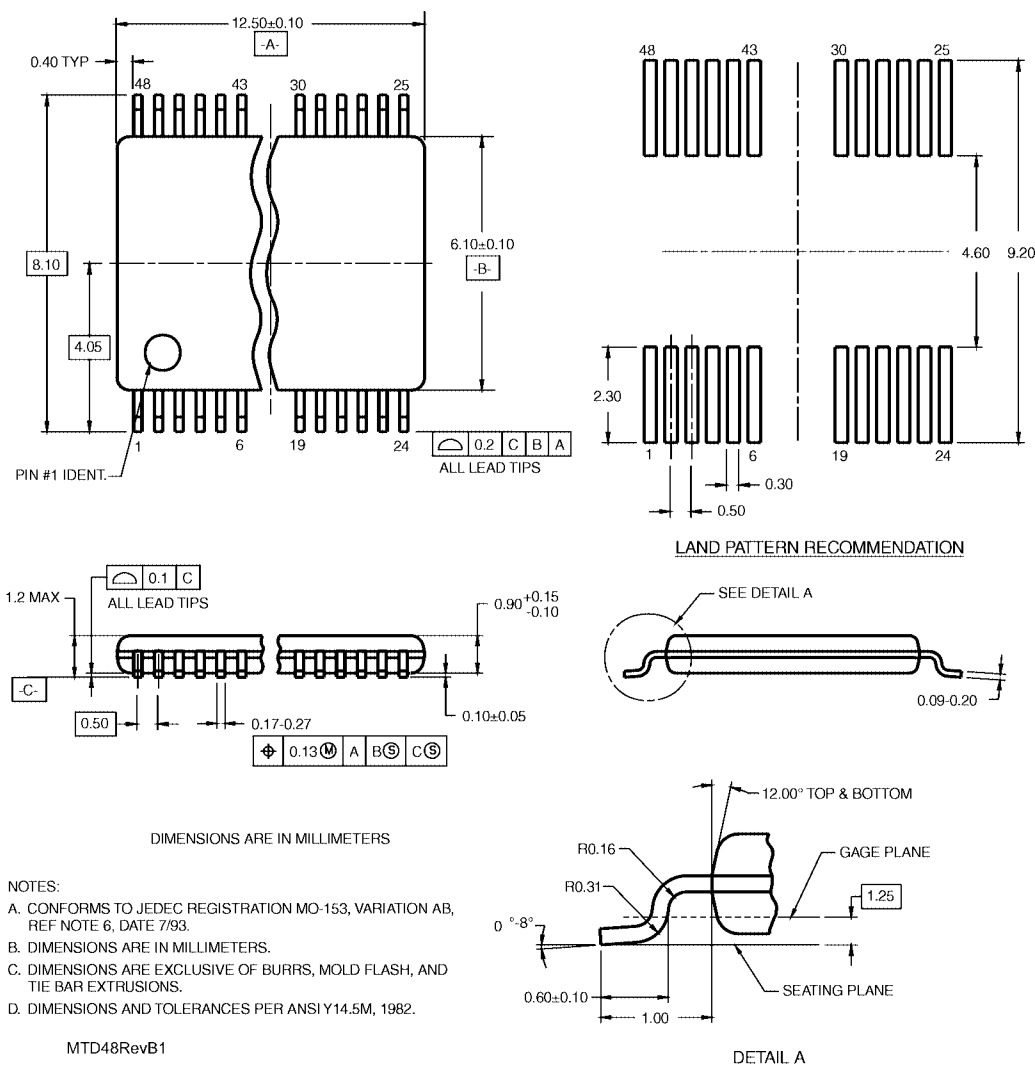


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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