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FAIRCHILD

SEMICONDUCTOR ™

74ABT244
Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The ABT244 is an octal buffer and line driver with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver.

Features

- Non-inverting buffers
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Disable time less than enable time to avoid bus contention

Ordering Code:

Order Number	Package Number	Package Description
74ABT244CSC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ABT244CSJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT244CMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ABT244CMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ABT244CPC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram
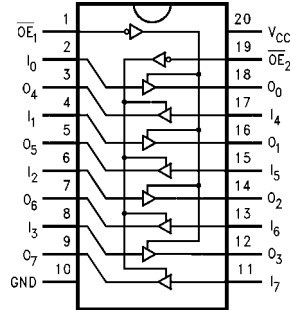
Pin Descriptions

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input (Active LOW)
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Table

$\overline{OE}_1$	I_{0-3}	O_{0-3}	$\overline{OE}_2$	I_{4-7}	O_{4-7}
H	X	Z	H	X	Z
L	H	H	L	H	H
L	L	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-Off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	−40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

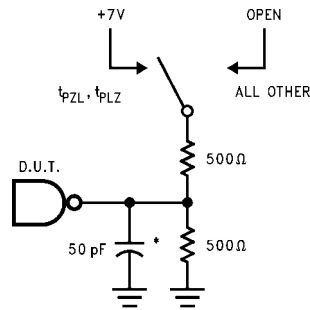| Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	$I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage		2.5			V	Min	$I_{OH} = -3$ mA
			2.0			V	Min	$I_{OH} = -32$ mA
V_{OL}	Output LOW Voltage				0.55			$I_{OL} = 64$ mA
I_{IH}	Input HIGH Current				1	µA	Max	$V_{IN} = 2.7$V (Note 4)
					1			$V_{IN} = V_{CC}$
I_{BVI}	Input HIGH Current Breakdown Test				7	µA	Max	$V_{IN} = 7.0$V
I_{IL}	Input LOW Current				−1	µA	Max	$V_{IN} = 0.5$V (Note 4)
					−1			$V_{IN} = 0.0$V
V_{ID}	Input Leakage Test		4.75			V	0.0	$I_{ID} = 1.9$ µA
								All Other Pins Grounded
I_{OZH}	Output Leakage Current				10	µA	0 − 5.5V	$V_{OUT} = 2.7$V; $\overline{OE}_n = 2.0$V
I_{OZL}	Output Leakage Current				−10	µA	0 − 5.5V	$V_{OUT} = 0.5$V; $\overline{OE}_n = 2.0$V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	$V_{OUT} = 0.0$V
I_{CEX}	Output High Leakage Current				50	µA	Max	$V_{OUT} = V_{CC}$
I_{ZZ}	Bus Drainage Test				100	µA	0.0	$V_{OUT} = 5.5$V; All Others GND
I_{CCH}	Power Supply Current				50	µA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	µA	Max	$\overline{OE}_n = V_{CC}$, All Others at V_{CC} or Ground
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA		$V_I = V_{CC} - 2.1$V
		Outputs 3-STATE			2.5	mA	Max	Enable Input $V_I = V_{CC} - 2.1$V
		Outputs 3-STATE			50	µA		Data Input $V_I = V_{CC} - 2.1$V All Others at V_{CC} or Ground
I_{CCD}	Dynamic I_{CC} (Note 4)	No Load			0.1	mA/ MHz	Max	Outputs OPEN $\overline{OE}_n = $ GND, (Note 3) One Bit Toggling, 50% Duty Cycle

Note 3: For 8 bits toggling, $I_{CCD} < 0.8$ mA/MHz.

Note 4: Guaranteed, but not tested.

DC Electrical Characteristics

(SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.5	0.8	V	5.0	$T_A = 25°C$ (Note 5)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.3	−0.8		V	5.0	$T_A = 25°C$ (Note 5)
V_{OHV}	Minimum HIGH Level Dynamic Output Voltage	2.7	3.1		V	5.0	$T_A = 25°C$ (Note 7)
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	2.0	1.5		V	5.0	$T_A = 25°C$ (Note 6)
V_{ILD}	Maximum LOW Level Dynamic Input Voltage		1.1	0.8	V	5.0	$T_A = 25°C$ (Note 6)

Note 5: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 6: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 7: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics

(SOIC and SSOP package)

Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5V$ $C_L = 50$ pF			$T_A = −55°C$ to $+125°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 50$ pF		$T_A = −40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	1.0	2.5	3.6	1.0	5.3	1.0	3.6	ns
t_{PHL}	Data to Outputs	1.0	2.3	3.6	1.0	5.0	1.0	3.6	
t_{PZH}	Output Enable	1.5	3.5	6.0	0.8	6.5	1.5	6.0	ns
t_{PZL}	Time	1.5	3.6	6.0	1.2	7.9	1.5	6.0	
t_{PHZ}	Output Disable	1.7	3.5	5.6	1.2	7.6	1.7	5.6	ns
t_{PLZ}	Time	1.7	3.3	5.6	1.0	7.9	1.7	5.6	

Extended AC Electrical Characteristics

(SOIC package)

Symbol	Parameter	T_A−40°C to +85°C $V_{CC} = 4.5V–5.5V$ $C_L = 50$ pF 8 Outputs Switching (Note 8)			$T_A = −40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 250$ pF 1 Output Switching (Note 9)		$T_A = −40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 250$ pF 8 Outputs Switching (Note 10)		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{TOGGLE}	Max Toggle Frequency		100						MHz
t_{PLH}	Propagation Delay	1.5		5.0	1.5	6.0	2.5	8.5	ns
t_{PHL}	Data to Outputs	1.5		5.0	1.5	6.0	2.5	8.5	
t_{PZH}	Output Enable Time	1.5		6.5	2.5	7.5	2.5	10.0	ns
t_{PZL}		1.5		6.5	2.5	7.5	2.5	12.0	
t_{PHZ}	Output Disable Time	1.0		5.6	(Note 11)		(Note 11)		ns
t_{PLZ}		1.0		5.6					

Note 8: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 9: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 10: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 11: The 3-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.

Skew

Symbol	Parameter	$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 50$ pF 8 Outputs Switching (Note 14) Max	$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 250$ pF 8 Outputs Switching (Note 15) Max	Units
t_{OSHL} (Note 12)	Pin to Pin Skew HL Transitions	0.8	1.8	ns
t_{OSLH} (Note 12)	Pin to Pin Skew LH Transitions	0.8	1.8	ns
t_{PS} (Note 16)	Duty Cycle LH–HL Skew	1.0	2.5	ns
t_{OST} (Note 12)	Pin to Pin Skew LH/HL Transitions	1.0	2.5	ns
t_{PV} (Note 13)	Device to Device Skew LH/HL Transitions	1.5	3.0	ns

Note 12: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}), LOW-to-HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t_{OST}). The specification is guaranteed but not tested.

Note 13: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 14: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.)

Note 15: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 16: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$
C_{OUT} (Note 17)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$

Note 17: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

AC Loading

+7V   OPEN

t_{PZL}, t_{PLZ} ALL OTHER

D.U.T.

500 Ω

50 pF   *   500 Ω

*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

AC Waveforms

t_W

90%   AMP (V)

NEGATIVE
PULSE V_M V_M

90%

10%   10%   0V

t_f t_r

t_r t_f

AMP (V)

POSITIVE
PULSE   90%   90%

V_M V_M

10%   10%   0V

t_W

$V_M = 1.5V$
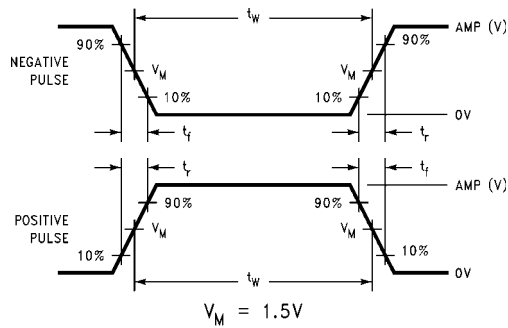
FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

t_W

CLOCK OR
CONTROL
INPUT   Vm = 1.5V

t_{PHL}

Vm

DATA
OUT

Vm

t_{PLH}
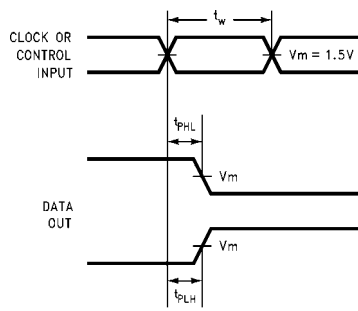
**FIGURE 4. Propagation Delay,
Pulse Width Waveforms**

OUTPUT
CONTROL   Vm = 1.5V

t_{PHZ}

t_{PZH} V_{OH}

DATA
OUT   Vm   0.3V

t_{PZL} t_{PLZ}

DATA
OUT   Vm   0.3V

V_{OL}
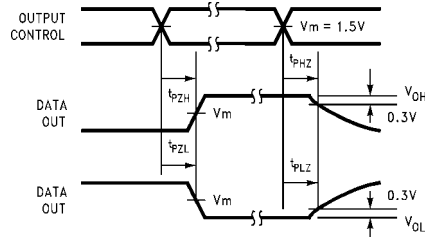
**FIGURE 5. 3-STATE Output HIGH
and LOW Enable and Disable Times**

DATA
IN   Vm = 1.5V

t_{PHL} t_{PLH}

Vm

DATA
OUT

Vm

t_{PLH} t_{PHL}

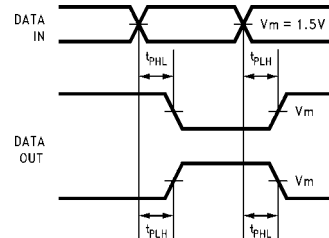**FIGURE 6. Propagation Delay Waveforms for
Inverting and Non-Inverting Functions**

DATA
IN   Vm = 1.5V

$t_{s(L)}$ $t_{h(L)}$

$t_{h(H)}$ Vm = 1.5V

$t_{s(H)}$

CLOCK OR
CONTROL
INPUT   Vm = 1.5V

t_{rec}
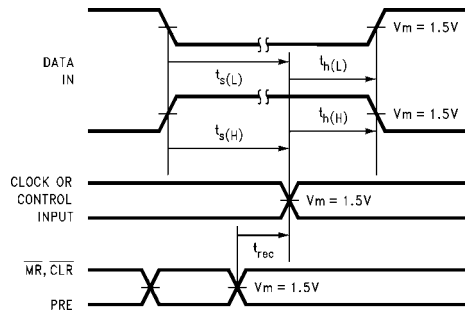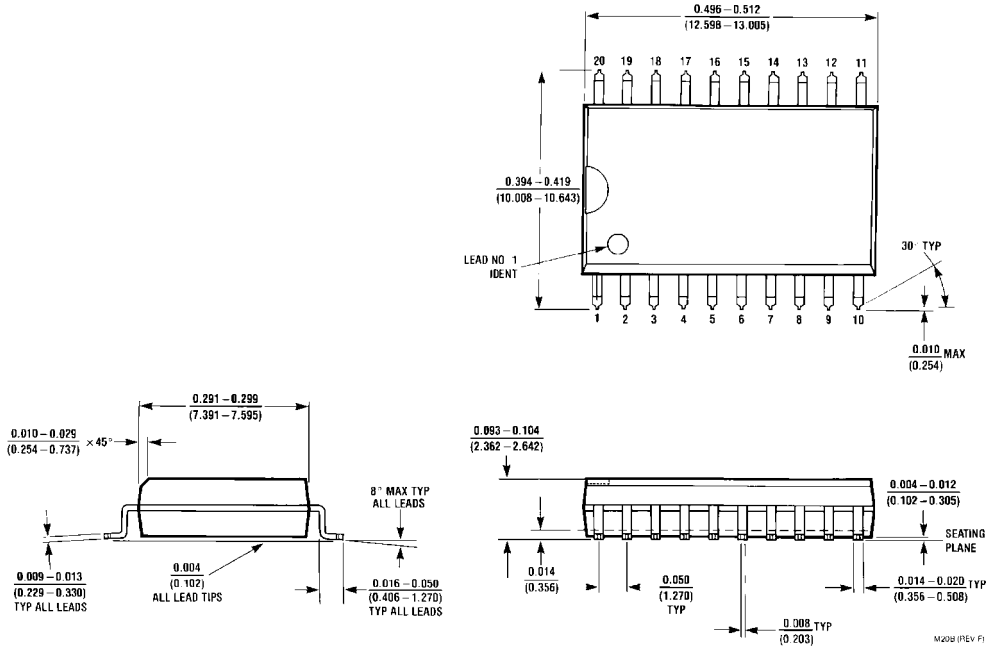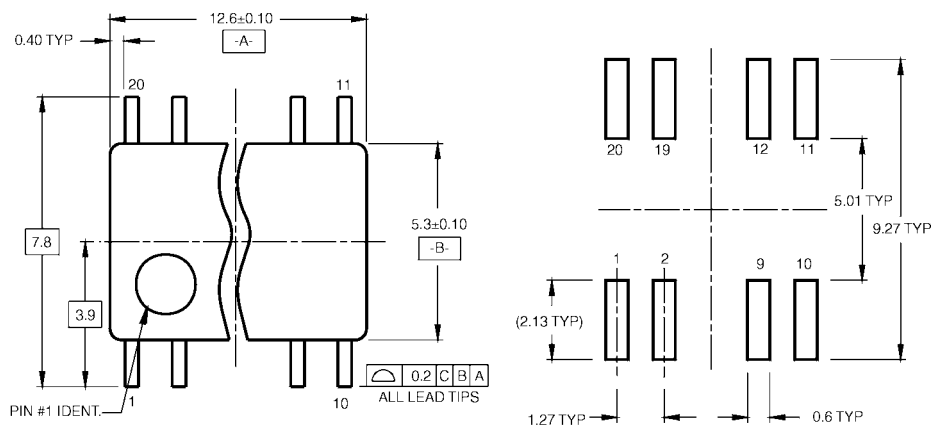
$\overline{MR}, \overline{CLR}$ Vm = 1.5V

PRE

**FIGURE 7. Setup Time, Hold Time
and Recovery Time Waveforms**

Physical Dimensions inches (millimeters) unless otherwise noted

0.496 – 0.512
(12.598 – 13.005)

20 19 18 17 16 15 14 13 12 11

0.394 – 0.419
(10.008 – 10.643)

LEAD NO. 1
IDENT

30° TYP

1 2 3 4 5 6 7 8 9 10

0.010 MAX
(0.254)

0.291 – 0.299
(7.391 – 7.595)

0.010 – 0.029
(0.254 – 0.737) × 45°

8° MAX TYP
ALL LEADS

0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS

0.093 – 0.104
(2.362 – 2.642)

0.004 – 0.012
(0.102 – 0.305)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008 TYP
(0.203)

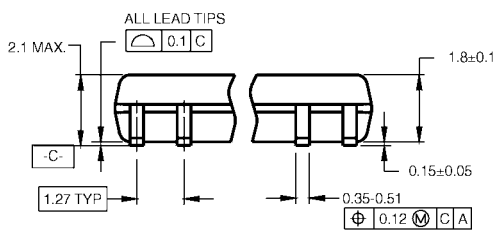0.014 – 0.020 TYP
(0.356 – 0.508)

M20B (REV F)

20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

12.6±0.10

-A-

0.40 TYP

20   11

7.8

5.3±0.10

-B-

3.9

PIN #1 IDENT.   1   10

⌓ 0.2 C B A

ALL LEAD TIPS

ALL LEAD TIPS

⌓ 0.1 C

2.1 MAX.

-C-

1.8±0.1

1.27 TYP

0.15±0.05

0.35-0.51

⊕ 0.12 Ⓜ C A

DIMENSIONS ARE IN MILLIMETERS

20   19   12   11

5.01 TYP

9.27 TYP

1   2   9   10

(2.13 TYP)

1.27 TYP   0.6 TYP

LAND PATTERN RECOMMENDATION

SEE DETAIL A

0.15-0.25

7° TYP

GAGE PLANE

0.25

0°-8° TYP

0.60±0.15

1.25

SEATING PLANE
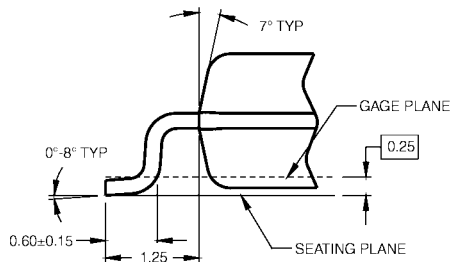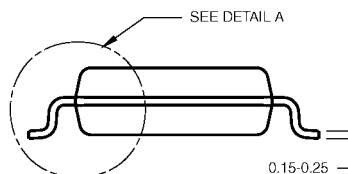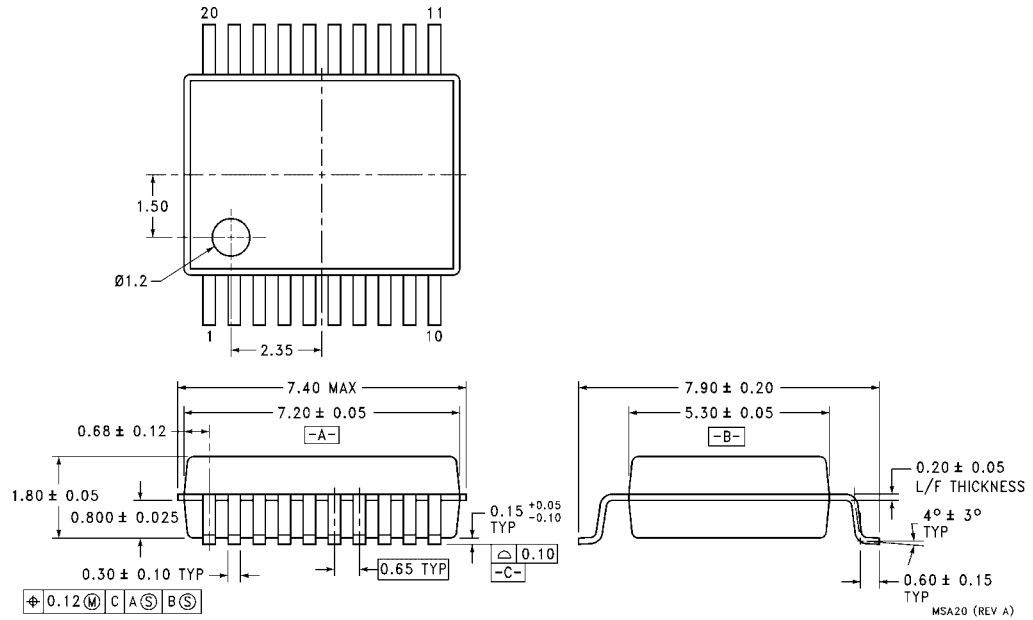
DETAIL A

NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

B. DIMENSIONS ARE IN MILLIMETERS.

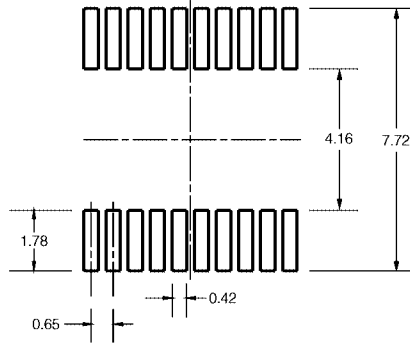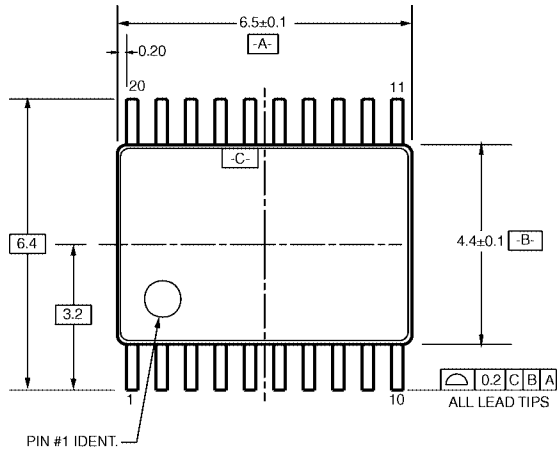C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
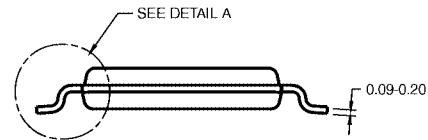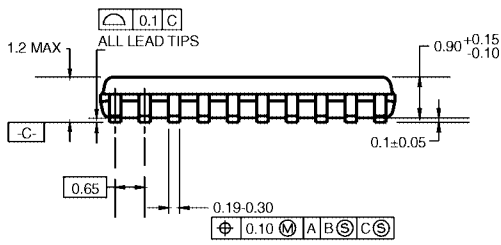

20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

6.5±0.1
-A-
0.20
20   11

-C-

6.4

4.4±0.1 -B-

3.2

1   10
⌒ 0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.

LAND PATTERN RECOMMENDATION

4.16   7.72

1.78

0.65   0.42

⌒ 0.1 C
ALL LEAD TIPS

1.2 MAX

0.90 +0.15 -0.10

-C-

0.1±0.05

0.65

0.19-0.30

⊕ 0.10 Ⓜ A B Ⓢ C Ⓢ

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.09-0.20

12.00°

R0.09 MIN   GAGE PLANE

0.25

0 - 8°

0.6 ±0.1

1.00   SEATING PLANE

R0.09 MIN
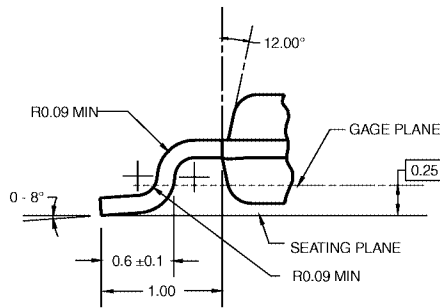
NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC,
   REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND
   TIE BAR EXTRUSIONS.
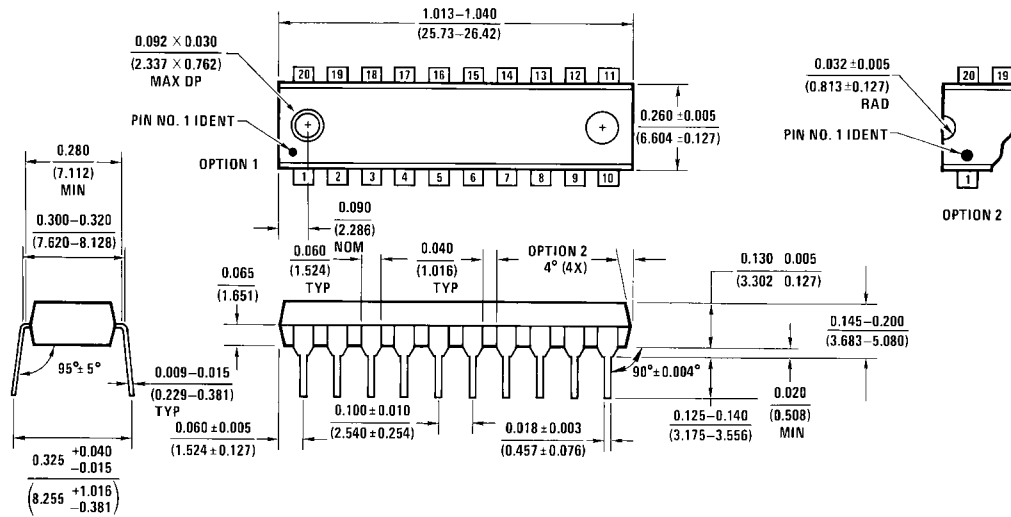D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

DETAIL A

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

1.013−1.040
(25.73−26.42)

0.092 × 0.030
(2.337 × 0.762)
MAX DP

PIN NO. 1 IDENT

OPTION 1

0.260 ±0.005
(6.604 −0.127)

0.032 ±0.005
(0.813 ±0.127)
RAD

PIN NO. 1 IDENT

OPTION 2

0.280
(7.112)
MIN

0.300−0.320
(7.620−8.128)

0.065
(1.651)

95°± 5°

0.009−0.015
(0.229−0.381)
TYP

0.060 ±0.005
(1.524 ±0.127)

0.325 +0.040 −0.015
(8.255 +1.016 −0.381)

0.090
(2.286)

0.060
(1.524)
TYP

NOM

0.040
(1.016)
TYP

OPTION 2
4° (4X)

0.130 0.005
(3.302 0.127)

0.145−0.200
(3.683−5.080)

90°±0.004°

0.020
(0.508)
MIN

0.100 ± 0.010
(2.540 ± 0.254)

0.018 ±0.003
(0.457 ±0.076)

0.125−0.140
(3.175−3.556)

N20A (REV G)

20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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