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# 74ABT574A

Octal D-type flip-flop; 3-state

Rev. 2 — 23 November 2012

Product data sheet

## 1. General description

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The 74ABT574A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT574A is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The clock input (CP) and output enable input ( $\overline{OE}$ ) control gates, control the two sections of the device independently. The state of each data input (Dn, one set-up time before the Low-to-High clock transition) is transferred to the Q output of the corresponding flip-flop.

When  $\overline{OE}$  is Low, the stored data appears at the outputs. When  $\overline{OE}$  is High, the outputs are in the High-impedance “off” state, which means they do not drive or load the bus.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ( $\overline{OE}$ ) controls all eight 3-State buffers independent of the clock operation.

## 2. Features and benefits

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- 74ABT574A is flow-through pinout version of 74ABT374A
- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State outputs for bus interfacing
- Power-on 3-state
- Power-on reset
- Common output enable
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Live insertion/extraction permitted.

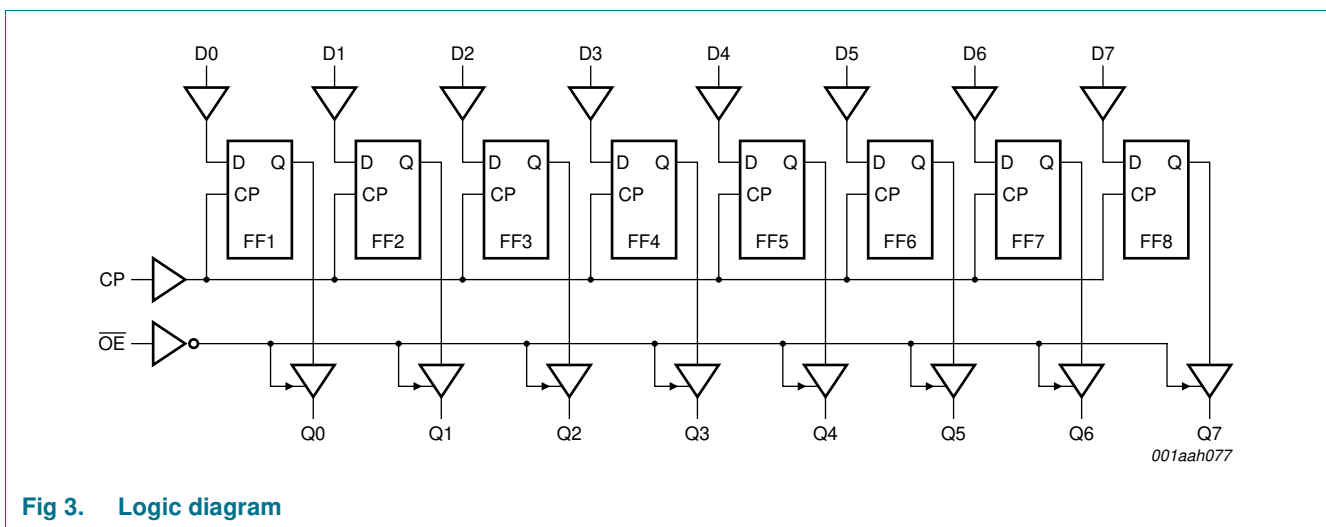
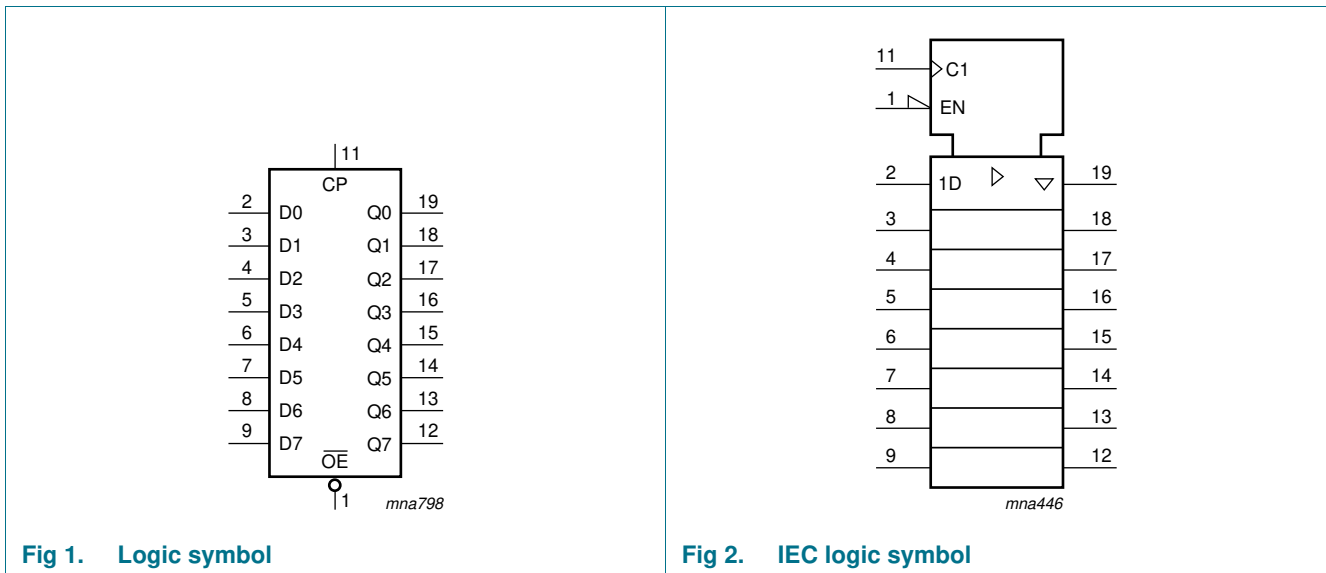


### 3. Ordering information

Table 1. Ordering information

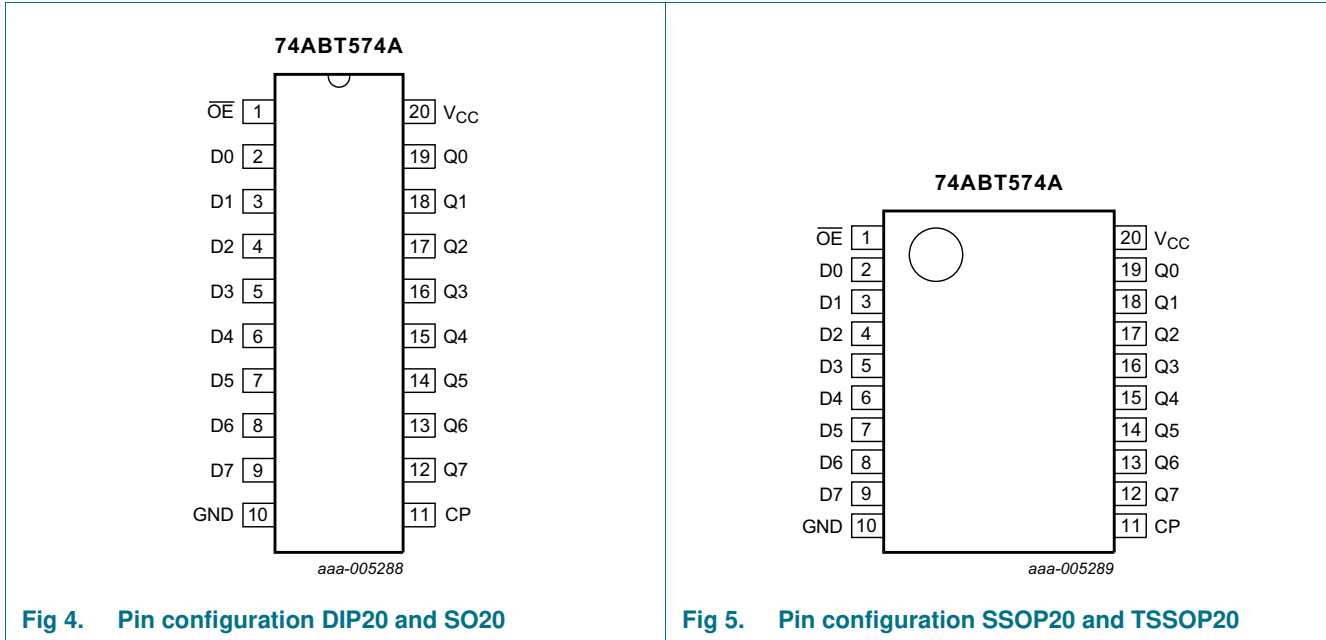
Type number	Package			Version
	Temperature range	Name	Description	
74ABT574AN	-40 °C to +85 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74ABT574AD	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ABT574ADB	-40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74ABT574APW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

### 4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	3-state output enable input (active LOW)
D0, D1, D2, D3, D4, D5, D6, D7	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
CP	11	clock pulse input (active rising edge)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	19, 18, 17, 16, 15, 14, 13, 12	3-state flip-flop output
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Operating mode	Input			Internal flip-flop	Output Qn
	$\overline{\text{OE}}$	CP	Dn		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable output	H	↑	l	L	Z
	H	↑	h	H	Z

- [1] H = HIGH voltage level;  
 h = HIGH voltage level one setup time before the HIGH-to-LOW CP transition;  
 L = LOW voltage level;  
 l = LOW voltage level one setup time before the HIGH-to-LOW CP transition;  
 Z = high-impedance OFF-state;  
 ↑ = LOW-to-HIGH clock transition.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		<sup>[1]</sup> -1.2	+7.0	V
$V_O$	output voltage	output in OFF-state or HIGH-state	<sup>[1]</sup> -0.5	+5.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-18	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$I_O$	output current	output in LOW-state	-	128	mA
$T_j$	junction temperature		<sup>[2]</sup> -	150	°C
$T_{stg}$	storage temperature		-65	+150	°C

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

## 8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		4.5	-	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$I_{OH}$	HIGH-level output current		-32	-	-	mA

**Table 5. Operating conditions ...continued**  
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OL}$	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	5	ns/V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C

## 9. Static characteristics

**Table 6. Static characteristics**

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit	
			Min	Typ	Max	Min	Max		
$V_{IK}$	input clamping voltage	$V_{CC} = 4.5\text{ V}; I_{IK} = -18\text{ mA}$	-1.2	-0.9	-	-1.2	-	V	
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IL}$ or $V_{IH}$							
		$V_{CC} = 4.5\text{ V}; I_{OH} = -3\text{ mA}$	2.5	2.9	-	2.5	-	V	
		$V_{CC} = 5.0\text{ V}; I_{OH} = -3\text{ mA}$	3.0	3.4	-	3.0	-	V	
		$V_{CC} = 4.5\text{ V}; I_{OH} = -32\text{ mA}$	2.0	2.4	-	2.0	-	V	
$V_{OL}$	LOW-level output voltage	$V_{CC} = 4.5\text{ V}; I_{OL} = 64\text{ mA};$ $V_I = V_{IL}$ or $V_{IH}$	-	0.42	0.55	-	0.55	V	
$V_{OL(pu)}$	power-up LOW-level output voltage	$V_{CC} = 5.5\text{ V}; I_O = 1\text{ mA};$ $V_I = \text{GND}$ or $V_{CC}$	[1]	-	0.13	0.55	-	0.55	V
$I_I$	input leakage current	$V_{CC} = 5.5\text{ V}; V_I = V_{CC}$ or GND	-	±0.01	±1.0	-	±1.0	µA	
$I_{OFF}$	power-off leakage current	$V_{CC} = 0\text{ V}; V_I$ or $V_O \leq 4.5\text{ V}$	-	±5.0	±100	-	±100	µA	
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} = 2.0\text{ V}; V_O = 0.5\text{ V};$ $V_I = \text{GND}$ or $V_{CC}; \overline{OE}$ HIGH	[2]	-	±5.0	±50	-	±50	µA
$I_{OZ}$	OFF-state output current	$V_{CC} = 5.5\text{ V}; V_I = V_{IL}$ or $V_{IH}$							
		$V_O = 2.7\text{ V}$	-	5.0	50	-	50	µA	
		$V_O = 0.5\text{ V}$	-50	-5.0	-	-50	-	µA	
$I_{LO}$	output leakage current	HIGH-state; $V_O = 5.5\text{ V};$ $V_{CC} = 5.5\text{ V}; V_I = \text{GND}$ or $V_{CC}$	-	5.0	50	-	50	µA	
$I_O$	output current	$V_{CC} = 5.5\text{ V}; V_O = 2.5\text{ V}$	[3]	-180	-40	-180	-40	mA	
$I_{CC}$	supply current	$V_{CC} = 5.5\text{ V}; V_I = \text{GND}$ or $V_{CC}$							
		outputs HIGH-state	-	100	250	-	250	µA	
		outputs LOW-state	-	24	30	-	30	mA	
		outputs disabled	-	100	250	-	250	µA	
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 5.5\text{ V};$ one input at 3.4 V; other inputs at $V_{CC}$ or GND	[4]	-	0.5	1.5	-	1.5	mA

**Table 6. Static characteristics ...continued**

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
C <sub>I</sub>	input capacitance	V <sub>I</sub> = 0 V or V <sub>CC</sub>	-	3	-	-	-	pF
C <sub>O</sub>	output capacitance	outputs disabled; V <sub>O</sub> = 0 V or V <sub>CC</sub>	-	6	-	-	-	pF

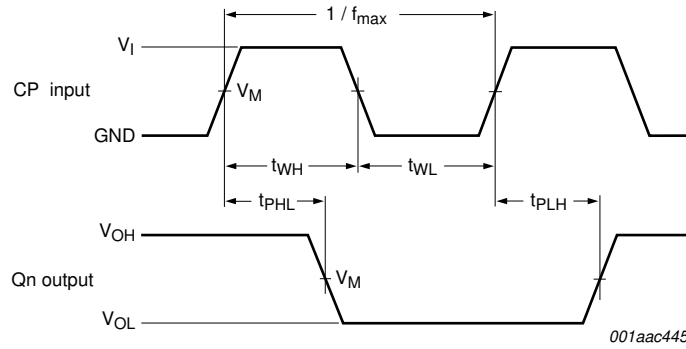
- [1] For valid test results, do not load data into the flip-flops (or latches) after applying the power.
- [2] This parameter is valid for any V<sub>CC</sub> between 0 V and 2.1 V, with a transition time of up to 10 ms. A transition time of up to 100 μs is permitted between V<sub>CC</sub> = 2.1 V and V<sub>CC</sub> = 5 V ± 10 %.
- [3] Do not test more than one output at a time, and the duration of the test must not exceed one second.
- [4] This characteristic is the increase in supply current for each input at 3.4 V.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**  
GND = 0 V; for test circuit, see [Figure 9](#).

Symbol	Parameter	Conditions	25 °C; V <sub>CC</sub> = 5.0 V			-40 °C to +85 °C; V <sub>CC</sub> = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
f <sub>max</sub>	maximum frequency	see <a href="#">Figure 6</a>	150	400	-	125	-	MHz
t <sub>PLH</sub>	LOW to HIGH propagation delay	CP to Qn, see <a href="#">Figure 6</a>	1.5	3.0	4.4	1.5	5.0	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	CP to Qn, see <a href="#">Figure 6</a>	2.0	3.4	4.7	2.0	5.1	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	$\overline{OE}$ to Qn; see <a href="#">Figure 8</a>	1.0	2.9	4.1	1.0	5.0	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	$\overline{OE}$ to Qn; see <a href="#">Figure 8</a>	2.5	3.8	5.2	2.5	5.7	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	$\overline{OE}$ to Qn; see <a href="#">Figure 8</a>	1.8	3.1	4.3	1.8	5.0	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	$\overline{OE}$ to Qn; see <a href="#">Figure 8</a>	1.4	2.6	3.8	1.4	4.0	ns
t <sub>su(H)</sub>	set-up time HIGH	Dn to CP; see <a href="#">Figure 7</a>	1.0	0.6	-	1.0	-	ns
t <sub>su(L)</sub>	set-up time LOW	Dn to CP; see <a href="#">Figure 7</a>	1.0	0.2	-	1.0	-	ns
t <sub>h(H)</sub>	hold time HIGH	CP to Dn; see <a href="#">Figure 7</a>	+1.0	-0.7	-	1.0	-	ns
t <sub>h(L)</sub>	hold time LOW	CP to Dn; see <a href="#">Figure 7</a>	+1.0	-0.4	-	1.0	-	ns
t <sub>WH</sub>	pulse width HIGH	CP; see <a href="#">Figure 6</a>	2.0	0.7	-	2.0	-	ns
t <sub>WL</sub>	pulse width LOW	CP; see <a href="#">Figure 6</a>	2.0	0.8	-	2.0	-	ns

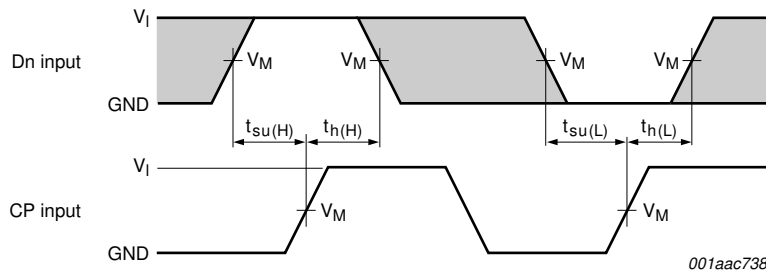
11. Waveforms



$V_M = 1.5\text{ V}$

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 6. Propagation delay clock input (CP) to output (Qn), clock pulse (CP) width and maximum clock (CP) frequency**

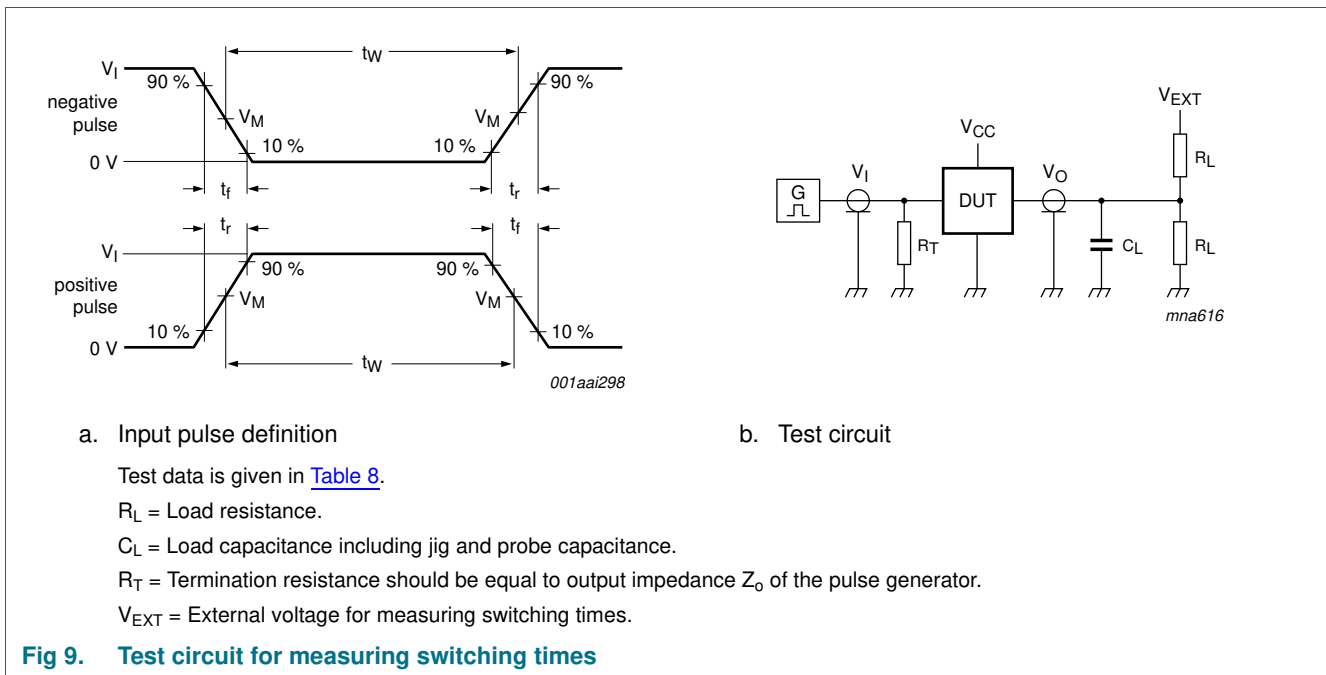
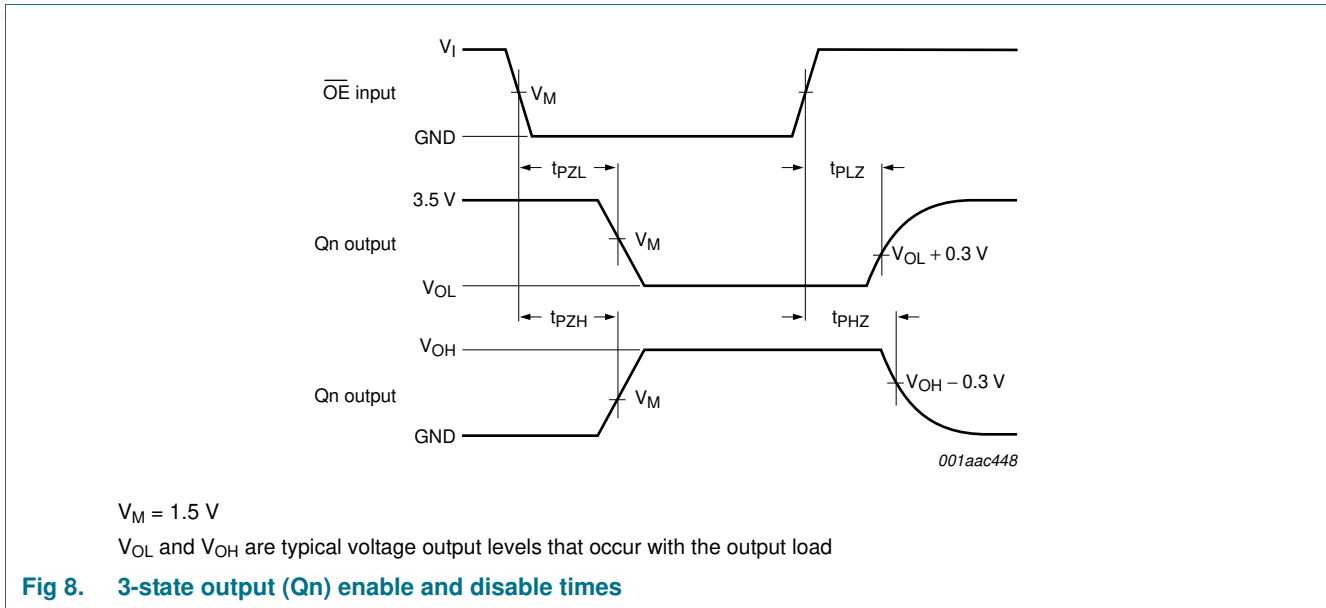


$V_M = 1.5\text{ V}$

The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 7. Set-up and hold times data output (Dn) to clock (CP)**





**Table 8. Test data**

Input				Load		$V_{EXT}$		
$V_I$	$f_i$	$t_w$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
3.0 V	1 MHz	500 ns	$\leq 2.5\text{ ns}$	50 pF	500 $\Omega$	open	open	7.0 V

12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

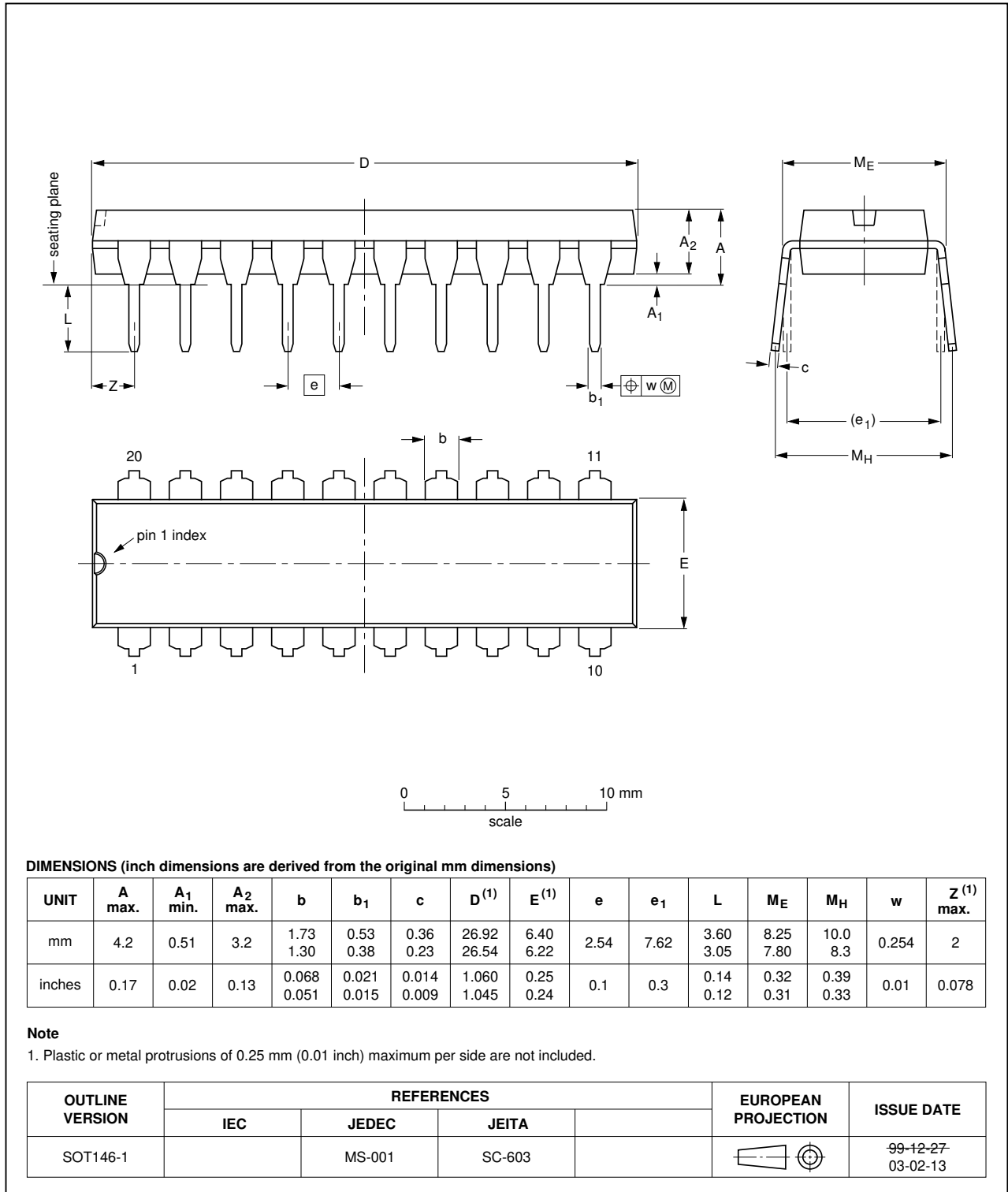


Fig 10. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

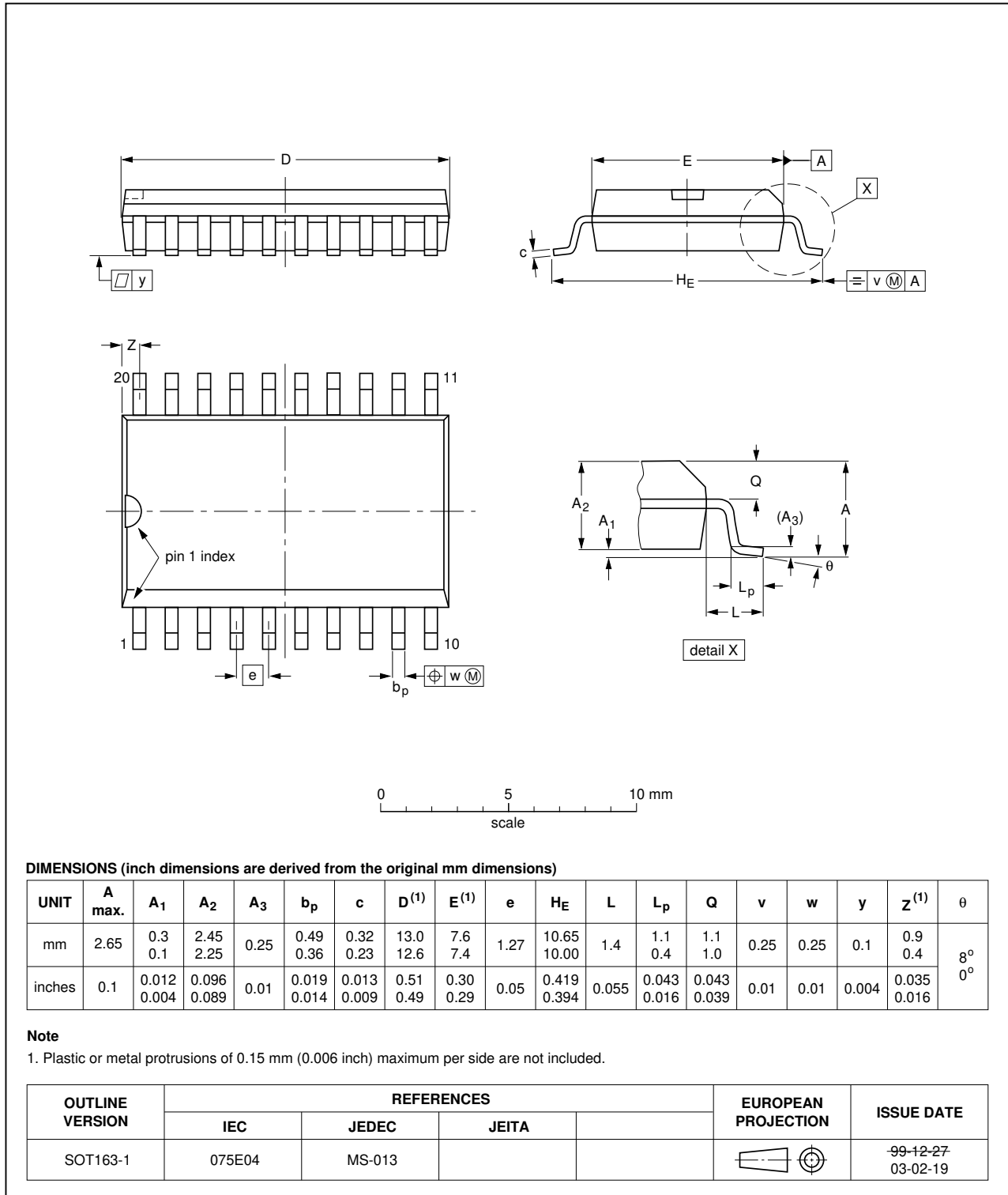


Fig 11. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

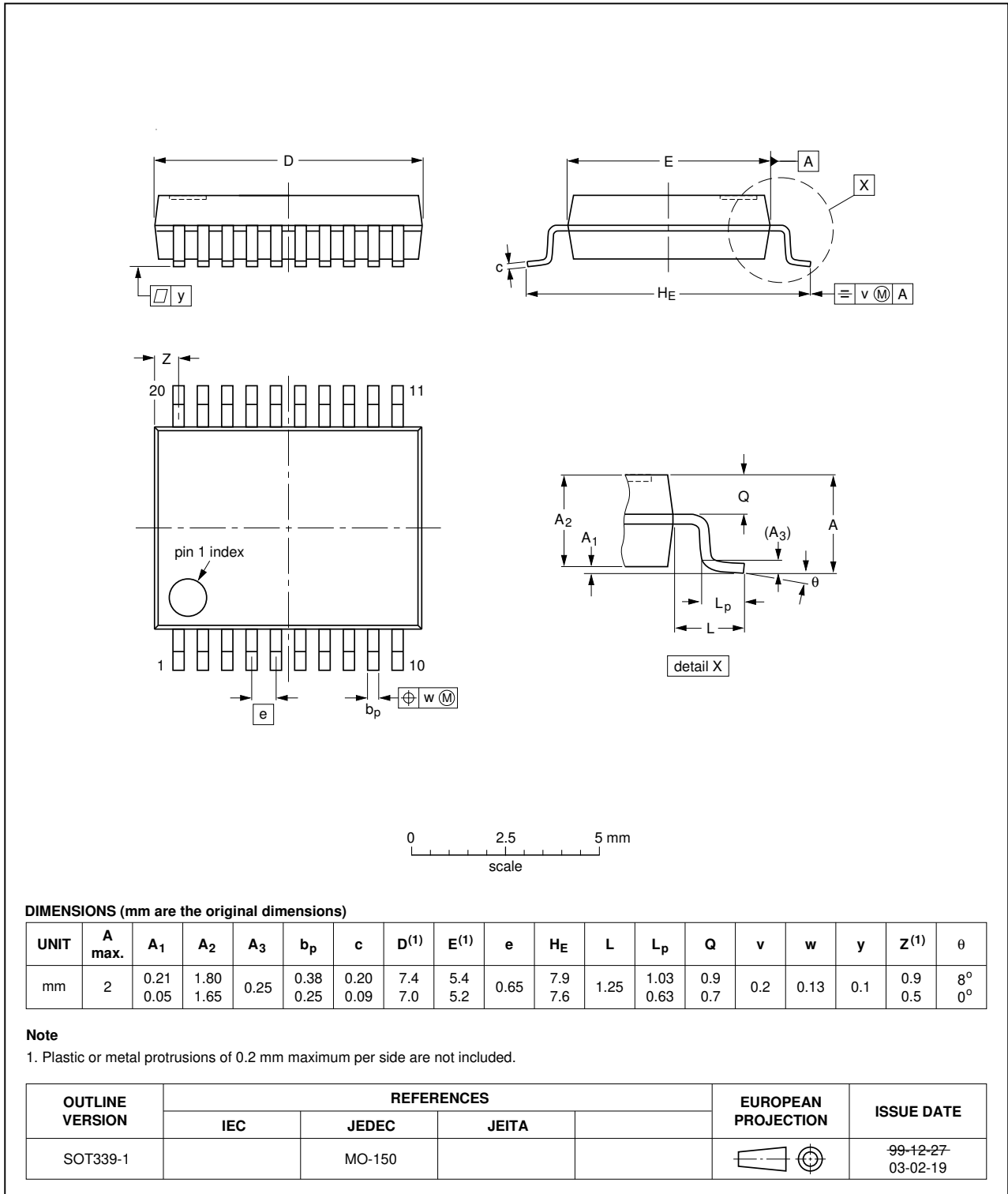


Fig 12. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

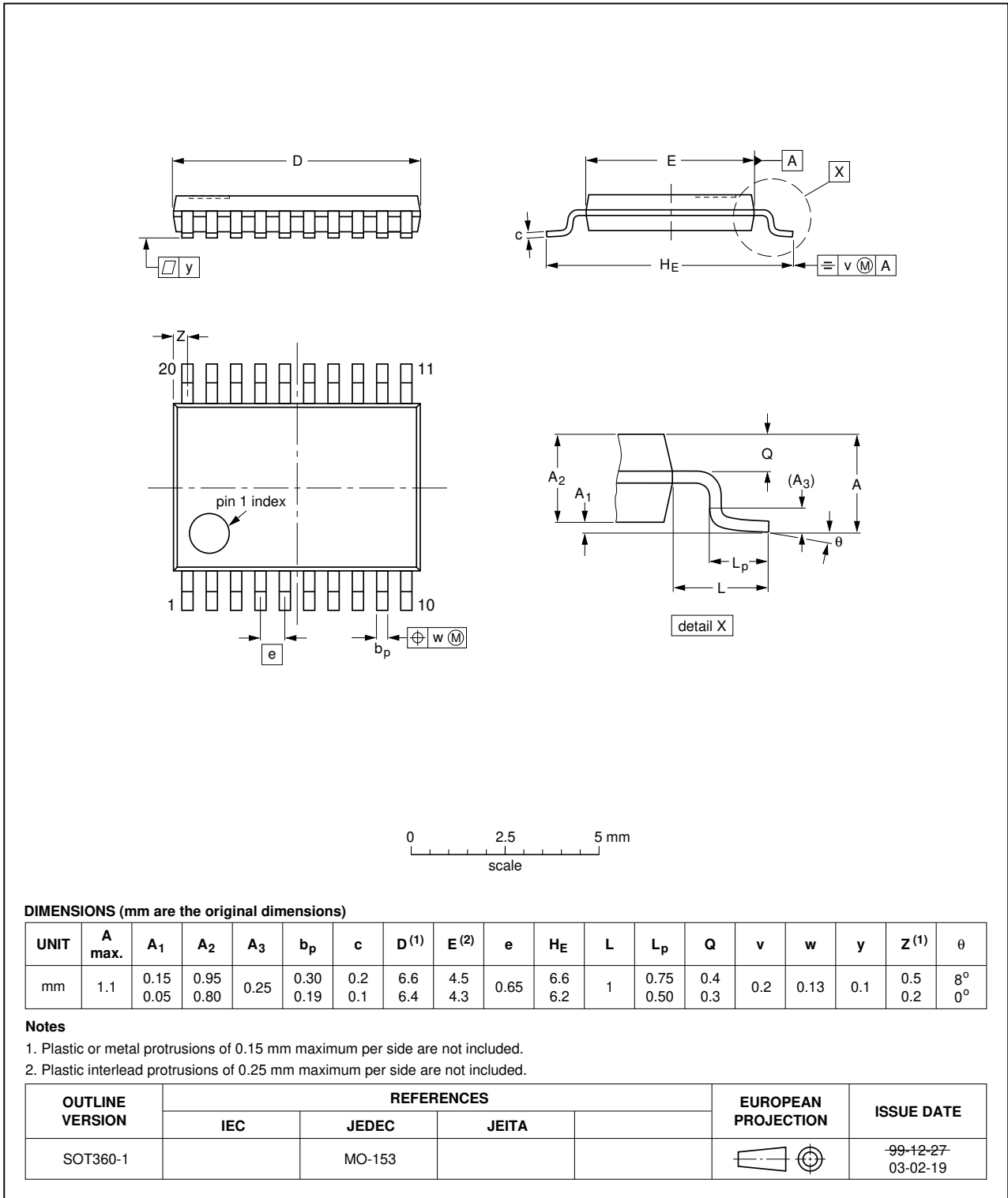


Fig 13. Package outline SOT360-1 (TSSOP20)

## 13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BICMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT574A v.2	20121123	Product data sheet	-	74ABT574A v.1
Modifications:		<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Legal texts have been adapted to the new company name where appropriate.</li></ul>		
74ABT574A v.1	19950522	Product specification	-	-

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### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 23 November 2012

Document identifier: 74ABT574A