

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

74AC10, 74ACT10 Triple 3-Input NAND Gate

Features

- I_{CC} reduced by 50% on 74AC only
- Outputs source/sink 24mA

General Description

The AC/ACT10 contains three, 3-input NAND gates.

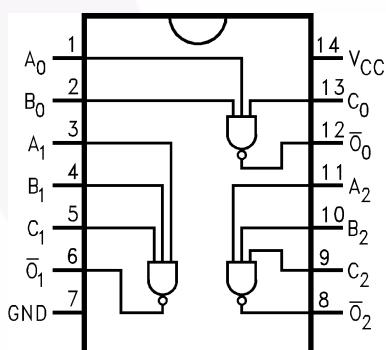
Ordering Information

Order Number	Package Number	Package Description
74AC10SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC10SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC10MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC10PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT10SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT10MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

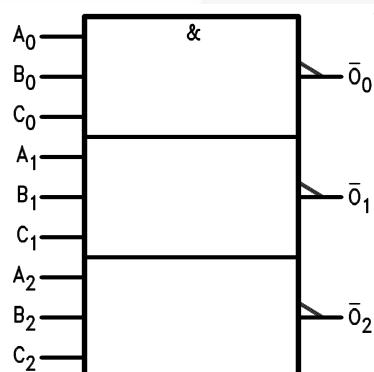
 All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Symbol

IEEE/IEC



Pin Description

Pin Names	Description
A_n, B_n, C_n	Inputs
\bar{O}_n	Outputs

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	-0.5V to +7.0V
I_{IK}	DC Input Diode Current $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$	-20mA +20mA
V_I	DC Input Voltage	-0.5V to $V_{CC} + 0.5V$
I_{OK}	DC Output Diode Current $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	-20mA +20mA
V_O	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
I_O	DC Output Source or Sink Current	$\pm 50mA$
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	$\pm 50mA$
T_{STG}	Storage Temperature	-65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage AC ACT	2.0V to 6.0V 4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	-40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC} , V_{CC} @ 3.3V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	125mV/ns

DC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C		Guaranteed Limits	Units
				Typ.	T _A = -40°C to +85°C		
V _{IH}	Minimum HIGH Level Input Voltage	3.0	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	2.1	2.1	V
		4.5		2.25	3.15	3.15	
		5.5		2.75	3.85	3.85	
V _{IL}	Maximum LOW Level Input Voltage	3.0	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	0.9	0.9	V
		4.5		2.25	1.35	1.35	
		5.5		2.75	1.65	1.65	
V _{OH}	Minimum HIGH Level Output Voltage	3.0	I _{OUT} = -50µA	2.99	2.9	2.9	V
		4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
		3.0	V _{IN} = V _{IL} or V _{IH} , I _{OH} = -12mA		2.56	2.46	
		4.5			3.86	3.76	
		5.5			4.86	4.76	
V _{OL}	Maximum LOW Level Output Voltage	3.0	I _{OUT} = 50µA	0.002	0.1	0.1	V
		4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
		3.0	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 12mA		0.36	0.44	
		4.5			0.36	0.44	
		5.5			0.36	0.44	
I _{IN} ⁽³⁾	Maximum Input Leakage Current	5.5	V _I = V _{CC} or GND		±0.1	±1.0	µA
I _{OLD}	Minimum Dynamic Output Current ⁽²⁾	5.5	V _{OLD} = 1.65V Max.			75	mA
I _{OHD}		5.5	V _{OHD} = 3.85V Min.			-75	mA
I _{CC} ⁽³⁾	Maximum Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND		2.0	20.0	µA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C		T _A = -40°C to +85°C		Units	
				Typ.	Guaranteed Limits				
V _{IH}	Minimum HIGH Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	2.0	2.0		V	
		5.5		1.5	2.0	2.0			
V _{IL}	Maximum LOW Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	0.8	0.8		V	
		5.5		1.5	0.8	0.8			
V _{OH}	Minimum HIGH Level Output Voltage	4.5	I _{OUT} = -50µA	4.49	4.4	4.4		V	
		5.5		5.49	5.4	5.4			
		4.5	V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA		3.86	3.76			
		5.5			4.86	4.76			
V _{OL}	Maximum LOW Level Output Voltage	4.5	I _{OUT} = 50µA	0.001	0.1	0.1		V	
		5.5		0.001	0.1	0.1			
		4.5	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA		0.36	0.44			
		5.5			0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5	V _I = V _{CC} , GND		±0.1	±1.0		µA	
I _{CCT}	Maximum I _{CC} /Input	5.5	V _I = V _{CC} - 2.1V	0.6		1.5		mA	
I _{OLD}	Minimum Dynamic Output Current ⁽⁵⁾	5.5	V _{OLD} = 1.65V Max.			75		mA	
I _{OHD}		5.5	V _{OHD} = 3.85V Min.			-75		mA	
I _{CC}	Maximum Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND		4.0	40.0		µA	

Notes:

4. All outputs loaded; thresholds on input associated with output under test.
5. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} (V) ⁽⁶⁾	T _A = +25°C, C _L = 50pF			T _A = -40°C to +85°C, C _L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t _{PLH}	Propagation Delay	3.3	1.5	6.0	9.5	1.0	10.5	ns
		5.0	1.5	4.5	7.0	1.0	8.0	
t _{PHL}	Propagation Delay	3.3	1.5	5.5	8.5	1.0	10.0	ns
		5.0	1.5	4.0	6.0	1.0	6.5	

Note:

6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V) ⁽⁷⁾	T _A = +25°C, C _L = 50pF			T _A = -40°C to +85°C, C _L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t _{PLH}	Propagation Delay	5.0	1.0	6.5	9.0	1.0	10.0	ns
t _{PHL}	Propagation Delay	5.0	1.0	6.5	9.0	1.0	9.5	ns

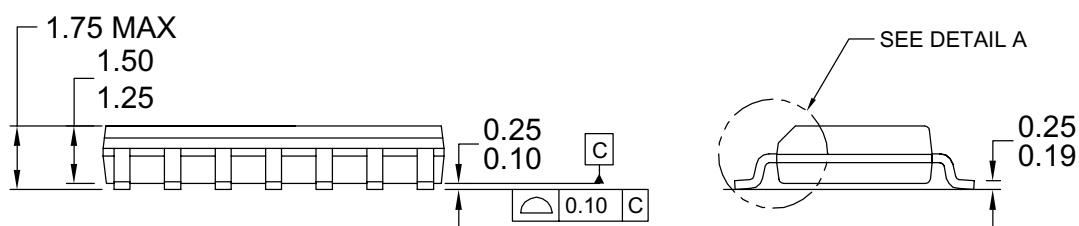
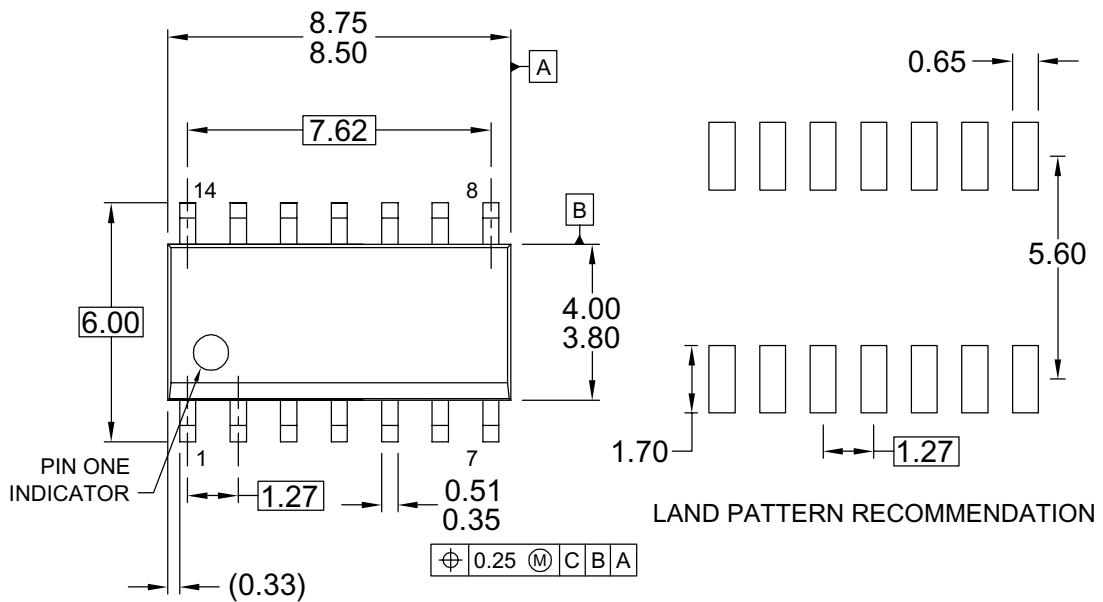
Note:

7. Voltage Range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C _{IN}	Input Capacitance	V _{CC} = OPEN	4.5	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 5.0V	25.0	pF

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
 - D) LANDPATTERN STANDARD:
SOIC127P600X145-14M
 - E) DRAWING CONFORMS TO ASME Y14.5M-1994
 - F) DRAWING FILE NAME: M14AREV13

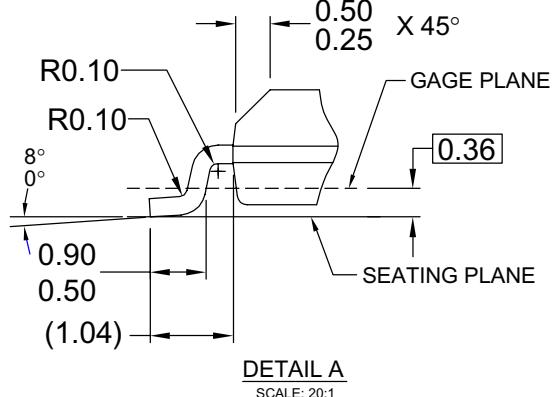


Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

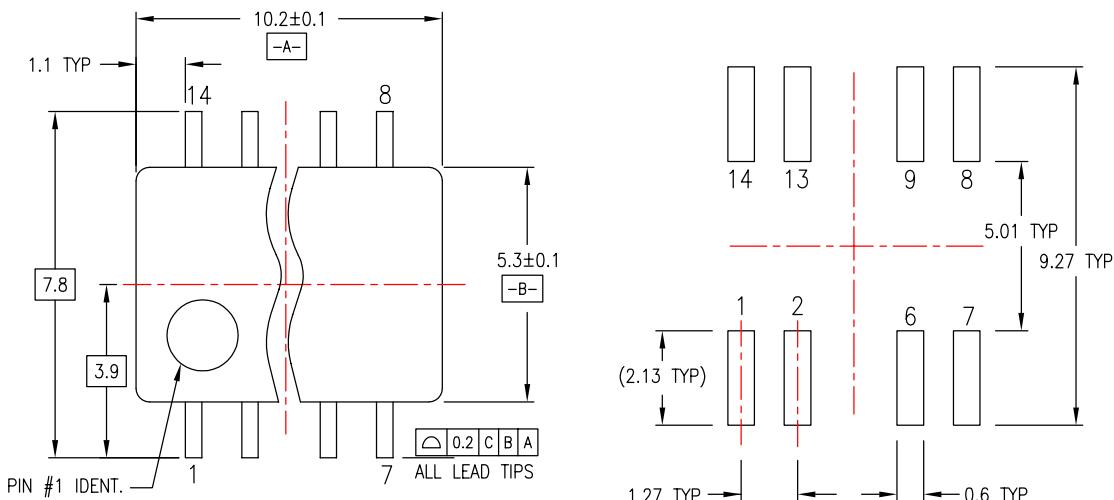
Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

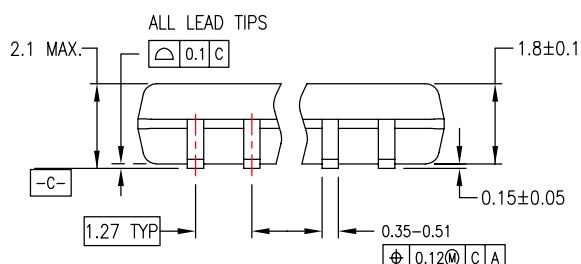
<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



LAND PATTERN RECOMMENDATION

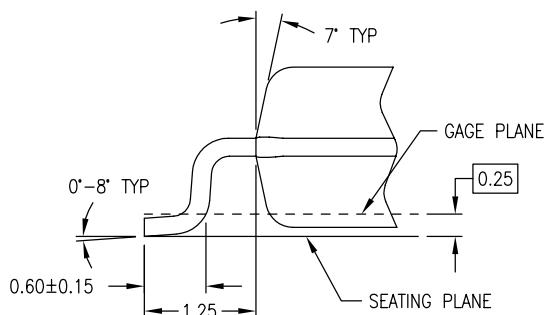
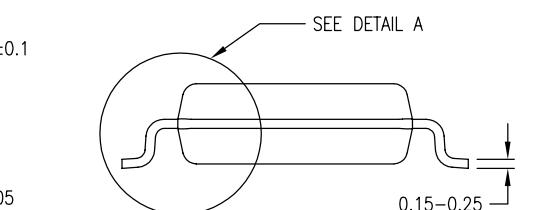


DIMENSIONS ARE IN MILLIMETERS

NOTES:

- NOTES:

 - A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



DETAIL A

M14DREV0

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)

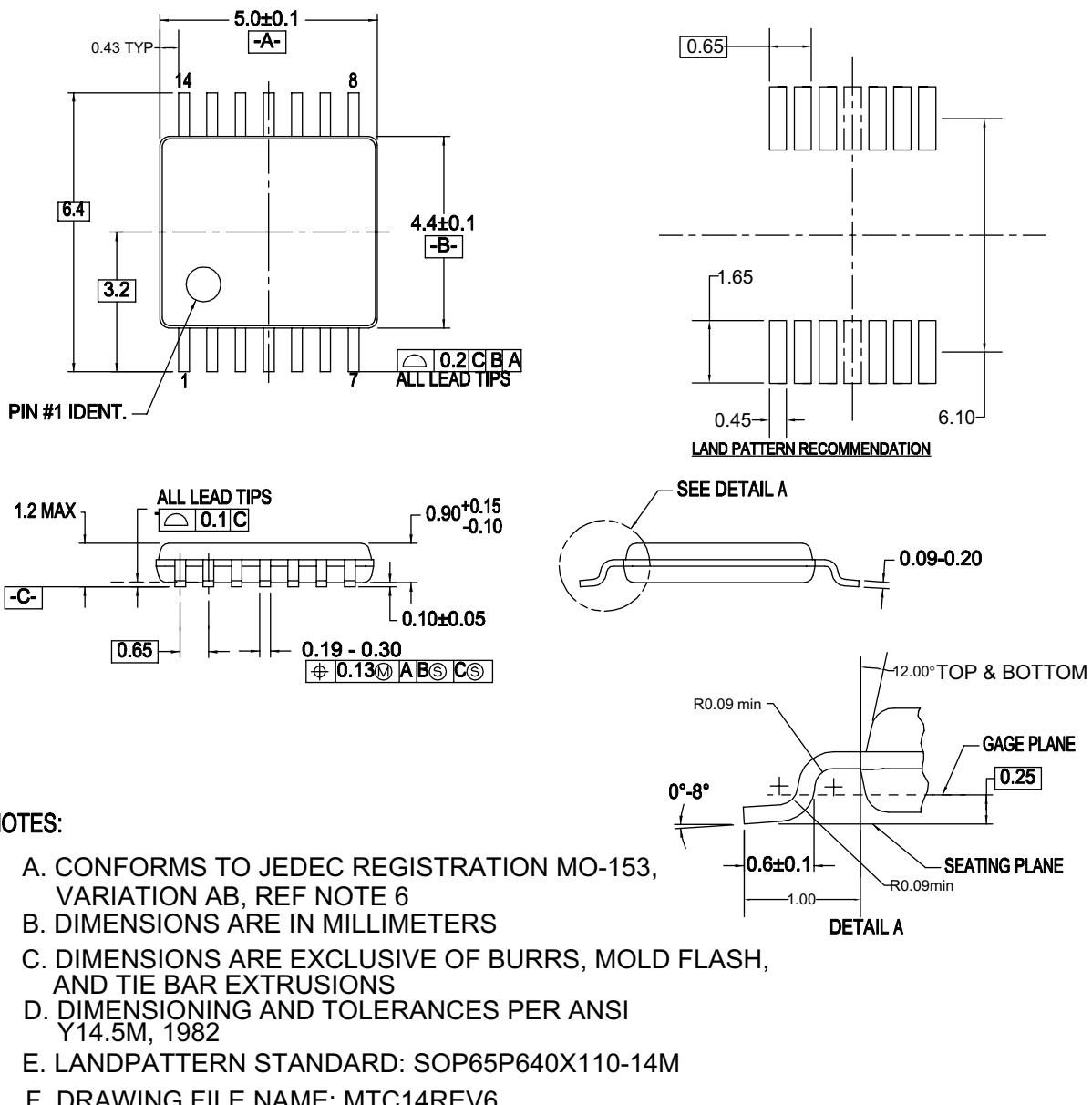


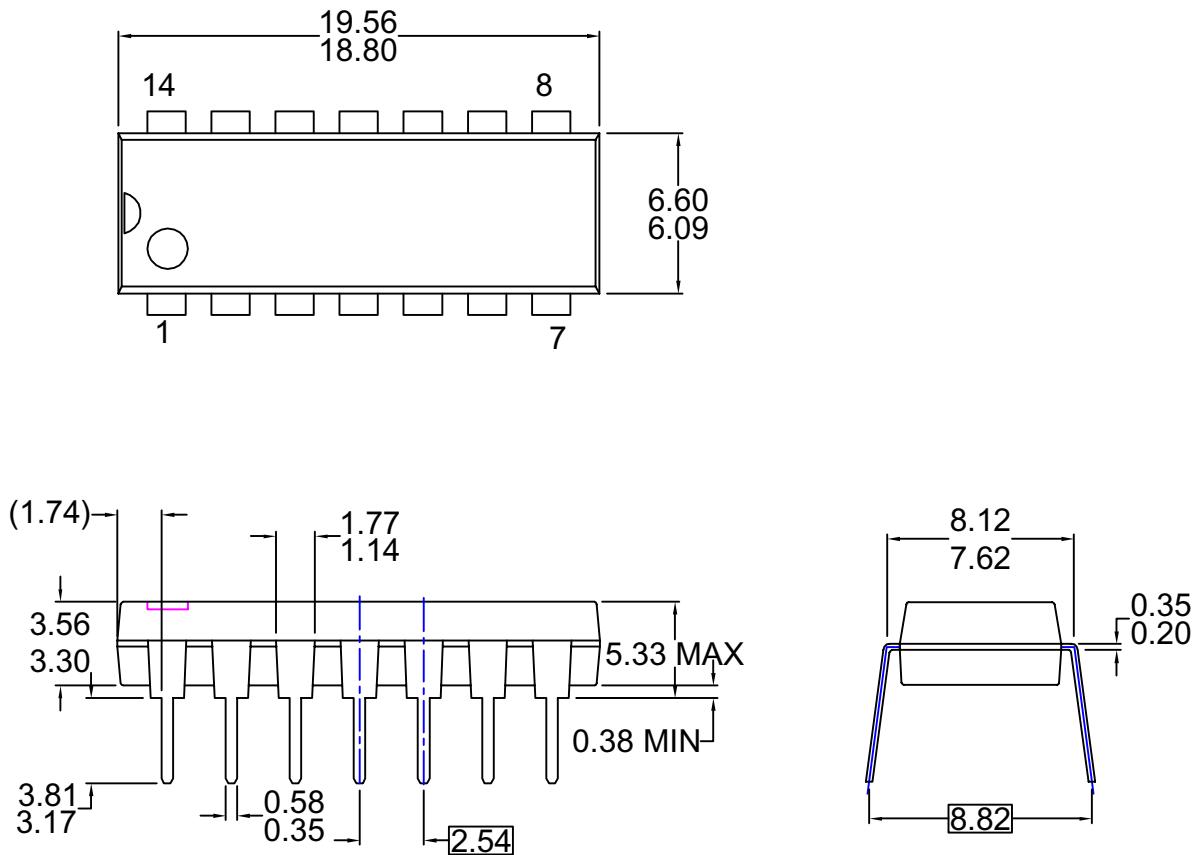
Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)



NOTES: UNLESS OTHERWISE SPECIFIED
 THIS PACKAGE CONFORMS TO
 A) JEDEC MS-001 VARIATION BA
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 DIMENSIONS ARE EXCLUSIVE OF BURRS,
 C) MOLD FLASH, AND TIE BAR EXTRUSIONS.
 D) DIMENSIONS AND TOLERANCES PER
 ASME Y14.5-1994
 E) DRAWING FILE NAME: MKT-N14AREV7

Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

ACE [®]	FPS [™]	PDP-SPM [™]	SyncFET [™]
Build it Now [™]	FRFET [®]	Power220 [®]	SYSTEM [®]
CorePLUS [™]	Global Power Resource SM	Power247 [®]	GENERAL
CROSSVOLT [™]	Green FPS [™]	POWEREDGE [®]	The Power Franchise [®]
CTL [™]	Green FPS [™] e-Series [™]	Power-SPM [™]	the power [®] franchise
Current Transfer Logic [™]	GTO [™]	PowerTrench [®]	TinyBoost [™]
EcoSPARK [®]	i-Lo [™]	Programmable Active Droop [™]	TinyBuck [™]
EZSWITCH [™] *	IntelliMAX [™]	QFET [®]	TinyLogic [®]
	ISOPLANAR [™]	QS [™]	TINYOPTO [™]
	MegaBuck [™]	QT Optoelectronics [™]	TinyPower [™]
Fairchild [®]	MICROCOUPLER [™]	Quiet Series [™]	TinyPWM [™]
Fairchild Semiconductor [®]	MicroFET [™]	RapidConfigure [™]	TinyWire [™]
FACT Quiet Series [™]	MicroPak [™]	SMART START [™]	SerDes [™]
FACT [®]	MillerDrive [™]	SPM [®]	UHC [®]
FAST [®]	Motion-SPM [™]	STEALTH [™]	Ultra FRFET [™]
FastvCore [™]	OPTOLOGIC [®]	SuperFET [™]	UniFET [™]
FlashWriter [®] *	OPTOPLANAR [®]	SuperSOT [™] -3	VCX [™]
		SuperSOT [™] -6	
		SuperSOT [™] -8	

* EZSWITCH[™] and FlashWriter[®] are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I32