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74AC16373

16-BIT D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS (NON INVERTED)

- HIGH SPEED:
  t_{PD} = 5.0 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION:
  I_{CC} = 8µA(MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- 50Ω TRASMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 24mA (MIN)
- OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 6V
- IMPROVED LATCH-UP IMMUNITY

TSSOP

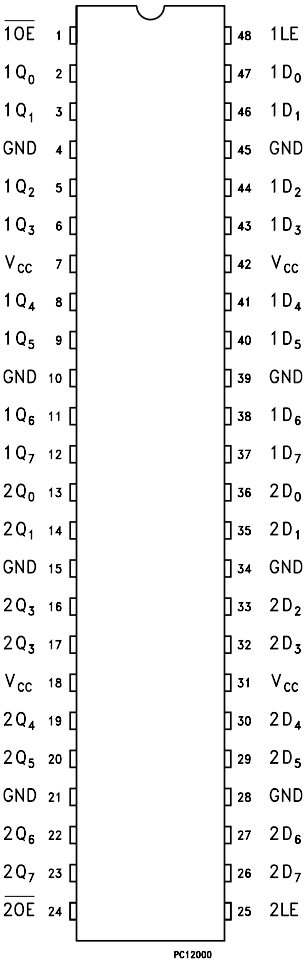
ORDER CODES

PACKAGE	TUBE	T & R
TSSOP		74AC16373TTR

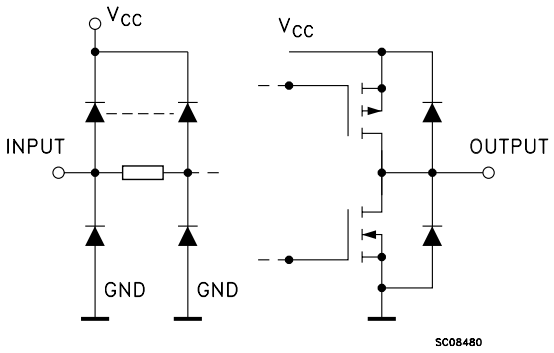
DESCRIPTION

The 74AC16373 CMOS 16 BIT D-TYPE LATCH with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology.
These 16 bit D-TYPE latches are byte controlled by two latch enable inputs (nLE) and two output enable inputs($n\overline{OE}$).
While the nLE input is held at a high level, the nQ outputs will follow the data (D) inputs.
When the nLE is taken LOW, the nQ outputs will be latched at the logic level of D data inputs.
When the ($n\overline{OE}$) input is low, the nQ outputs will be in a normal logic state (high or low logic level); when $n\overline{OE}$ is at high level ,the outputs will be in a high impedance state.
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

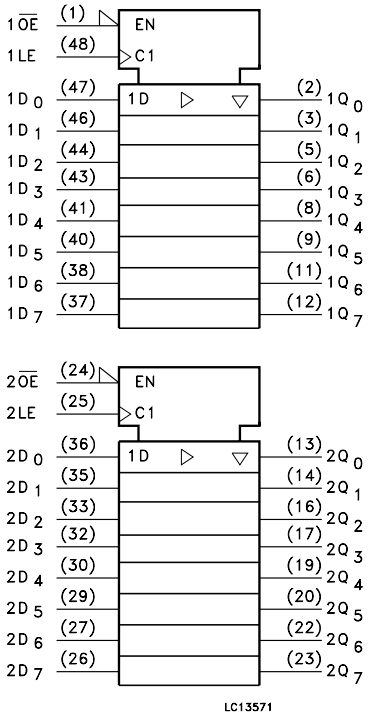
PIN No	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	3 State Output Enable Input (Active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3-State Outputs
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3-State Outputs
24	$2\overline{OE}$	3 State Output Enable Input (Active LOW)
25	2LE	Latch Enable Input
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data Inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data Inputs
48	1LE	Latch Enable Input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive Supply Voltage

TRUTH TABLE

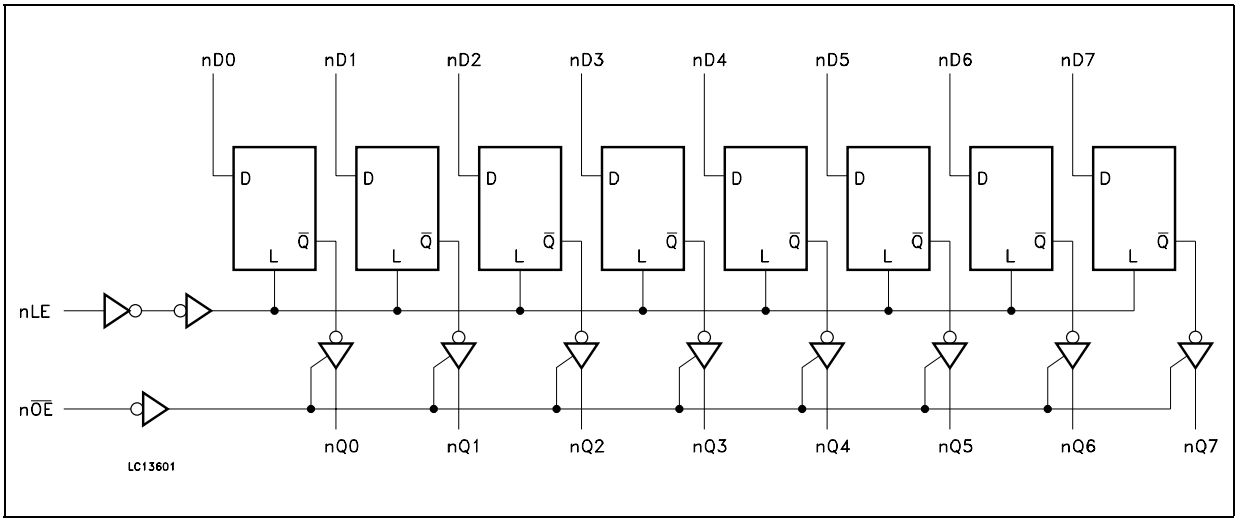
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE *
L	H	L	L
L	H	H	H

X : Don't Care
Z : High Impedance
* : Q outputs are latched at the time when the LE input is taken low logic level.

IEC LOGIC SYMBOLS



LOGIC DIAGRAM



This logic diagram has not to be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 400	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time V_{CC} = 3.0, 4.5 or 5.5V (note 1)	8	ns/V

1) V_{IN} from 30% to 70% of V_{CC}

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	3.0	V_O = 0.1 V or V_{CC}-0.1V	2.1	1.5		2.1		2.1		V
		4.5		3.15	2.25		3.15		3.15		
		5.5		3.85	2.75		3.85		3.85		
V_{IL}	Low Level Input Voltage	3.0	V_O = 0.1 V or V_{CC}-0.1V		1.5	0.9		0.9		0.9	V
		4.5			2.25	1.35		1.35		1.35	
		5.5			2.75	1.65		1.65		1.65	
V_{OH}	High Level Output Voltage	3.0	I_O=-50 µA	2.9	2.99		2.9		2.9		V
		4.5	I_O=-50 µA	4.4	4.49		4.4		4.4		
		5.5	I_O=-50 µA	5.4	5.49		5.4		5.4		
		3.0	I_O=-12 mA	2.56			2.46		2.46		
		4.5	I_O=-24 mA	3.86			3.76		3.76		
		5.5	I_O=-24 mA	4.86			4.76		4.76		
V_{OL}	Low Level Output Voltage	3.0	I_O=50 µA		0.002	0.1		0.1		0.1	V
		4.5	I_O=50 µA		0.001	0.1		0.1		0.1	
		5.5	I_O=50 µA		0.001	0.1		0.1		0.1	
		3.0	I_O=12 mA			0.36		0.44		0.44	
		4.5	I_O=24 mA			0.36		0.44		0.44	
		5.5	I_O=24 mA			0.36		0.44		0.44	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{OZ}	High Impedance Output Leakage Current	5.5	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND			± 0.5		± 5		± 5	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND			8		80		80	µA
I_{OLD}	Dynamic Output Current (note 1, 2)	5.5	V_{OLD} = 1.65 V max					75		75	mA
I_{OHD}			V_{OHD} = 3.85 V min					-75		-75	mA

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50Ω

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, Input $t_r = t_f$ = 3ns)

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time LE to Q	3.3(*)			8.0	10.0		15.6		15.6	ns
		5.0(**)			6.0	8.0		11.9		11.9	
t_{PLH} t_{PHL}	Propagation Delay Time D to Q	3.3(*)			8.3	11.0		15.1		15.1	ns
		5.0(**)			6.0	9.1		10.1		10.1	
t_{PZL} t_{PZH}	Output Enable Time	3.3(*)			11.8	19.8		22.3		22.3	ns
		5.0(**)			7.4	11.3		12.8		12.8	
t_{PLZ} t_{PHZ}	Output Disable Time	3.3(*)			7.1	9.5		10.2		10.2	ns
		5.0(**)			5.9	8.0		8.8		8.8	
t_W	LE Pulse Width HIGH	3.3(*)		4.0			4.0		4.0		ns
		5.0(**)		5.0			5.0		5.0		
t_s	Setup Time D to LE, HIGH or LOW	3.3(*)		1.5			1.5		1.5		ns
		5.0(**)		1.5			1.5		1.5		
t_h	Hold Time D to LE, HIGH or LOW	3.3(*)		3			3		3		ns
		5.0(**)		2.5			2.5		2.5		

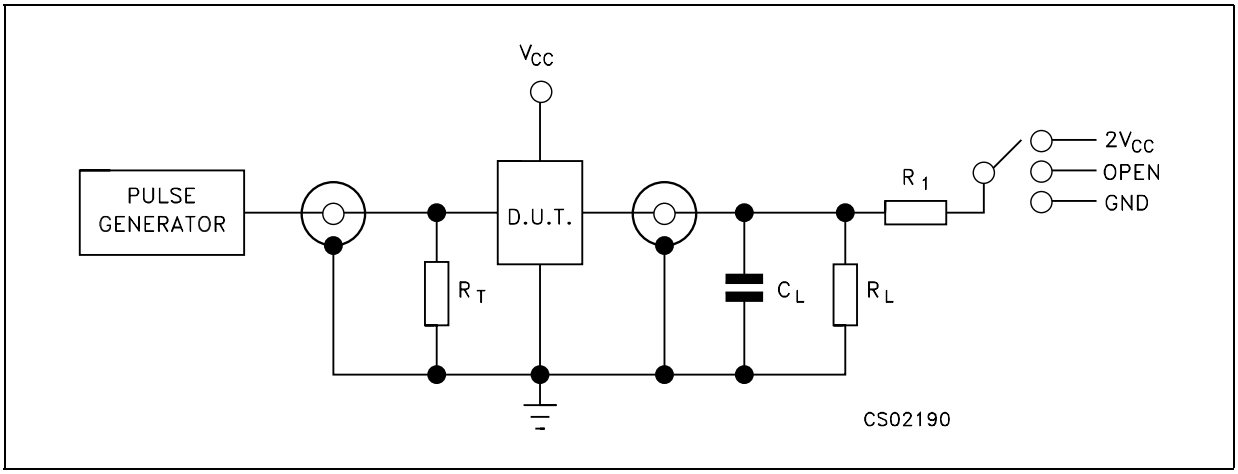
(*) Voltage range is 3.3V ± 0.3V
(**) Voltage range is 5.0V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	5.0			3.5						pF
C_{OUT}	Output Capacitance	5.0			15						pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0	f_{IN}=10MHz		25						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$ (per circuit)

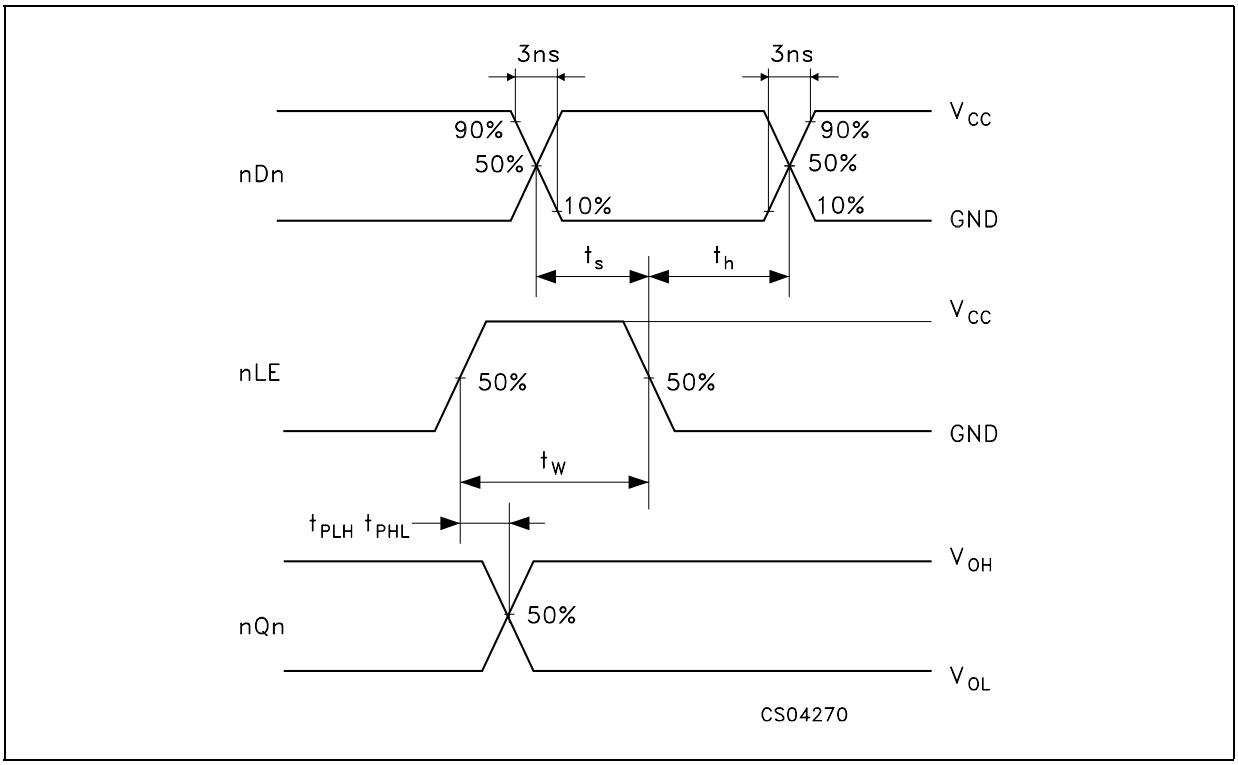
TEST CIRCUIT



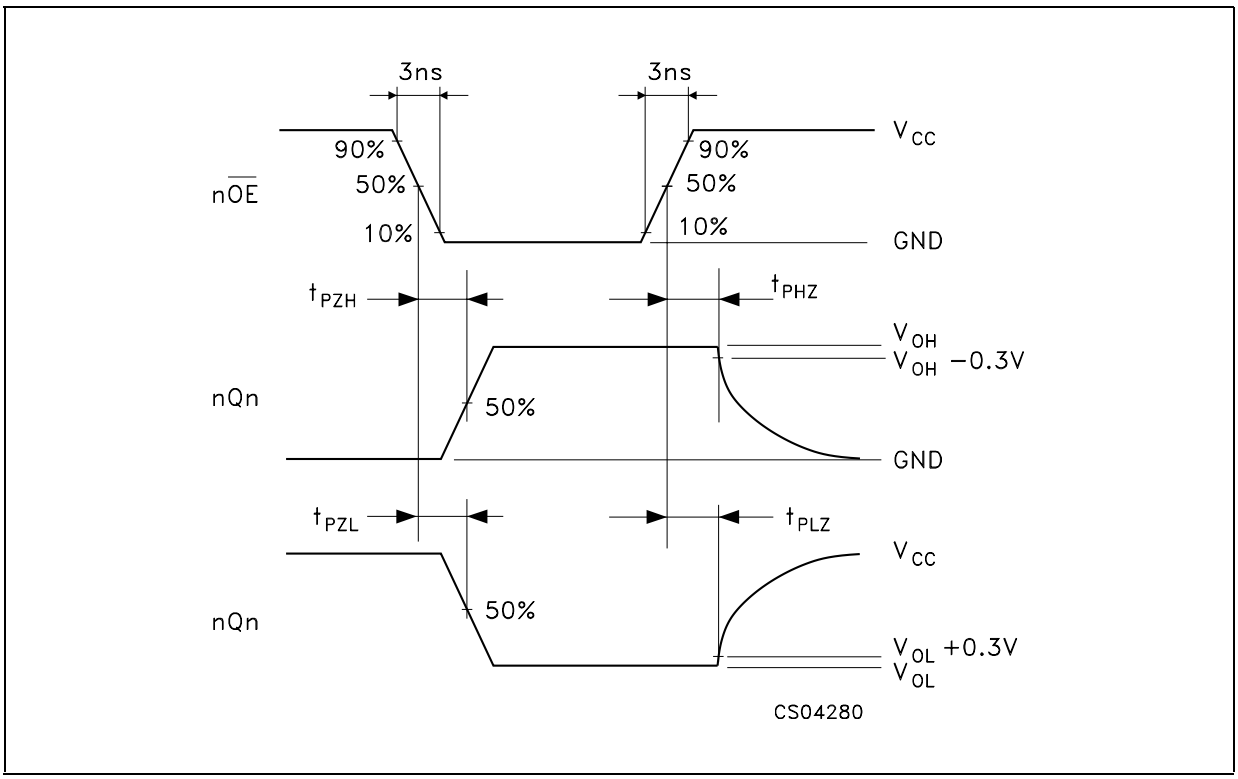
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	$2V_{CC}$
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

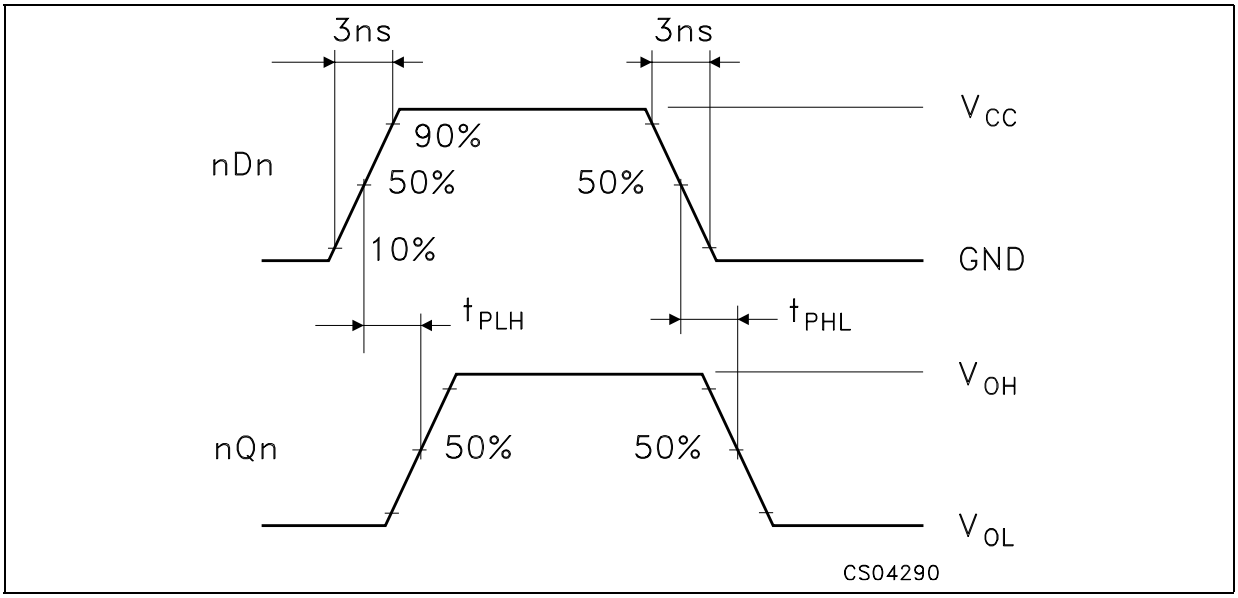
WAVEFORM 1 : LE TO Qn PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn TO LE SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)

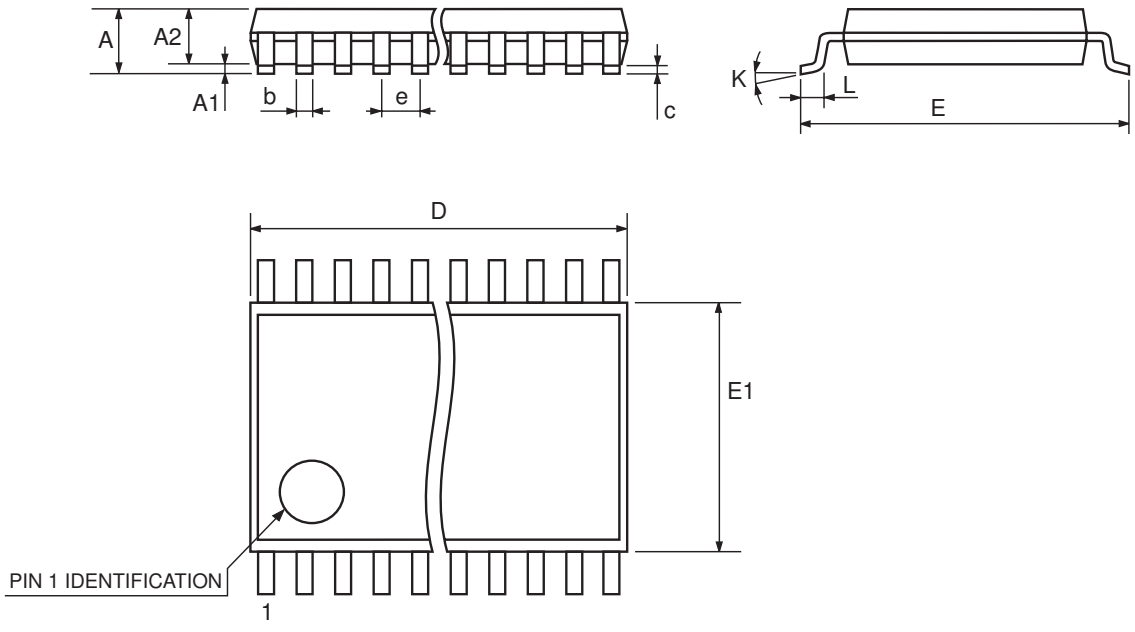


WAVEFORM 3 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



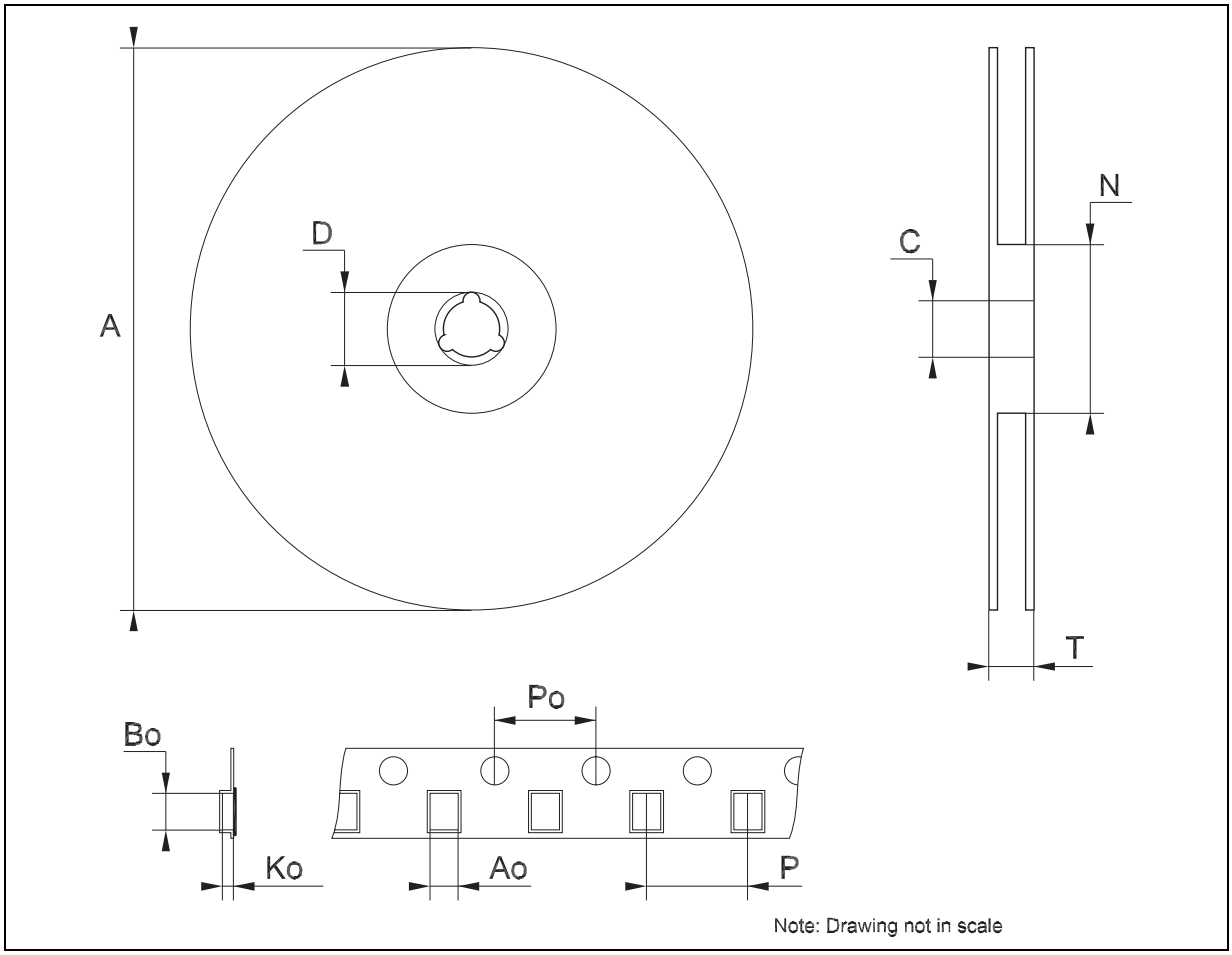
TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.488		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0˚		8˚	0˚		8˚
L	0.50		0.75	0.020		0.030



Tape & Reel TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.343		0.350
Bo	13.1		13.3	0.516		0.524
Ko	1.5		1.7	0.059		0.067
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Note: Drawing not in scale