Chipsmall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

FAIRCHILD

SEMICONDUCTOR®

74ACT16373
16-Bit Transparent Latch with 3-STATE Outputs

General Description

The ACT16373 contains sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state.

Features

■ Separate control logic for each byte
■ 16-bit version of the ACT373
■ Outputs source/sink 24 mA
■ TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74ACT16373SSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACT16373MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol
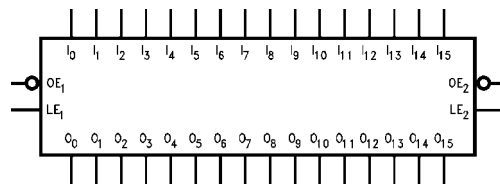
Connection Diagram
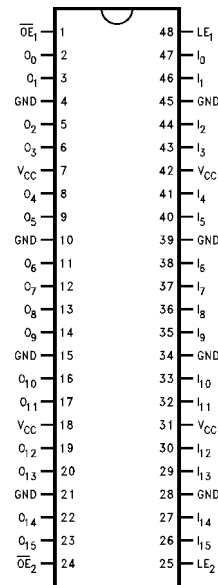
Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
LE_n	Latch Enable Input
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

FACT™ is a trademark of Fairchild Semiconductor Corporation.

www.fairchildsemi.com

Functional Description

The ACT16373 contains sixteen D-type latches with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e., a latch output will change states each time its D input changes. When LE_n is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE_n. The 3-STATE standard outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.
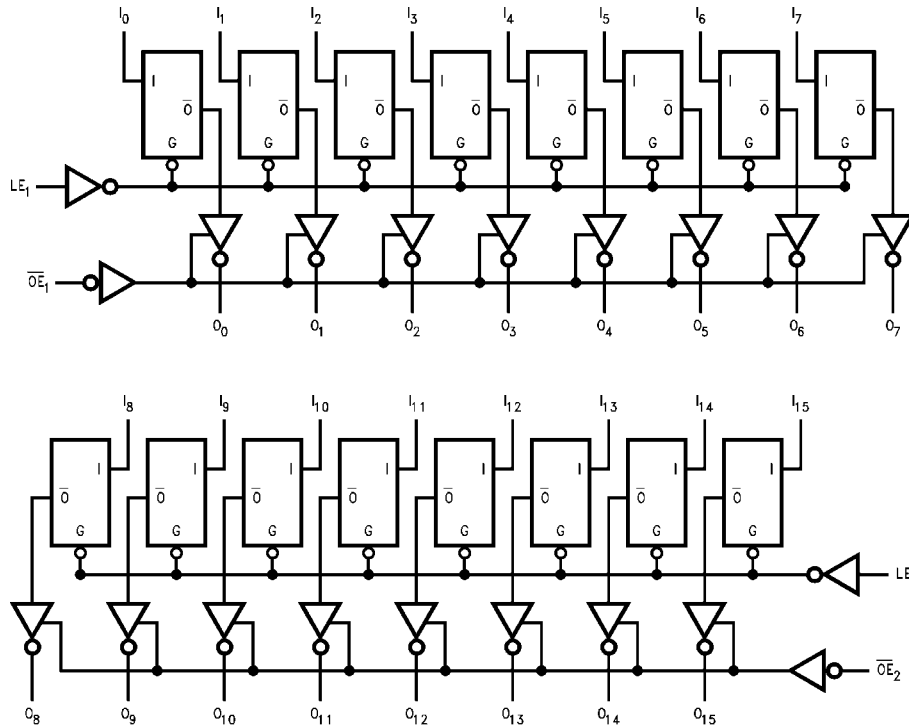
Truth Tables

Inputs			Outputs
LE_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	(Previous)

Inputs			Outputs
LE_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	(Previous)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
Previous = previous output prior to HIGH-to-LOW transition of LE

Logic Diagrams

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	+50 mA
DC V_{CC} or Ground Current	+50 mA
per Output Pin	
Junction Temperature	+140°C
Storage Temperature	−65°C to+150°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = +25°C$ Guaranteed Limits	$T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum HIGH	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$
	Input Voltage	5.5	1.5	2.0	2.0		or $V_{CC} - 0.1V$
V_{IL}	Maximum LOW	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$
	Input Voltage	5.5	1.5	0.8	0.8		or $V_{CC} - 0.1V$
V_{OH}	Minimum HIGH	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$
	Output Voltage	5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24$ mA
		5.5		4.86	4.76		$I_{OH} = -24$ mA (Note 2)
V_{OL}	Maximum LOW	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$
	Output Voltage	5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24$ mA
		5.5		0.36	0.44		$I_{OL} = 24$ mA (Note 2)
I_{OZ}	Maximum 3-STATE Leakage Current	5.5		± 0.5	± 5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{CC}	Max Quiescent Supply Current	5.5		8.0	80.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}	Output Current (Note 3)				−75	mA	$V_{OHD} = 3.85V$ Min

Note 2: All outputs loaded; thresholds associated with output under test.

Note 3: Maximum test duration 2.0 ms; one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 4)	$T_A = +25°C$ $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	5.0	3.1	5.3	7.9	3.1	8.4	ns
t_{PHL}	D_n to O_n		2.6	4.6	7.3	2.6	7.8	
t_{PLH}	Propagation Delay	5.0	3.1	5.4	7.9	3.2	8.4	ns
t_{PHL}	LE to O_n		2.8	4.9	7.3	2.8	7.8	
t_{PZH}	Output Enable	5.0	2.5	4.7	7.4	2.5	7.9	ns
t_{PZL}	Delay		2.7	4.8	7.5	2.7	8.0	
t_{PHZ}	Output Disable	5.0	2.1	5.1	7.9	2.1	8.2	ns
t_{PLZ}	Delay		2.0	4.5	7.4	2.0	7.9	

Note 4: Voltage Range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 5)	$T_A = +25°C$ $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units
			Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW, Input to Clock	5.0	3.0	3.0	ns
t_H	Hold time, HIGH or LOW, Input to Clock	5.0	1.5	1.5	ns
t_W	CS Pulse Width, HIGH or LOW	5.0	4.0	4.0	ns

Note 5: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	30	pF	$V_{CC} = 5.0V$

Physical Dimensions inches (millimeters) unless otherwise noted

0.620 – 0.630
[15.75 – 16.00]
– A –

48   25

LEAD #1
IDENT

0.398 – 0.417
[10.10 – 10.60]

⬭ 0.010[0.25] C B Ⓢ A Ⓢ

0.291 – 0.299
[7.40 – 7.59]
– B –

1   24

0.025
[0.635] TYP

0.020±0.003
[0.51 ± 0.08]
TYP

0.008 – 0.012
[0.21 – 0.30] TYP

⬭ 0.0031[0.08]Ⓜ C A Ⓢ B Ⓢ

0.005 – 0.009
[0.13 – 0.22]

GAUGE PLANE

0.010
[0.25]

0.020 – 0.040
[0.51 – 1.01]

DETAIL E TYP

0.096 – 0.108
[2.44 – 2.74]

SEATING PLANE

45° x 0.015 – 0.025
[0.39 – 0.63]

SEE DETAIL E

– D –

0.025
[0.635] TYP

0.10
[0.25] MIN TYP

– C –

0° – 8° TYP

▱ 0.004[0.10]

MS48A (REV E)
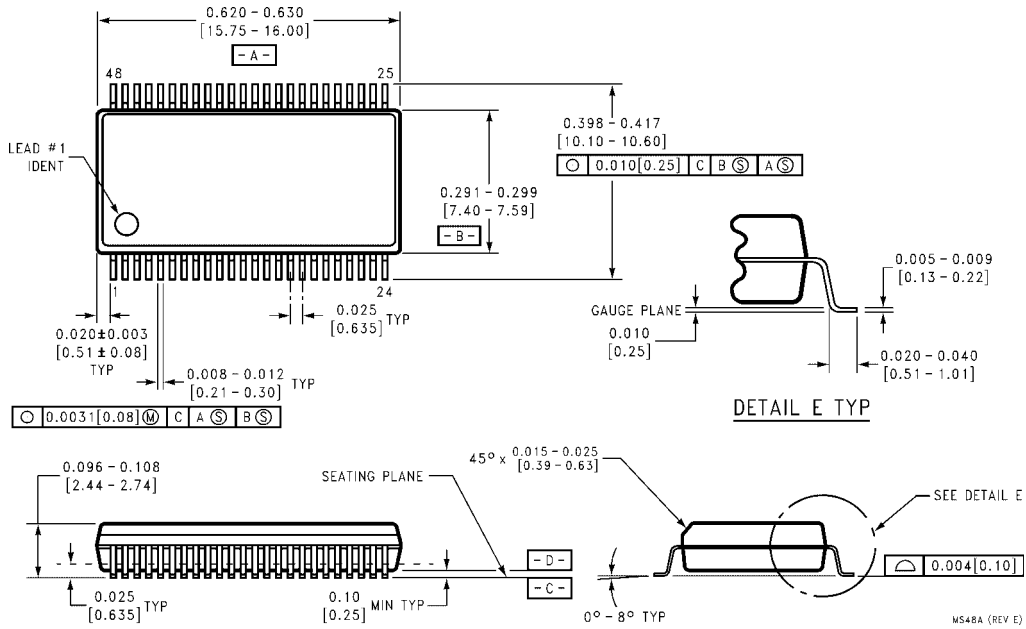
48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

12.50±0.10

0.40 TYP

48   43   30   25

-A-

-B-

8.10

6.10±0.10

4.05

PIN #1 IDENT.

1   6   19   24

⌕ 0.2 C B A
ALL LEAD TIPS

48   43   30   25

4.60

9.20

2.30

1   6   19   24

0.30

0.50

LAND PATTERN RECOMMENDATION

⌕ 0.1 C
ALL LEAD TIPS

1.2 MAX

-C-

0.50

0.17–0.27

0.90 +0.15 −0.10

0.10±0.05

⌖ 0.13 Ⓜ A BⓈ CⓈ

DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO−153, VARIATION ED,
   DATE 4/97.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH,
   AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48REVC

SEE DETAIL A

0.09–0.20

12.00° TOP & BOTTOM

R0.16

R0.31

0°–8°

0.60±0.10

1.00

GAGE PLANE

0.25

SEATING PLANE

DETAIL A

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.