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FAIRCHILD SEMICONDUCTOR®

April 2007

74AC253, 74ACT253
Dual 4-Input Multiplexer with 3-STATE Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- Multifunction capability
- Non inverting 3-STATE outputs
- Outputs source/sink 24mA
- ACT253 has TTL-compatible inputs

General Description

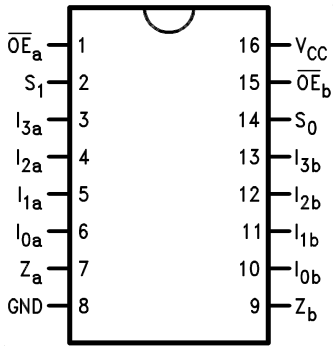
The AC/ACT253 is a dual 4-input multiplexer with 3-STATE outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

Ordering Information

Order Number	Package Number	Package Description
74AC253SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC253SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC253PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT253SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT253SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT253MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

Connection Diagram



Pin Descriptions

Pin Names	Description
I_{0a}–I_{3a}	Side A Data Inputs
I_{0b}–I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{OE}_a$	Side A Output Enable Input
$\overline{OE}_b$	Side B Output Enable Input
Z_a, Z_b	3-STATE Outputs

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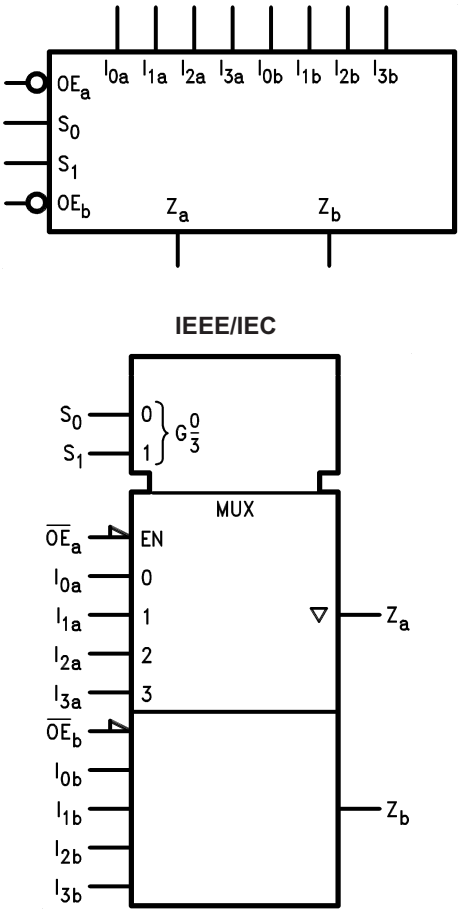
Logic Diagram



Functional Description

The AC/ACT253 contains two identical 4-input multiplexers with 3-STATE outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown:

$$Z_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-STATE devices whose outputs are tied together are designed so that there is no overlap.

Truth Table

Select Inputs		Data Inputs				Output Enable	Outputs
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address Inputs S_0 and S_1 are common to both sections.

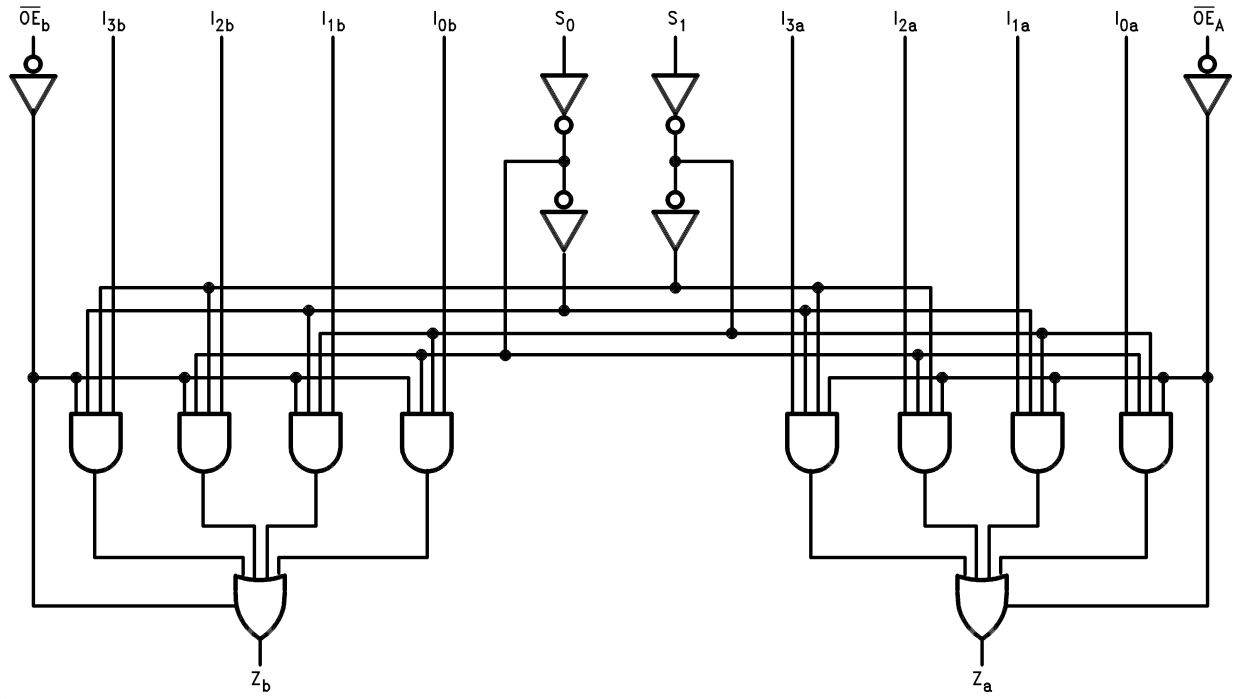
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 1.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
I_{IK}	DC Input Diode Current	
	$V_I = –0.5V$	–20mA
	$V_I = V_{CC} + 0.5V$	+20mA
V_I	DC Input Voltage	–0.5V to V_{CC} + 0.5V
I_{OK}	DC Output Diode Current	
	$V_O = –0.5V$	–20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	
	AC	2.0V to 6.0V
	ACT	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	–40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices:	125mV/ns
	V_{IN} from 30% to 70% of V_{CC}, V_{CC} @ 3.3V, 4.5V, 5.5V	
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices:	125mV/ns
	V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C	T_A = –40°C to +85°C		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	3.0	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	2.1	2.1	V
		4.5		2.25	3.15	3.15	
		5.5		2.75	3.85	3.85	
V_{IL}	Maximum LOW Level Input Voltage	3.0	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	0.9	0.9	V
		4.5		2.25	1.35	1.35	
		5.5		2.75	1.65	1.65	
V_{OH}	Minimum HIGH Level Output Voltage	3.0	I_{OUT} = –50µA	2.99	2.9	2.9	V
		4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
		3.0	V_{IN} = V_{IL} or V_{IH}: I_{OH} = –12mA		2.56	2.46	
		4.5	I_{OH} = –24mA		3.86	3.76	
		5.5	I_{OH} = –24mA(1)		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	3.0	I_{OUT} = 50µA	0.002	0.1	0.1	V
		4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
		3.0	V_{IN} = V_{IL} or V_{IH}: I_{OL} = 12mA		0.36	0.44	
		4.5	I_{OL} = 24mA		0.36	0.44	
		5.5	I_{OL} = 24mA(1)		0.36	0.44	
I_{IN}(3)	Maximum Input Leakage Current	5.5	V_I = V_{CC}, GND		±0.1	±1.0	µA
I_{OZ}	Maximum 3-STATE Current	5.5	V_I (OE) = V_{IL}, V_{IH}; V_I = V_{CC}, GND; V_O = V_{CC}, GND		±0.25	±2.5	µA
I_{OLD}	Minimum Dynamic Output Current(2)	5.5	V_{OLD} = 1.65V Max.			75	mA
I_{OHD}		5.5	V_{OHD} = 3.85V Min.			–75	mA
I_{CC}(3)	Maximum Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND		4.0	40.0	µA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C	T_A = –40°C to +85°C		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	4.5	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	2.0	2.0	V
		5.5		1.5	2.0	2.0	
V_{IL}	Maximum LOW Level Input Voltage	4.5	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	0.8	0.8	V
		5.5		1.5	0.8	0.8	
V_{OH}	Minimum HIGH Level Output Voltage	4.5	I_{OUT} = –50µA	4.49	4.4	4.4	V
		5.5		5.49	5.4	5.4	
		4.5	V_{IN} = V_{IL} or V_{IH}: I_{OH} = –24mA		3.86	3.76	
		5.5	I_{OH} = –24mA[4]		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	4.5	I_{OUT} = 50µA	0.001	0.1	0.1	V
		5.5		0.001	0.1	0.1	
		4.5	V_{IN} = V_{IL} or V_{IH}: I_{OL}= 24mA		0.36	0.44	
		5.5	I_{OL} = 24mA[4]		0.36	0.44	
I_{IN}	Maximum Input Leakage Current	5.5	V_I = V_{CC}, GND		±0.1	±1.0	µA
I_{OZ}	Maximum 3-STATE Current	5.5	V_I = V_{IL}, V_{IH}; V_O = V_{CC}, GND		±0.25	±2.5	µA
I_{CCT}	Maximum I_{CC}/Input	5.5	V_I = V_{CC} – 2.1V	0.6		1.5	mA
I_{OLD}	Minimum Dynamic Output Current[5]	5.5	V_{OLD} = 1.65V Max.			75	mA
I_{OHD}		5.5	V_{OHD} = 3.85V Min.			–75	mA
I_{CC}	Maximum Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND		4.0	40.0	µA

Notes:

4. All outputs loaded; thresholds on input associated with output under test.

5. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)[6]	T_A = +25°C, C_L = 50pF			T_A = –40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min	Max	
t_{PLH}	Propagation Delay, S_n to Z_n	3.3	2.0	8.5	15.5	2.0	17.5	ns
		5.0	2.0	6.5	11.0	1.5	12.5	
t_{PHL}	Propagation Delay, S_n to Z_n	3.3	2.5	9.5	16.0	2.0	18.0	ns
		5.0	2.0	7.0	11.5	1.5	13.0	
t_{PLH}	Propagation Delay, I_n to Z_n	3.3	1.5	7.0	14.5	1.5	17.0	ns
		5.0	1.5	5.5	10.0	1.5	11.5	
t_{PHL}	Propagation Delay, I_n to Z_n	3.3	2.0	7.5	13.0	1.5	15.0	ns
		5.0	1.5	5.5	9.5	1.5	11.0	
t_{PZH}	Output Enable Time	3.3	1.5	4.5	8.0	1.0	8.5	ns
		5.0	1.5	3.5	6.0	1.0	6.5	
t_{PZL}	Output Enable Time	3.3	1.5	5.0	8.0	1.0	9.0	ns
		5.0	1.5	3.5	6.0	1.0	7.0	
t_{PHZ}	Output Disable Time	3.3	2.0	5.5	9.5	1.5	10.0	ns
		5.0	2.0	5.0	8.0	1.5	8.5	
t_{PLZ}	Output Disable Time	3.3	1.5	5.0	8.0	1.0	9.0	ns
		5.0	1.5	4.0	7.0	1.0	7.5	

Note:

6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)[7]	T_A = +25°C, C_L = 50pF			T_A = –40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, S_n to Z_n	5.0	2.0	7.0	11.5	2.0	13.0	ns
t_{PHL}	Propagation Delay, S_n to Z_n	5.0	3.0	7.5	13.0	2.5	14.5	ns
t_{PLH}	Propagation Delay, I_n to Z_n	5.0	2.5	5.5	10.0	2.0	11.0	ns
t_{PHL}	Propagation Delay, I_n to Z_n	5.0	3.5	6.5	11.0	3.0	12.5	ns
t_{PZH}	Output Enable Time	5.0	2.0	4.5	7.5	1.5	8.5	ns
t_{PZL}	Output Enable Time	5.0	2.0	5.0	8.0	1.5	9.0	ns
t_{PHZ}	Output Disable Time	5.0	3.0	6.0	9.5	2.5	10.0	ns
t_{PLZ}	Output Disable Time	5.0	2.5	4.5	7.5	2.0	8.5	ns

Note:

7. Voltage range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN	4.5	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0V	50.0	pF

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

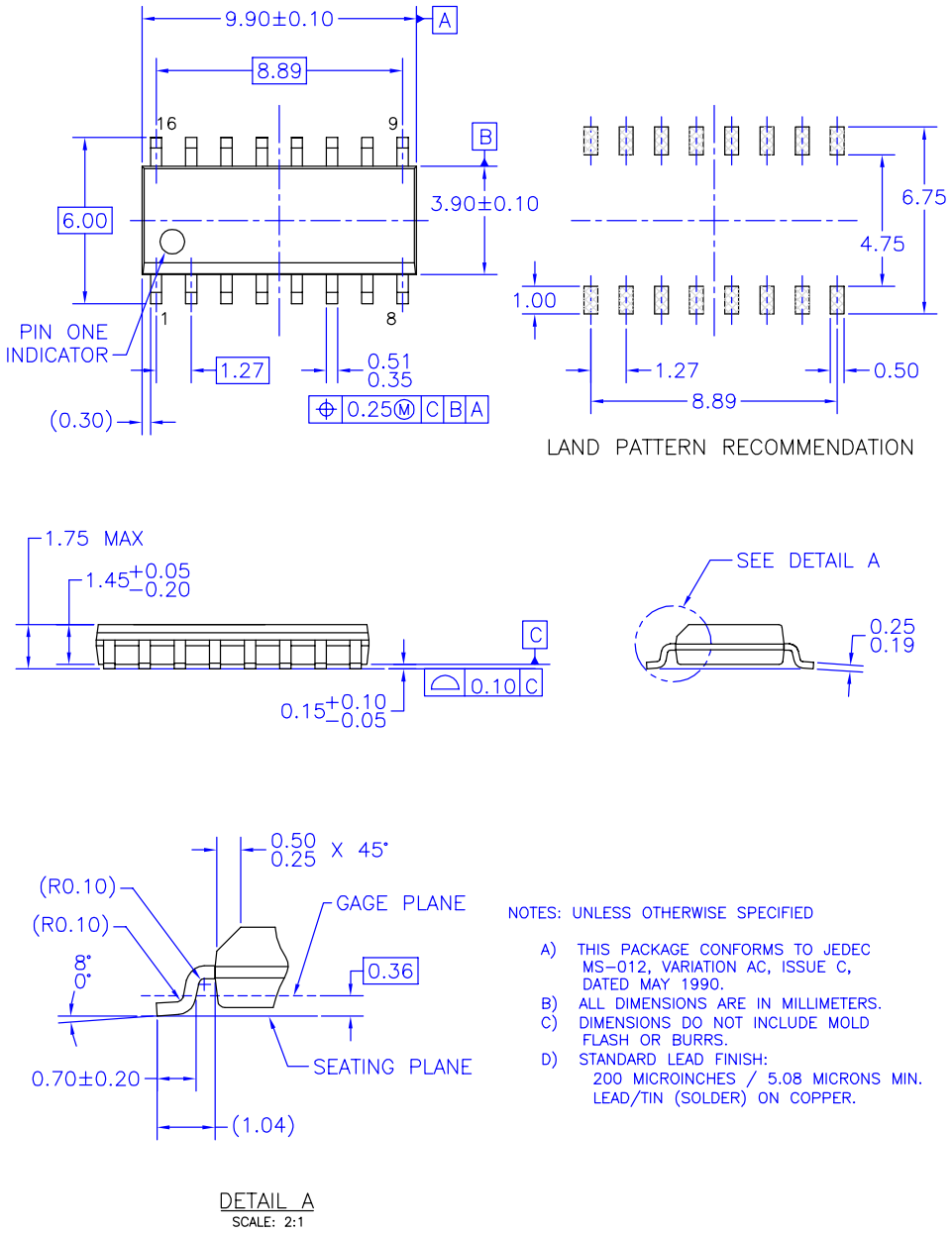
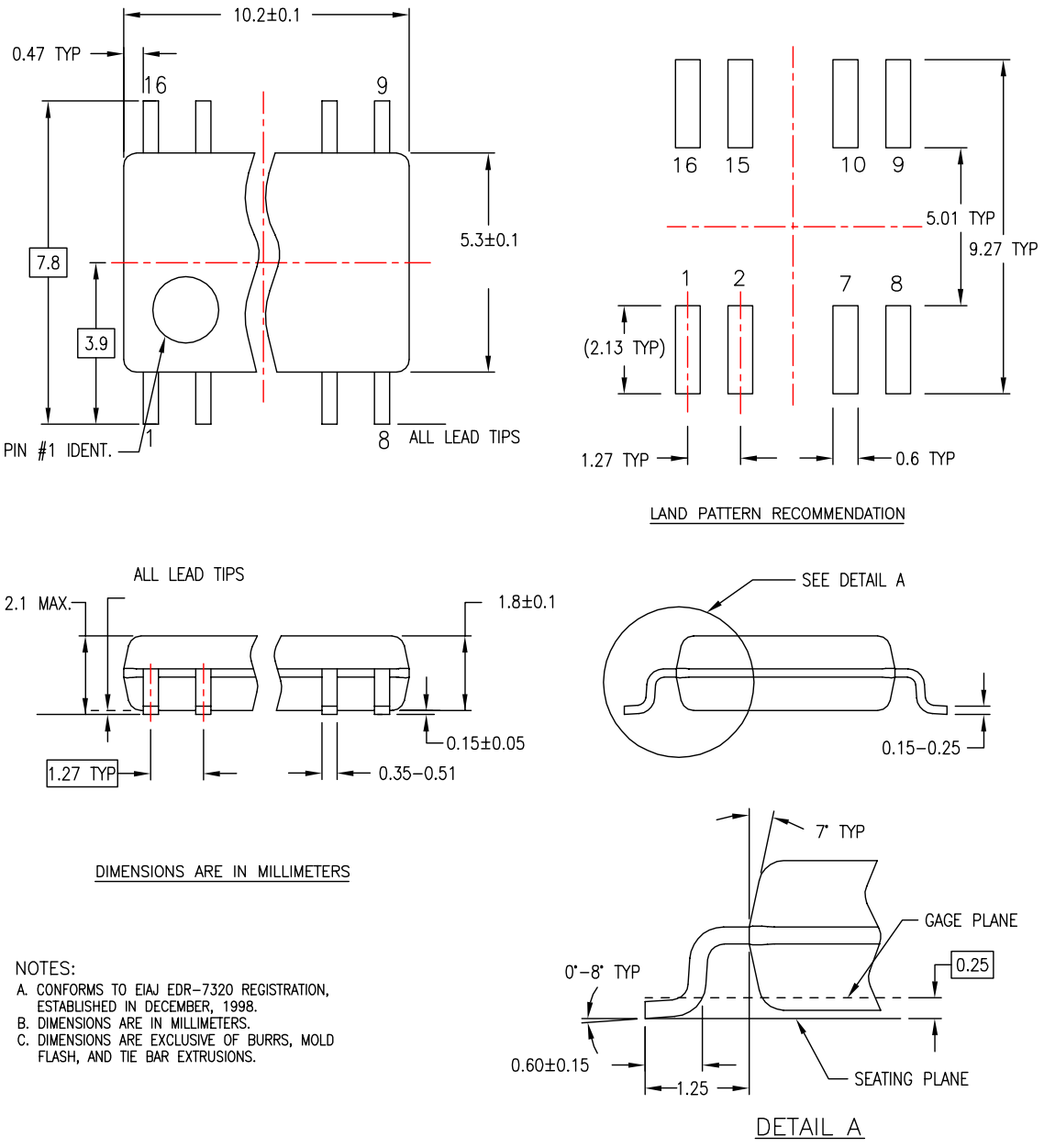


Figure 2. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

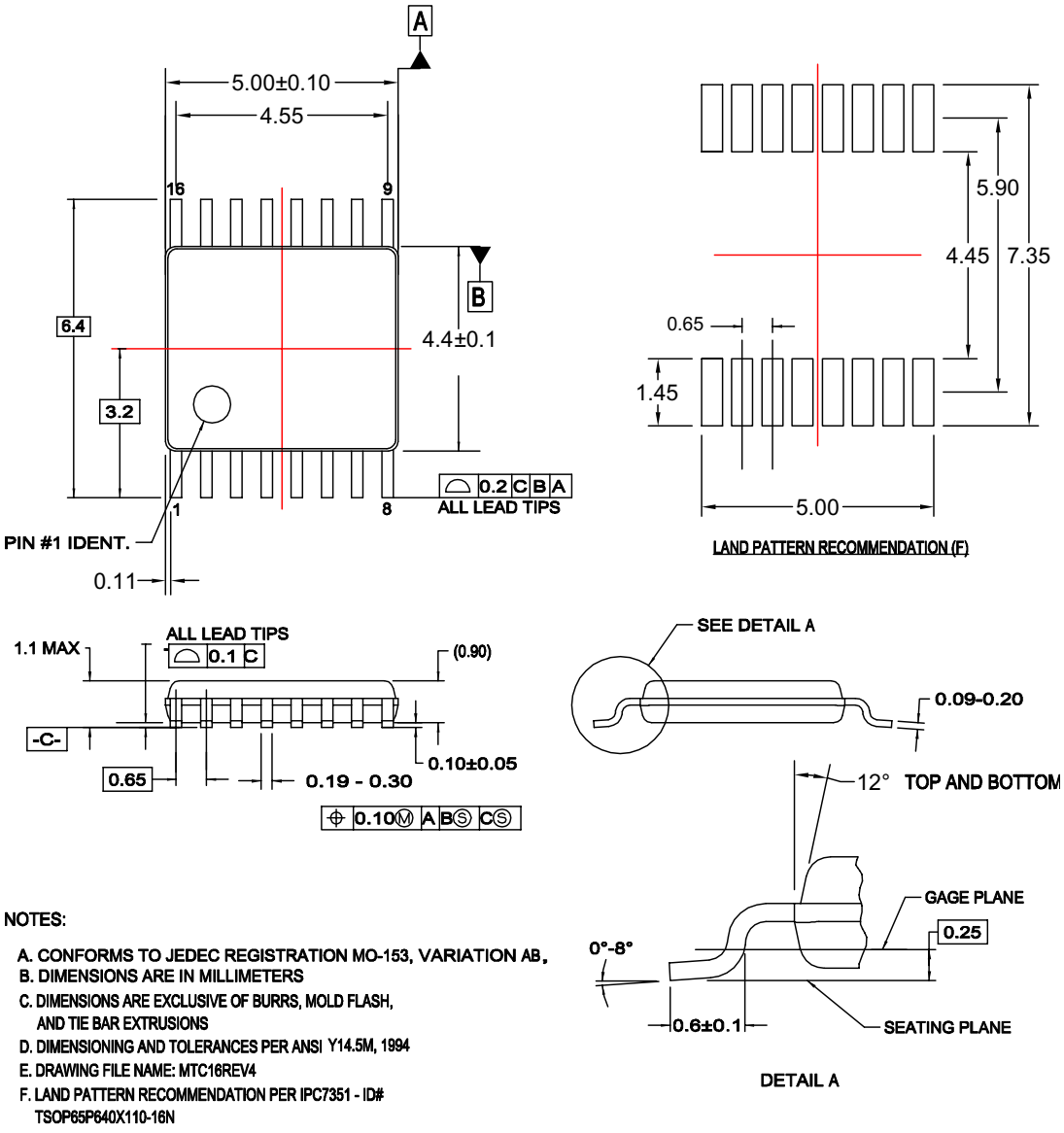
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DREVC

Figure 3. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB,
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1994
E. DRAWING FILE NAME: MTC16REV4
F. LAND PATTERN RECOMMENDATION PER IPC7351 - ID# TSOP65P640X110-16N

MTC16rev4

Figure 4. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

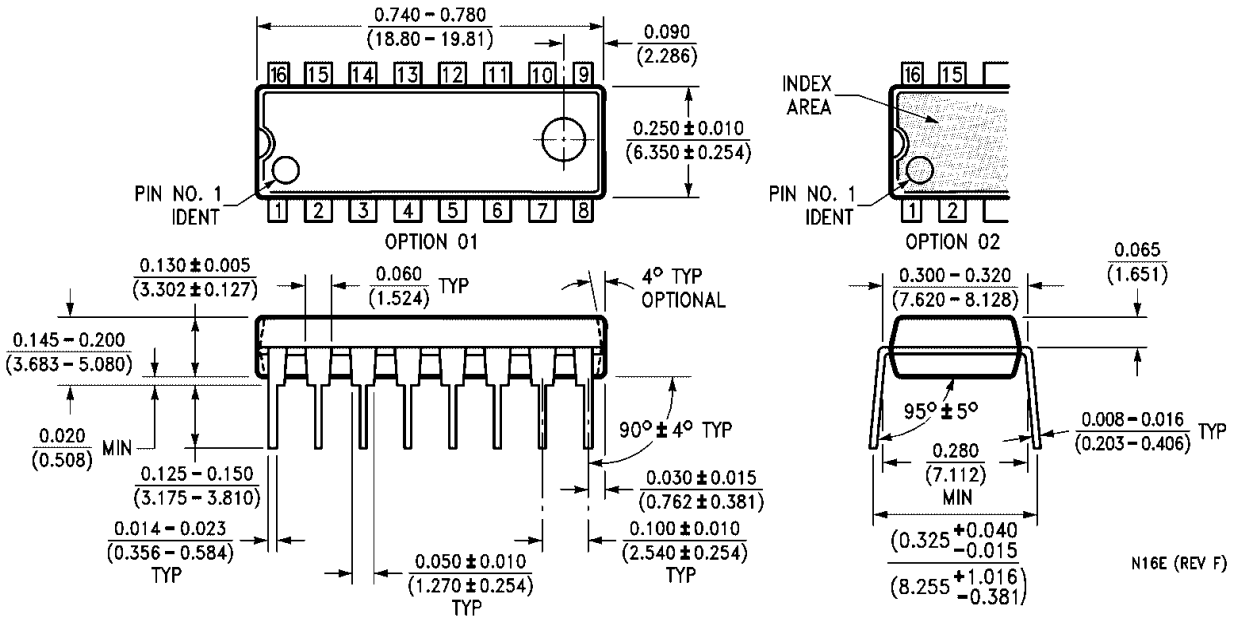


Figure 5. 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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