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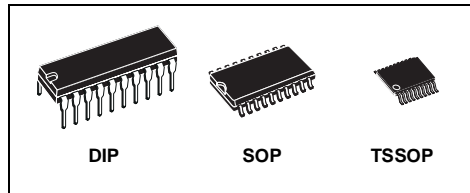




# 74ACT373

## OCTAL D-TYPE LATCH WITH 3 STATE OUTPUTS (NON INVERTED)

- HIGH SPEED:  $t_{PD} = 6ns$  (TYP.) at  $V_{CC} = 5V$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4\mu A$ (MAX.) at  $T_A=25^\circ C$
- COMPATIBLE WITH TTL OUTPUTS  
 $V_{IH} = 2V$  (MIN.),  $V_{IL} = 0.8V$  (MAX.)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 24mA$  (MIN)
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \equiv t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC}$  (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 373
- IMPROVED LATCH-UP IMMUNITY



### ORDER CODES

PACKAGE	TUBE	T & R
DIP	74ACT373B	
SOP	74ACT373M	74ACT373MTR
TSSOP		74ACT373TTR

### DESCRIPTION

The 74ACT373 is a high-speed CMOS OCTAL D-TYPE LATCH with 3 STATE OUTPUT NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

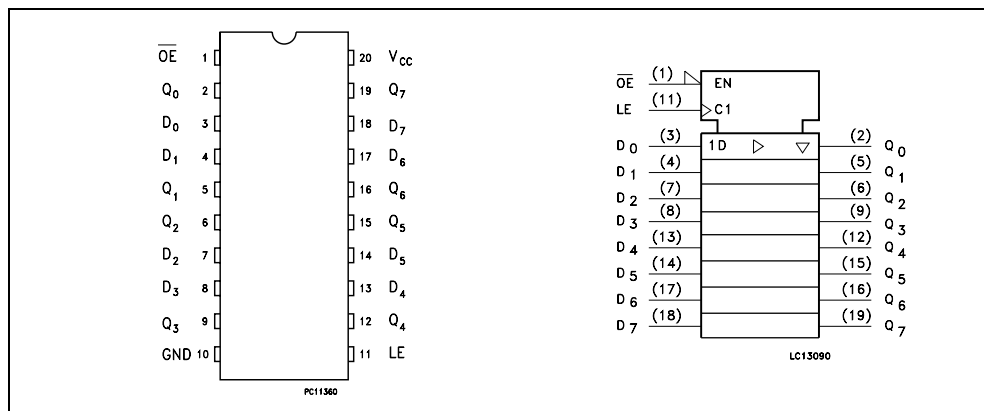
These 8 bit D-Type latch are controlled by a latch enable input (LE) and an output enable input ( $\overline{OE}$ ). When the (LE) input is high, the Q outputs follow the data (D) inputs. When the (LE) is taken low, the Q outputs will be latched at the logic levels set

up at the D inputs. When the ( $\overline{OE}$ ) input is low, the 8 outputs will be in a normal logic state (high or low logic level); when the ( $\overline{OE}$ ) input is high, the outputs will be in a high impedance state.

This device is designed to interface directly High Speed CMOS systems with TTL and NMOS components.

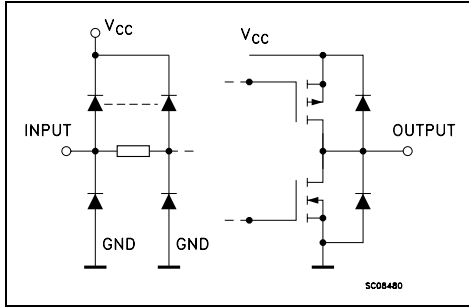
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



## 74ACT373

### INPUT AND OUTPUT EQUIVALENT CIRCUIT



### PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	OE	3 state Output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	3-State Outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	V <sub>CC</sub>	Positive Supply Voltage

### TRUTH TABLE

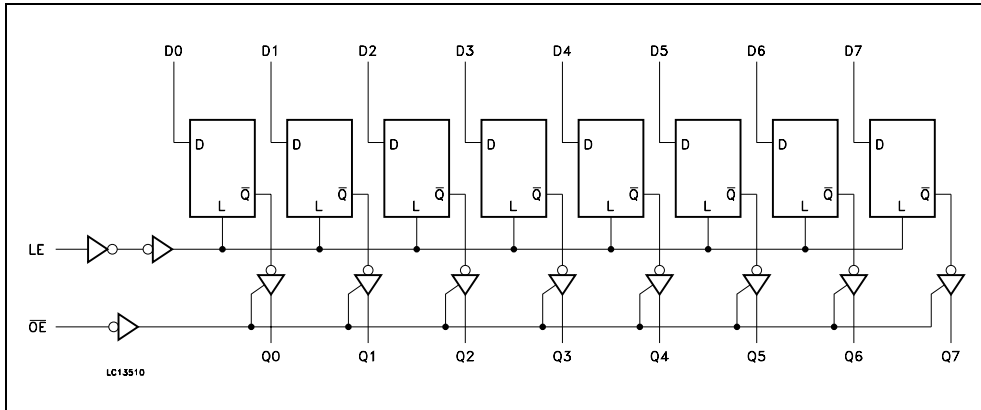
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE
L	H	L	L
L	H	H	H

X : Don't care

Z : High Impedance

NOTE: Outputs are latched at the time when the input is taken LOW logic level

### LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 400$	mA
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	4.5 to 5.5	V
$V_I$	Input Voltage	0 to $V_{CC}$	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time $V_{CC} = 4.5$ to $5.5V$ (note 1)	8	ns/V

1)  $V_{IN}$  from 0.8V to 2.0V

## 74ACT373

### DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	4.5	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> -0.1V	2.0	1.5		2.0		2.0		V
		5.5		2.0	1.5		2.0		2.0		
V <sub>IL</sub>	Low Level Input Voltage	4.5	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> -0.1V		1.5	0.8		0.8		0.8	V
		5.5			1.5	0.8		0.8		0.8	
V <sub>OH</sub>	High Level Output Voltage	4.5	I <sub>O</sub> =-50 μA	4.4	4.49		4.4		4.4		V
		5.5	I <sub>O</sub> =-50 μA	5.4	5.49		5.4		5.4		
		4.5	I <sub>O</sub> =-24 mA	3.86			3.76		3.7		
		5.5	I <sub>O</sub> =-24 mA	4.86			4.76		4.7		
V <sub>OL</sub>	Low Level Output Voltage	4.5	I <sub>O</sub> =50 μA		0.001	0.1		0.1		0.1	V
		5.5	I <sub>O</sub> =50 μA		0.001	0.1		0.1		0.1	
		4.5	I <sub>O</sub> =24 mA			0.36		0.44		0.5	
		5.5	I <sub>O</sub> =24 mA			0.36		0.44		0.5	
I <sub>I</sub>	Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			± 0.1		± 1		± 1	μA
I <sub>OZ</sub>	High Impedance Output Leakage Current	5.5	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND			± 0.5		± 5		± 5	μA
I <sub>CC(T)</sub>	Max I <sub>CC</sub> /Input	5.5	V <sub>I</sub> = V <sub>CC</sub> - 2.1V		0.6			1.5		1.6	mA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			4		40		80	μA
I <sub>OLD</sub>	Dynamic Output Current (note 1, 2)	5.5	V <sub>OLD</sub> = 1.65 V max					75		50	mA
I <sub>OHD</sub>			V <sub>OHD</sub> = 3.85 V min					-75		-50	mA

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50Ω

### AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, R<sub>L</sub> = 500 Ω, Input t<sub>r</sub> = t<sub>f</sub> = 3ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time LE to Q	5.0(*)			5.5	10.0		11.5		11.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time D to Q	5.0(*)			6.0	10.0		11.5		11.5	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time	5.0(*)			6.0	9.5		10.5		10.5	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time	5.0(*)			7.0	11.0		12.5		12.5	ns
t <sub>w</sub>	LE Minimum Pulse Width, HIGH	5.0(*)			1.3	7.0		8.0		8.0	ns
t <sub>s</sub>	Setup Time D to LE, HIGH or LOW	5.0(*)			-0.5	7.0		8.0		8.0	ns
t <sub>h</sub>	Hold Time D to LE, HIGH or LOW	5.0(*)			0.5	0.0		1.0		1.0	ns

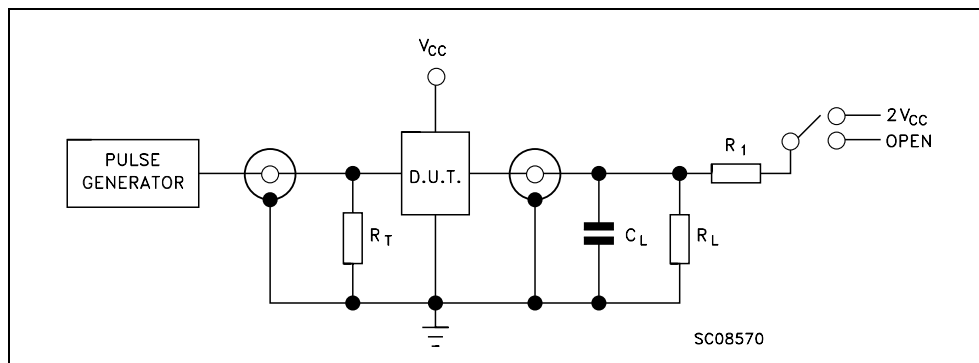
(\*) Voltage range is 5.0V ± 0.5V

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C <sub>IN</sub>	Input Capacitance	5.0			4						pF
C <sub>OUT</sub>	Output Capacitance	5.0			8						pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)	5.0	f <sub>IN</sub> = 10MHz		25						pF

1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/n$  (per circuit)

## TEST CIRCUIT



TEST	SWITCH
t <sub>PLH</sub> , t <sub>PHL</sub>	Open
t <sub>PZL</sub> , t <sub>PLZ</sub>	2V <sub>CC</sub>
t <sub>PZH</sub> , t <sub>PHZ</sub>	Open

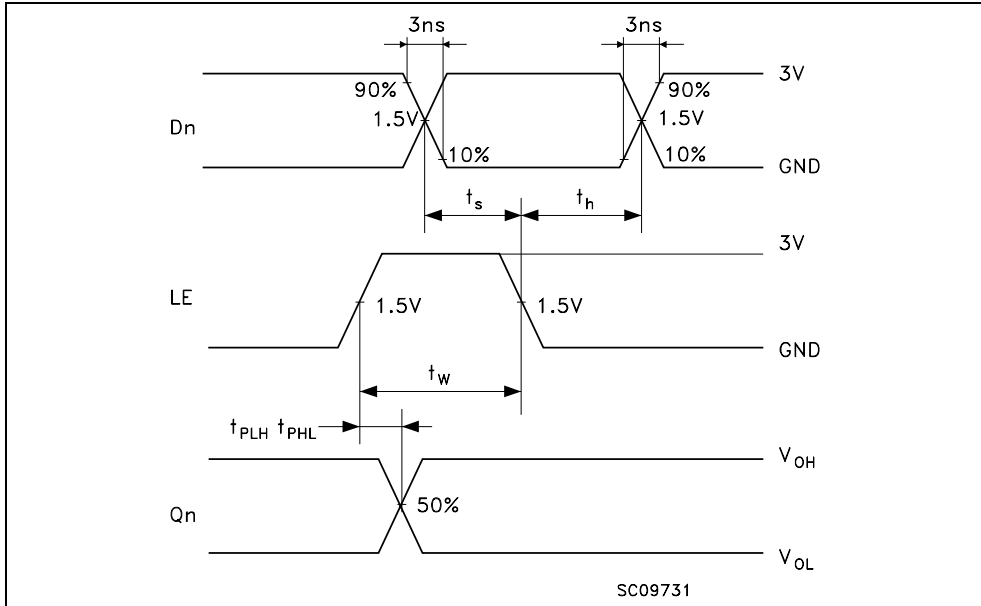
C<sub>L</sub> = 50pF or equivalent (includes jig and probe capacitance)

R<sub>L</sub> = R<sub>1</sub> = 500Ω or equivalent

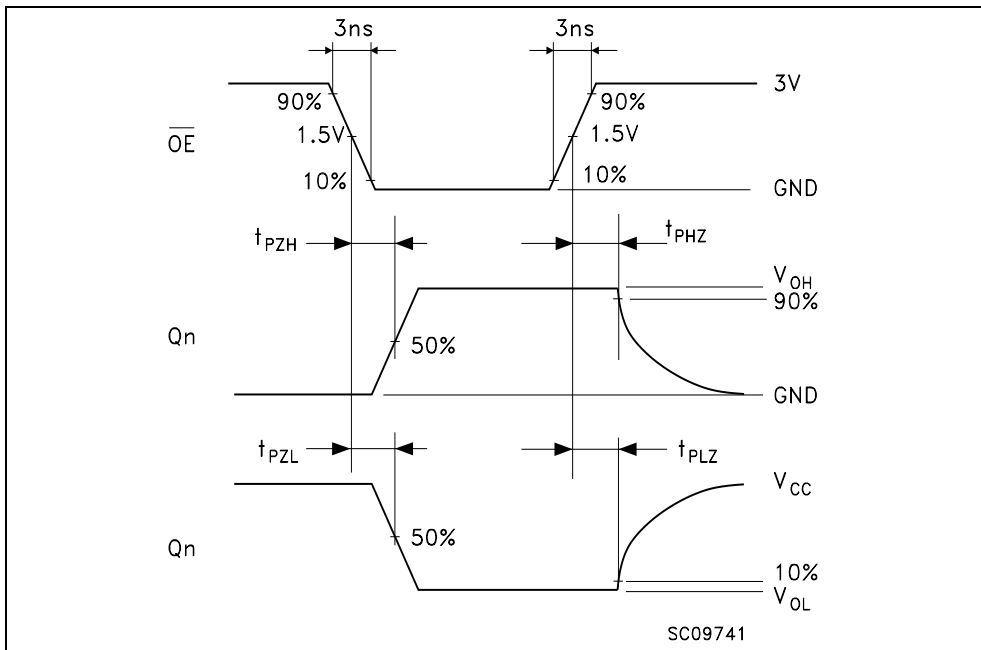
R<sub>T</sub> = Z<sub>OUT</sub> of pulse generator (typically 50Ω)

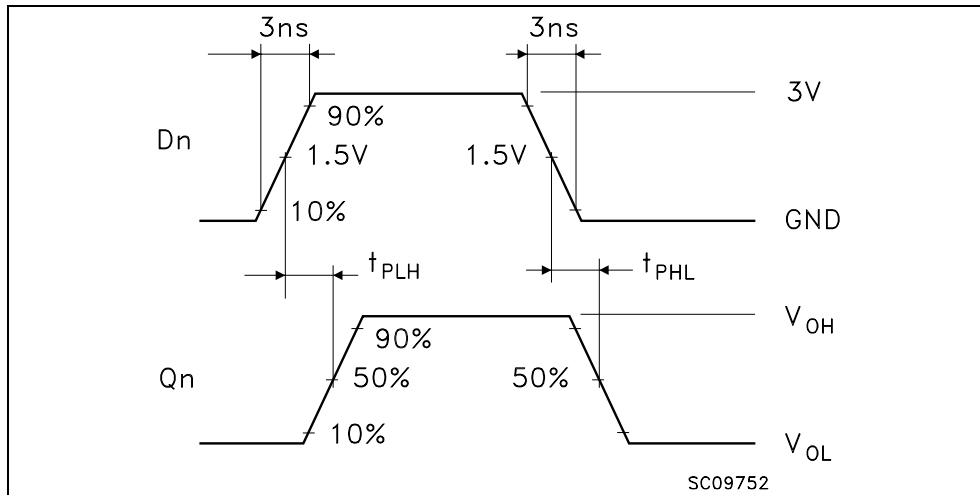
**74ACT373**

**WAVEFORM 1: PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn TO LE SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)**



**WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES (f=1MHz; 50% duty cycle)**

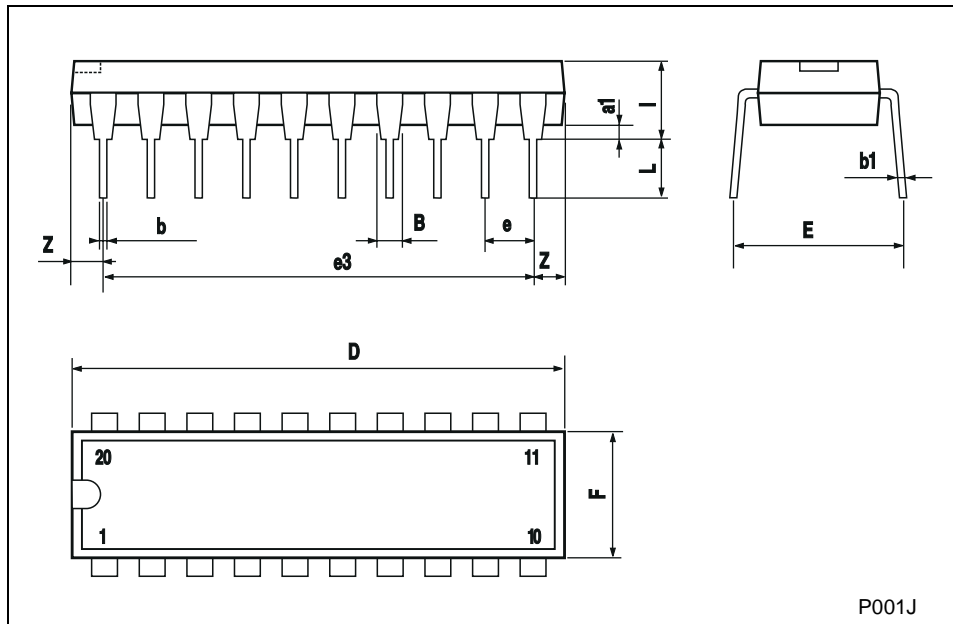


**WAVEFORM 3: PROPAGATION DELAYS TIME** (f=1MHz; 50% duty cycle)



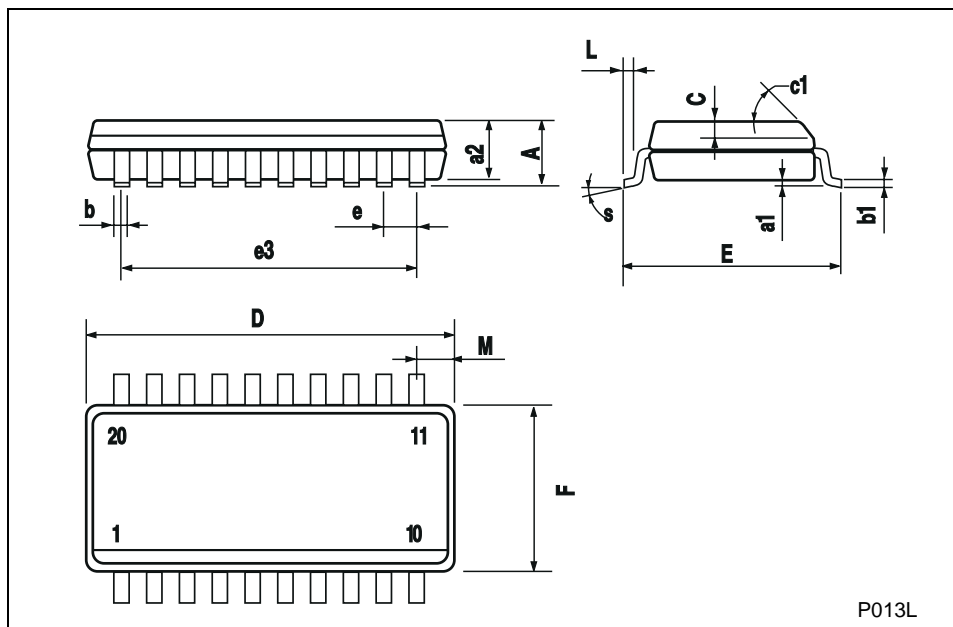
**Plastic DIP-20 (0.25) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
l			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



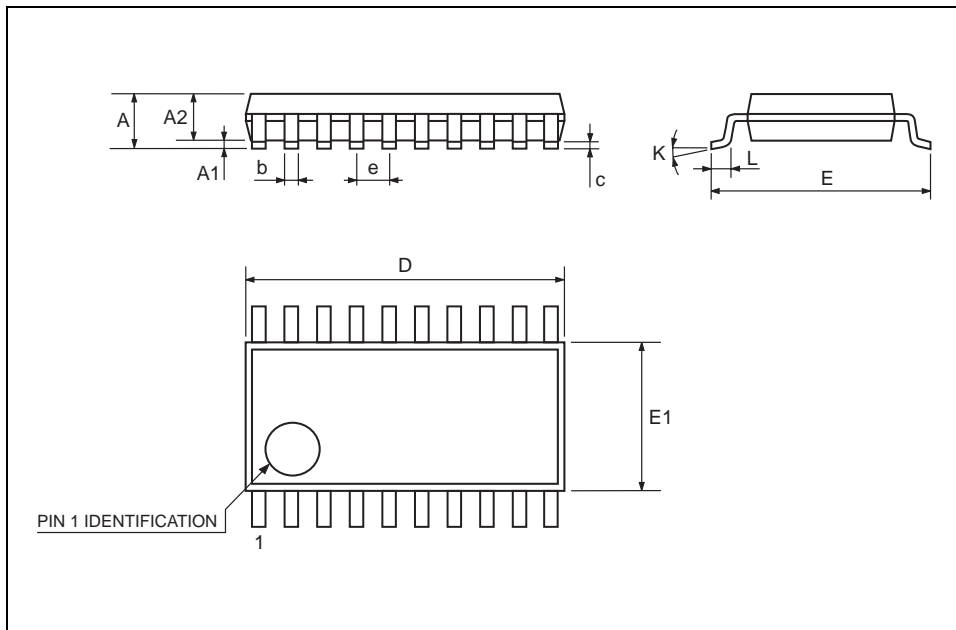
## SO-20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8 (max.)					



## TSSOP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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