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## 74ACT534

### Octal D-Type Flip-Flop with 3-STATE Outputs

#### General Description

The ACT534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ( $\overline{OE}$ ) are common to all flip-flops. The ACT534 is the same as the ACT374 except that the outputs are inverted.

#### Features

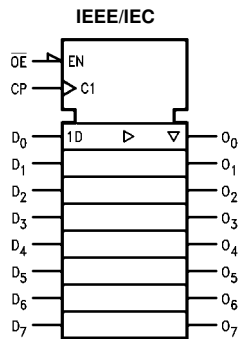
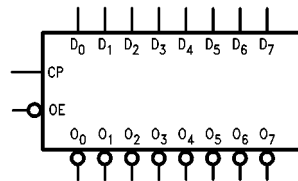
- $I_{CC}$  and  $I_{OZ}$  reduced by 50%
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- 3-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- ACT534 has TTL-compatible inputs
- Inverted output version of ACT374

#### Ordering Code:

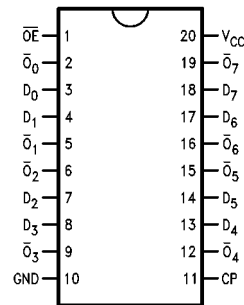
Order Number	Package Number	Package Description
74ACT534SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ACT534SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT534PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### Logic Symbols



#### Connection Diagram



#### Pin Descriptions

Pin Names	Description
$D_0$ - $D_7$	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-STATE Output Enable Input
$\overline{O_0}$ - $\overline{O_7}$	Complementary 3-STATE Outputs

FACT™ is a trademark of Fairchild Semiconductor Corporation.

## Functional Description

The ACT534 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP)

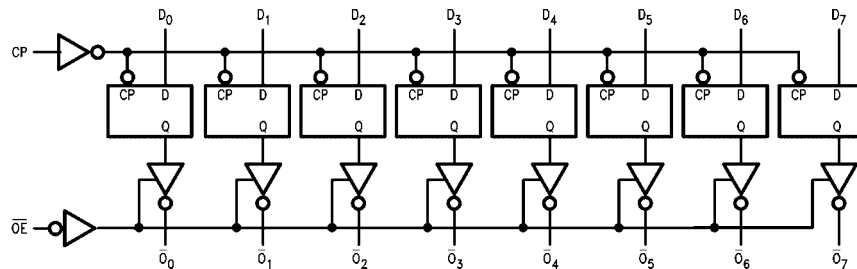
transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Function Table

Inputs			Output
CP	OE	D	$\overline{O}$
↗	L	H	L
↗	L	L	H
L	L	X	$\overline{O}_0$
X	H	X	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↗ = LOW-to-HIGH Clock Transition  
 Z = High Impedance  
 $\overline{O}_0$  = Value stored from previous clock cycle

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
PDIP	140°C

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
$V_{IH}$	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	1.5	2.0	2.0			
$V_{IL}$	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	1.5	0.8	0.8			
$V_{OH}$	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$	
		5.5	5.49	5.4	5.4			
			4.5		3.86	3.76	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA (Note 2)}$
			5.5		4.86	4.76		
$V_{OL}$	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		5.5	0.001	0.1	0.1			
			4.5		0.36	0.44	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA (Note 2)}$
			5.5		0.36	0.44		
$I_{IN}$	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\mu A$	$V_I = V_{CC}, GND$	
$I_{OZ}$	Maximum 3-STATE Current	5.5		$\pm 0.25$	$\pm 2.5$	$\mu A$	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$	
$I_{CCT}$	Maximum $I_{CC}/\text{Input}$	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$	
$I_{OLD}$	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V \text{ Max}$	
$I_{OHD}$	Output Current (Note 3)	5.5			-75	mA	$V_{OHD} = 3.85V \text{ Min}$	
$I_{CC}$	Maximum Quiescent Supply Current	5.5		4.0	40.0	$\mu A$	$V_{IN} = V_{CC}$ or GND	

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 4)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>MAX</sub>	Maximum Clock Frequency	5.0	100			120		MHz
t <sub>PLH</sub>	Propagation Delay CP to $\overline{Q}_n$	5.0	2.5	6.5	11.5	2.0	12.5	ns
t <sub>PHL</sub>	Propagation Delay CP to $\overline{Q}_n$	5.0	2.0	6.0	10.5	2.0	12.0	ns
t <sub>PZH</sub>	Output Enable Time	5.0	2.5	6.5	12.0	2.0	12.5	ns
t <sub>PZL</sub>	Output Enable Time	5.0	2.0	6.0	11.0	2.0	11.5	ns
t <sub>PHZ</sub>	Output Disable Time	5.0	1.5	7.0	12.5	1.0	13.5	ns
t <sub>PLZ</sub>	Output Disable Time	5.0	1.5	5.5	10.5	1.0	10.5	ns

Note 4: Voltage Range 5.0 is 5.0V ± 0.5V

## AC Operating Requirements

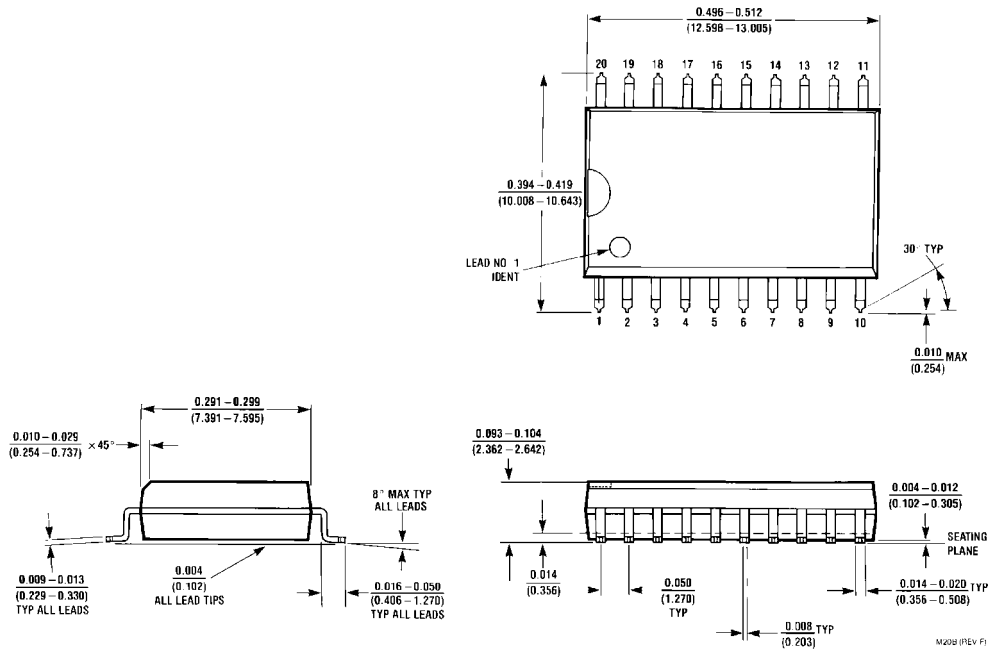
Symbol	Parameter	V <sub>CC</sub> (V) (Note 5)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Typ	Guaranteed Minimum			
t <sub>S</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	5.0	1.0	3.5	4.0		ns
t <sub>H</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	5.0	-1.0	1.0	1.5		ns
t <sub>w</sub>	CP Pulse Width HIGH or LOW	5.0	2.0	3.5	3.5		ns

Note 5: Voltage Range 5.0 is 5.0V ± 0.5V

## Capacitance

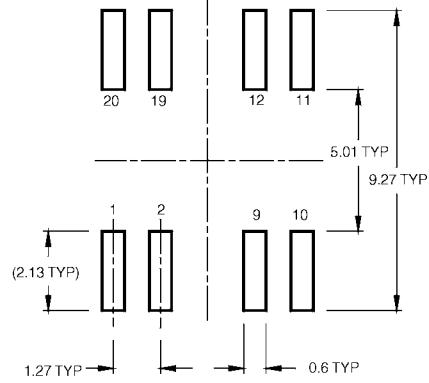
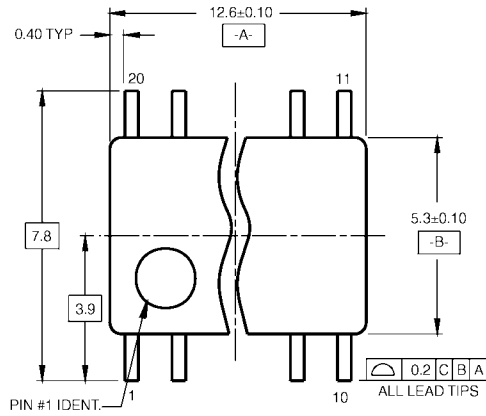
Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	40.0	pF	V <sub>CC</sub> = 5.0V

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body  
Package Number M20B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**

