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FAIRCHILD SEMICONDUCTOR™

July 1988
Revised September 2000

# 74ACT843
# 9-Bit Transparent Latch

## General Description

The ACT843 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths.

## Features

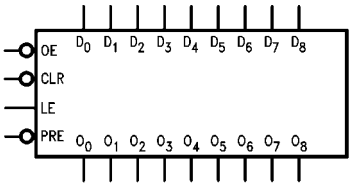
- TTL compatible inputs
- 3-STATE outputs for bus interfacing

## Ordering Code:

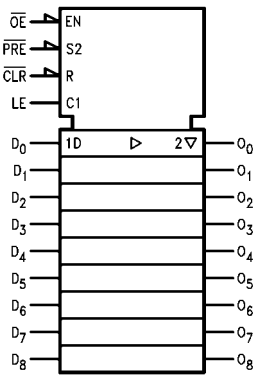
| Order Number | Package Number | Package Description |
|---|---|---|
| 74ACT843SC | M24B | 24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74ACT843SPC | N24C | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code. (SPC not available in Tape and Reel.)

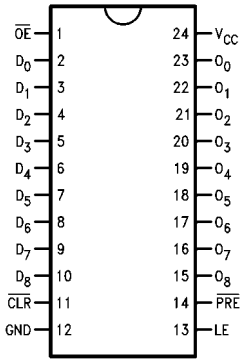
## Logic Symbols




**IEEE/IEC**




## Connection Diagram




## Pin Descriptions

| Pin Names | Description |
|---|---|
| $D_0$–$D_8$ | Data Inputs |
| $O_0$–$O_8$ | Data Outputs |
| $\overline{OE}$ | Output Enable |
| LE | Latch Enable |
| $\overline{CLR}$ | Clear |
| $\overline{PRE}$ | Preset |

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## Functional Description

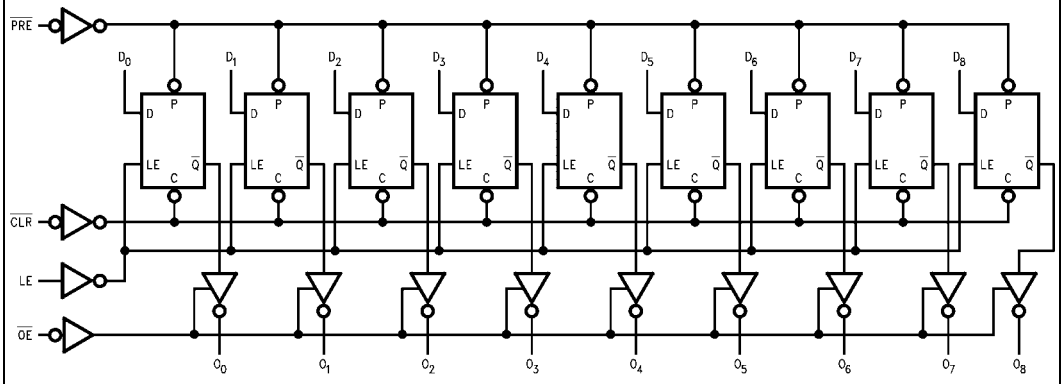
The ACT843 consists of nine D-type latches with 3-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state. In addition to the LE and $\overline{OE}$ pins, the ACT843 has a Clear ($\overline{CLR}$) pin and a Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

## Function Tables

| Inputs | | | | | Internal | Outputs | Function |
|---|---|---|---|---|---|---|---|
| $\overline{CLR}$ | $\overline{PRE}$ | $\overline{OE}$ | LE | D | Q | O | |
| H | H | H | H | L | L | Z | High Z |
| H | H | H | H | H | H | Z | High Z |
| H | H | H | L | X | NC | Z | Latched |
| H | H | L | H | L | L | L | Transparent |
| H | H | L | H | H | H | H | Transparent |
| H | H | L | L | X | NC | NC | Latched |
| H | L | L | X | X | H | H | Preset |
| L | H | L | X | X | L | L | Clear |
| L | L | L | X | X | H | H | Preset |
| L | H | H | L | X | L | Z | Clear/High Z |
| H | L | H | L | X | H | Z | Preset/High Z |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

## Logic Diagram



## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| $V_I$ = $V_{CC}$ +0.5V | +20 mA |
| DC Input Voltage ($V_I$) | −0.5V to $V_{CC}$ +0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| $V_O$ = $V_{CC}$ +0.5V | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to $V_{CC}$ +0.5V |
| DC Output Source or Sink Current ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current per Output Pin ($I_{CC}$ or $I_{GND}$) | ±50 mA |
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| Junction Temperature ($T_J$) | |
| PDIP | 140°C |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 4.5V to 5.5V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | −40°C to +85°C |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | 125 mV/ns |
| $V_{IN}$ from 0.8V to 2.0V | |
| $V_{CC}$ @ 4.5V, 5.5V | |

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

## DC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | $T_A$ = +25°C | $T_A$ = −40°C to +85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | |
| $V_{IH}$ | Minimum HIGH Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| | | 5.5 | 1.5 | 2.0 | 2.0 | | |
| $V_{IL}$ | Maximum LOW Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| | | 5.5 | 1.5 | 0.8 | 0.8 | | |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT}$ = −50 μA |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 4.5 | | 3.86 | 3.76 | V | $I_{OH}$ = −24 mA |
| | | 5.5 | | 4.86 | 4.76 | | $I_{OH}$ = −24 mA (Note 2) |
| $V_{OL}$ | Maximum LOW Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT}$ = 50 μA |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 4.5 | | 0.36 | 0.44 | V | $I_O$ = 24 mA |
| | | 5.5 | | 0.36 | 0.44 | | $I_{OL}$ = 24 mA (Note 2) |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $I_{OZ}$ | Maximum 3-STATE Leakage Current | 5.5 | | ±0.5 | ±5.0 | μA | $V_I$ = $V_{IL}$, $V_{IH}$ $V_O$ = $V_{CC}$, GND |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | 0.6 | | 1.5 | mA | $V_I$ = $V_{CC}$ − 2.1V |
| $I_{OLD}$ | Minimum Dynamic | 5.5 | | | 75 | mA | $V_{OLD}$ = 1.65V Max |
| $I_{OHD}$ | Output Current (Note 3) | 5.5 | | | −75 | mA | $V_{OHD}$ = 3.85V Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 80.0 | μA | $V_{IN}$ = $V_{CC}$ or GND |

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

## AC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) (Note 4) | $T_A = +25°C$, $C_L = 50$ pF | | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay $D_n$ to $O_n$ | 5.0 | 2.5 | 5.5 | 9.5 | 2.0 | 10.0 | ns |
| $t_{PHL}$ | Propagation Delay $D_n$ to $O_n$ | 5.0 | 2.5 | 5.5 | 9.5 | 2.0 | 10.0 | ns |
| $t_{PLH}$ | Propagation Delay LE to $O_n$ | 5.0 | 2.5 | 5.5 | 9.0 | 2.0 | 10.0 | ns |
| $t_{PHL}$ | Propagation Delay LE to $O_n$ | 5.0 | 2.5 | 5.5 | 9.0 | 2.0 | 10.0 | ns |
| $t_{PLH}$ | Propagation Delay $\overline{PRE}$ to $O_n$ | 5.0 | 2.5 | 6.5 | 14.0 | 2.0 | 16.0 | ns |
| $t_{PHL}$ | Propagation Delay $\overline{CLR}$ to $O_n$ | 5.0 | 2.5 | 7.5 | 15.5 | 2.0 | 17.5 | ns |
| $t_{PZH}$ | Output Enable Time $\overline{OE}$ to $O_n$ | 5.0 | 2.5 | 5.5 | 9.5 | 2.0 | 10.5 | ns |
| $t_{PZL}$ | Output Enable Time $\overline{OE}$ to $O_n$ | 5.0 | 2.5 | 5.5 | 9.5 | 2.0 | 10.5 | ns |
| $t_{PHZ}$ | Output Disable Time $\overline{OE}$ to $O_n$ | 5.0 | 2.5 | 6.0 | 10.5 | 2.0 | 11.0 | ns |
| $t_{PLZ}$ | Output Disable Time $\overline{OE}$ to $O_n$ | 5.0 | 2.5 | 6.0 | 10.5 | 2.0 | 11.0 | ns |
| $t_{PHL}$ | Propagation Delay $\overline{PRE}$ to $O_n$ | 5.0 | 2.5 | 6.0 | 10.5 | 2.0 | 11.0 | ns |
| $t_{PLH}$ | Propagation Delay $\overline{CLR}$ to $O_n$ | 5.0 | 2.5 | 5.5 | 9.5 | 2.0 | 10.5 | ns |

**Note 4:** Voltage Range 5.0 is 5.0V ± 0.5V

## AC Operating Requirements

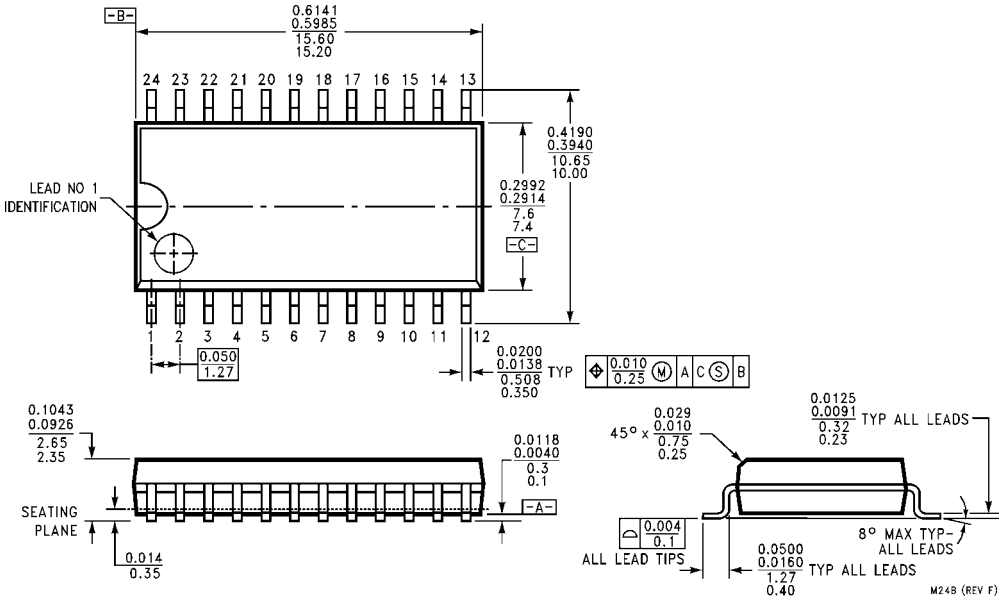
| Symbol | Parameter | $V_{CC}$ (V) (Note 5) | $T_A = +25°C$, $C_L = 50$ pF | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | Units |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | |
| $t_S$ | Setup Time, HIGH or LOW $D_n$ to LE | 5.0 | −0.5 | 0.5 | 1.0 | ns |
| $t_H$ | Hold Time, HIGH or LOW $D_n$ to LE | 5.0 | 0.5 | 2.0 | 2.0 | ns |
| $t_W$ | LE Pulse Width, HIGH | 5.0 | 2.0 | 3.5 | 3.5 | ns |
| $t_W$ | $\overline{PRE}$ Pulse Width, LOW | 5.0 | 5.0 | 8.5 | 10.0 | ns |
| $t_W$ | $\overline{CLR}$ Pulse Width, LOW | 5.0 | 5.5 | 9.5 | 11.0 | ns |
| $t_{rec}$ | $\overline{PRE}$ Recovery Time | 5.0 | 0.5 | 2.0 | 2.0 | ns |
| $t_{rec}$ | $\overline{CLR}$ Recovery Time | 5.0 | −0.5 | 1.0 | 1.0 | ns |

**Note 5:** Voltage Range 5.0 is 5.0V ± 0.5V

## Capacitance

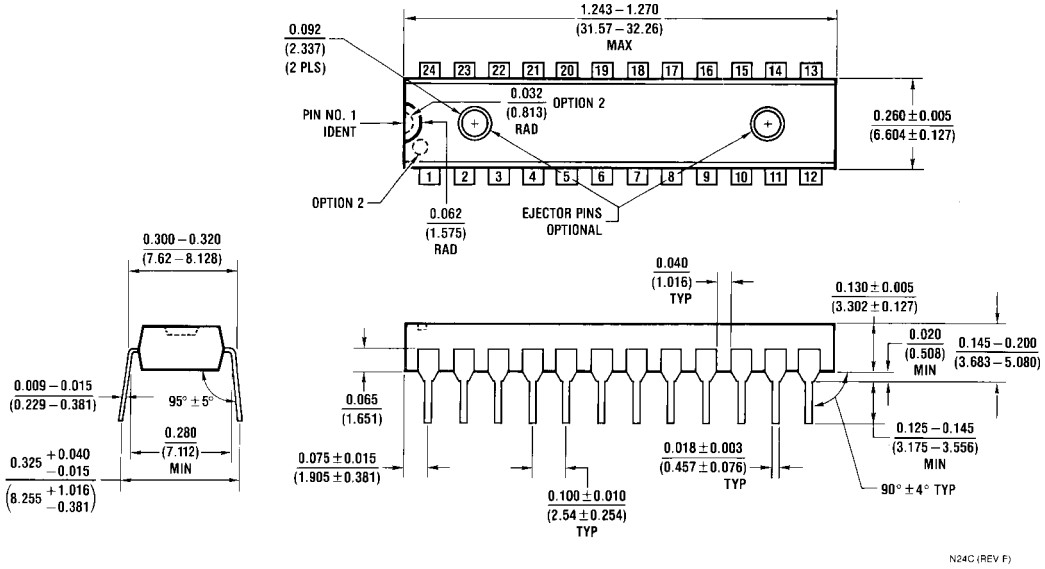
| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = OPEN |
| $C_{PD}$ | Power Dissipation Capacitance | 44 | pF | $V_{CC}$ = 5.0V |

## Physical Dimensions inches (millimeters) unless otherwise noted




**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide**
**Package Number M24B**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide**
**Package Number N24C**