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8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

Description

The 74AHC164 is a serial input 8-bit edge-triggered shift register that has outputs from each of eight stages.

SERIAL DATA INPUT PINS

The serial input data is entered at pin SDA or pin SDB as these are logically ANDED. Either input could be used as an active HIGH enable with data entry on the other pin. If a single input is desired, the pins can be tied together or the unused input can be tied HIGH.

DATA ENTRY

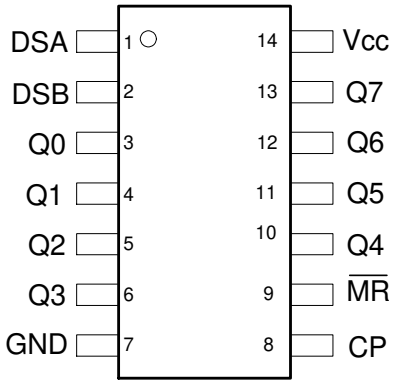
Data is shifted into Q0 from the serial input pins on each LOW to HIGH transition of the CP pin. Also during the CP edge the data is transferred from each Qn to Qn+1. The serial data on pins DSA and DSB must be stable before and after the CP rising edge to meet the set-up and hold timing requirements.

RESET

When asserted LOW the Master Reset ($\overline{MR}$) pin sets all Qn to LOW. This action does not depend on the condition of serial input or clock pins. The $\overline{MR}$ must be asserted HIGH for a recovery time before the next CP positive edge pulse.

Pin Assignments

(Top View)



SO-14 / TSSOP-14 / PDIP-14

Features

- Wide Supply Voltage Range from 2.0V to 5.5V
- Sinks or Sources 8mA at V_{CC} = 4.5V
- CMOS Low Power Consumption
- Schmitt Trigger Action at All Inputs
- ESD Protection Exceeds JESD 22
  - 200-V Machine Model (A115)
  - 2000-V Human Body Model (A114)
  - Exceeds 1000-V Charged Device Model (C101)
- Range of Package Options SO-14 and TSSOP-14
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

- General Purpose Logic
- Wide Array of Products Such as:
  - PCs, Networking, Notebooks, Netbooks
  - Computer Peripherals, Hard Drives, CD/DVD ROMs
  - TVs, DVDs, DVRs, Set-Top Boxes

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Device ordering information is on page 7

Pin Descriptions

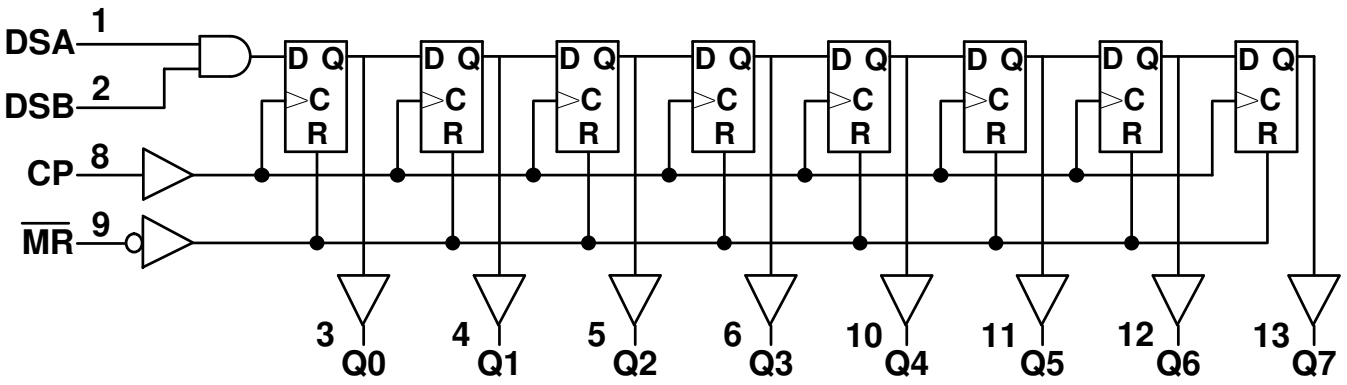
Pin Number	Pin Name	Function
1	DSA	Serial Data Input
2	DSB	Serial Data Input
3	Q0	Data Output
4	Q1	Data Output
5	Q2	Data Output
6	Q3	Data Output
7	GND	Ground
8	CP	Clock Pulse –Positive Edge Triggered
9	$\overline{MR}$	Master Reset - Asynchronous
10	Q4	Data Output
11	Q5	Data Output
12	Q6	Data Output
13	Q7	Data Output
14	V_{CC}	Supply Voltage

Function Table (Note 4)

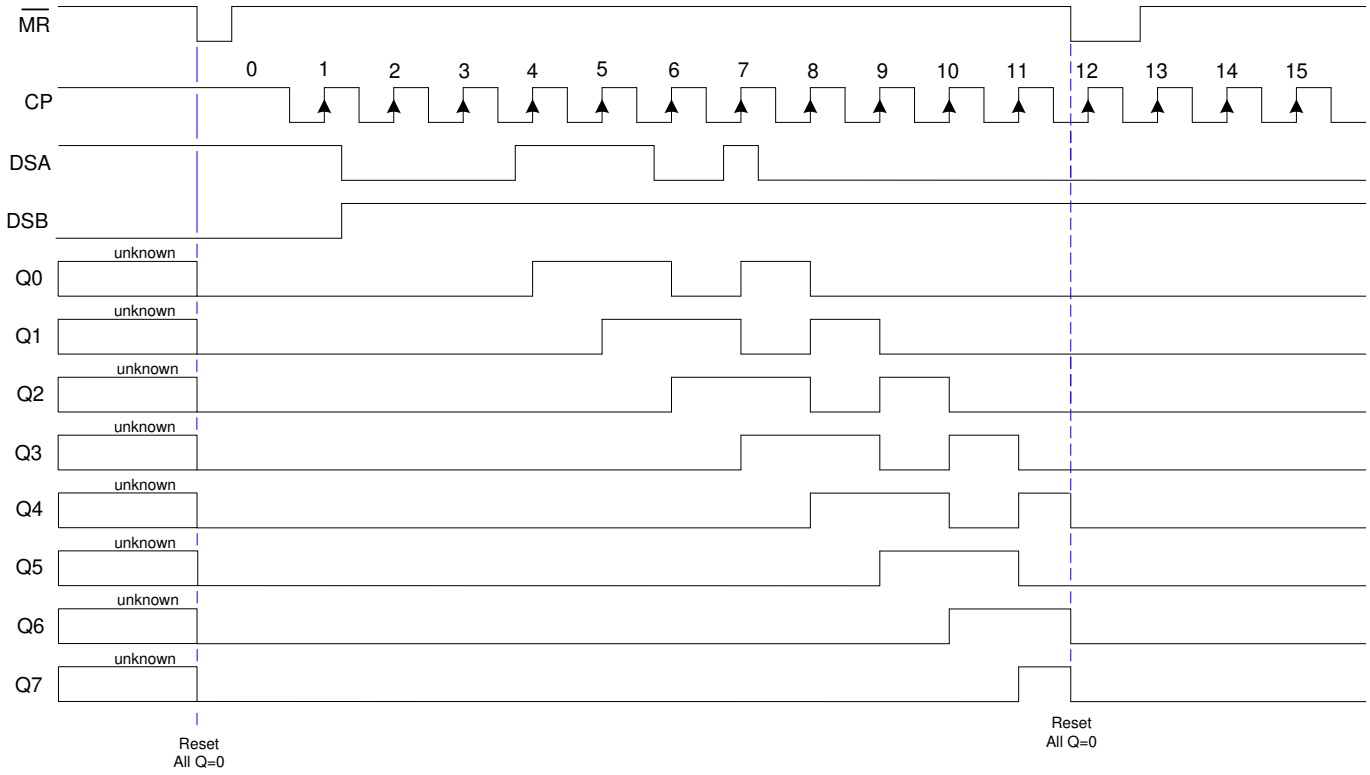
Mode	Input				Output	
	$\overline{MR}$	CP	DSA	DSB	Q0	Q1-Q7
Reset	L	X	X	X	L	L
Shift	H	↑	L	X	L	Qn←Qn-1 (n= 1 to7)
	H	↑	X	L	L	Qn←Qn-1 (n= 1 to7)
	H	↑	H	H	H	Qn←Qn-1 (n= 1 to7)

Note: 4. Signals asserted on DSA and DSB must be in place longer than Tsu (set up time) before CP occurs and remain in place Thold (hold time) after CP.

Logic Diagram



Timing Diagram



Notes: 5. All Q values are reset to LOW when $\overline{MR}$ goes low. $\overline{MR}$ is asynchronous and overrides all other signals.
6. Serial data supplied at DSA and DSB is ANDED and transferred to Q0 on positive edge of CP.

Absolute Maximum Ratings (Note 7) (T_A = +25°C, unless otherwise specified.)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	kV
ESD CDM	Charged Device Model ESD Protection	1	kV
ESD MM	Machine Model ESD Protection	200	V
V_{CC}	Supply Voltage Range	-0.5 to +7.0	V
V_I	Input Voltage Range (Note 8)	-0.5 to +7.0	V
I_{IK}	Input Clamp Current V_I < -0.5V	-20	mA
I_{OK}	Output Clamp Current V_O < -0.5V or V_O > V_{CC} +0.5V	±20	mA
I_O	Continuous Output Current -0.5V < V_O V_{CC} +0.5V	±25	mA
I_{CC}	Continuous Current Through Vcc	75	mA
I_{GND}	Continuous Current Through GND	-75	mA
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_{TOT}	Total Power Dissipation	500	mW

Notes: 7. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.
8. Input Voltage cannot exceed Vcc to the extent the Maximum clamp current is exceeded.

Recommended Operating Conditions (Note 9) (T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	-	2.0	5.5	V
V_I	Input Voltage	-	0	5.5	V
V_O	Output Voltage	-	0	V_{CC}	V
Δt/ΔV	Input Transition Rise or Fall Rate	V_{CC} = 3.0V to 3.6V	-	100	ns/V
		V_{CC} = 4.5V to 5.5V	-	20	
T_A	Operating Free-Air Temperature	-	-40	+125	°C

Note: 9. Unused inputs should be held at V_{CC} or Ground.

Electrical Characteristics (T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	V_{CC}	T_A = +25°C			T_A = -40°C to +85°C		T_A = -40°C to +125°C		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High-Level Input Voltage	-	2.0V	1.5	-	-	1.5	-	1.5	-	V
			3.0V	2.1	-	-	2.1	-	2.1	-	
			5.5V	3.85	-	-	3.85	-	3.85	-	
V_{IL}	Low-Level Input Voltage	-	2.0V	-	-	0.5	-	0.5	-	0.5	V
			3.0V	-	-	0.9	-	0.9	-	0.9	
			5.5V	-	-	1.65	-	1.65	-	1.65	
V_{OH}	High-Level Output Voltage	I_{OH} = -50μA	2.0V	1.9	2.0	-	1.9	-	1.9	-	V
		I_{OH} = -50μA	3.0V	2.9	3.0	-	2.9	-	2.9	-	
		I_{OH} = -50μA	4.5V	4.4	4.5	-	4.4	-	4.4	-	
		I_{OH} = -4.0mA	3.0V	2.58	-	-	2.48	-	2.40	-	
		I_{OH} = -8mA	4.5	3.94	-	-	3.80	-	3.70	-	
V_{OL}	Low-Level Output Voltage	I_{OL} = 50μA	2.0V	-	0	0.1	-	0.1	-	0.1	V
		I_{OL} = 50μA	3.0V	-	0	0.1	-	0.1	-	0.1	
		I_{OL} = 50μA	4.5V	-	0	0.1	-	0.1	-	0.1	
		I_{OL} = 4mA	3.0V	-	0.15	0.36	-	0.44	-	0.55	
		I_{OL} = 8mA	4.5V	-	0.15	0.36	-	0.44	-	0.55	
I_I	Input Current	V_I = GND or 5.5V	0V or 5.5V	-	-	±0.1	-	± 1	-	± 2	μA
I_{CC}	Supply Current	V_I = GND or V_{CC}, I_O = 0A	5.5V	-	-	4.0	-	40	-	80	μA

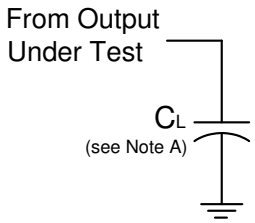
Switching Characteristics

Symbol / Parameter	Pins	Test Conditions Figure 1	V_{CC}	T_A = +25°C			-40°C to +85°C		-40°C to +125°C		Unit
				Min	Typ.	Max	Min	Max	Min	Max	
f_{MAX} Maximum Frequency	CP	C_L = 15pF	3.0V to 3.6V	80	125	-	65	-	50	-	MHz
		C_L = 50pF		50	75	-	45	-	35	-	
		C_L = 15pF	4.5V to 5.0V	125	175	-	105	-	85	-	
		C_L = 50pF		85	115	-	75	-	65	-	
t_W Pulse Width	CP HIGH or LOW	-	3.0V to 3.6V	5.0	-	-	5.0	-	5.0	-	ns
			4.5V to 5.0V	5.0	-	-	5.0	-	5.0	-	
	$\overline{MR}$ LOW	-	3.0V to 3.6V	5.0	-	-	5.0	-	5.0	-	ns
			4.5V to 5.0V	5.0	-	-	5.0	-	5.0	-	
t_{SU} Set-up Time	DSA or DSB to CP	-	3.0V to 3.6V	5.0	-	-	6.0	-	6.0	-	ns
			4.5V to 5.0V	4.5	-	-	4.5	-	4.5	-	
t_H Hold Time	DSA or	-	3.0V to 3.6V	1.5	-	-	1.5	-	1.5	-	ns
			4.5V to 5.0V	2.0	-	-	2.0	-	2.0	-	
t_{rec} RecoveryTime	$\overline{MR}$ to CP	-	3.0V to 3.6V	2.5	-	-	2.5	-	2.5	-	ns
			4.5V to 5.0V	2.5	-	-	2.5	-	2.5	-	
t_{PD} Propagation Delay	CP to Qn	C_L = 15pF	3.0V to 3.6V	-	6.5	12.8	1.0	15.0	1.0	16.0	ns
		C_L = 50pF		-	9.3	16.3	1.0	18.5	1.0	20.5	
		C_L = 15pF	4.5V to 5.0V	-	4.5	9.0	1.0	10.5	1.0	11.5	
		C_L = 50pF		-	6.4	11.0	1.0	12.5	1.0	14.0	
	$\overline{MR}$ to Qn	C_L = 15pF	3.0V to 3.6V	-	5.3	12.8	1.0	15.0	1.0	16.0	ns
		C_L = 50pF		-	7.6	16.3	1.0	18.5	1.0	20.5	
		C_L = 15pF	4.5V to 5.0V	-	4.0	8.6	1.0	10.0	1.0	11.0	
		C_L = 50pF		-	5.8	10.6	1.0	12.0	1.0	13.5	

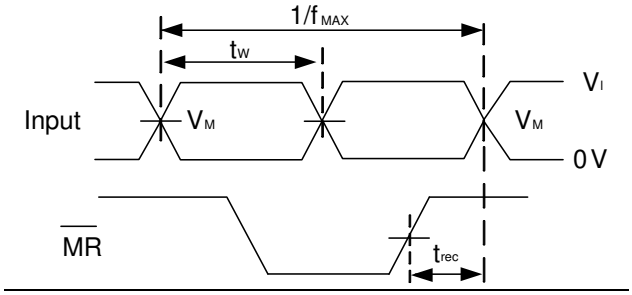
Operating Characteristics (T_A = +25°C, unless otherwise specified.)

Parameter		Test Conditions	V_{CC} = 5.5V		Unit
			Typ	Maximum	
C_{pd}	Power Dissipation Capacitance per Gate	f = 1 MHz	51	-	pF
C_I	Input Capacitance	V_I = V_{CC} or GND	3	10	pF

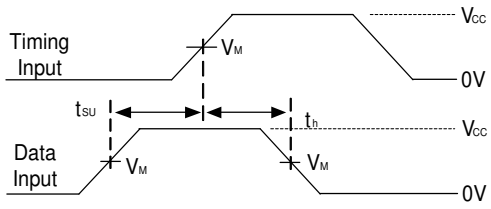
Parameter Measurement Information



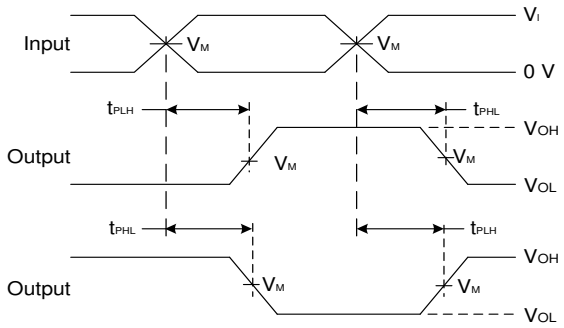
V_{CC}	Inputs		V_M	C_L
	V_I	t_r/t_f		
3.0V-3.6V	V_{CC}	≤3ns	$V_{CC}/2$	15pF,50pF
4.5V-5.5V	V_{CC}	≤3ns	$V_{CC}/2$	15pF,50pF



Voltage Waveform
Pulse Duration and Recovery Time



Voltage Waveform
Set-up and Hold Times

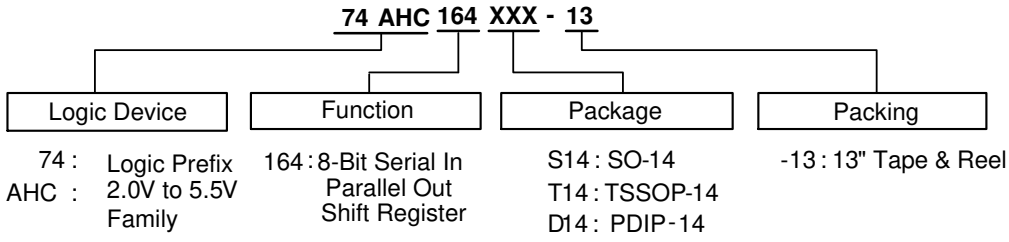


Voltage Waveform
Propagation Delay Times
Inverting and Non Inverting Outputs

Notes: A. Includes test lead and test apparatus capacitance.
B. All pulses are supplied at pulse repetition rate ≤10 MHz.
C. Inputs are measured separately one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{PD}.

Figure 1 Load Circuit and Voltage Waveforms

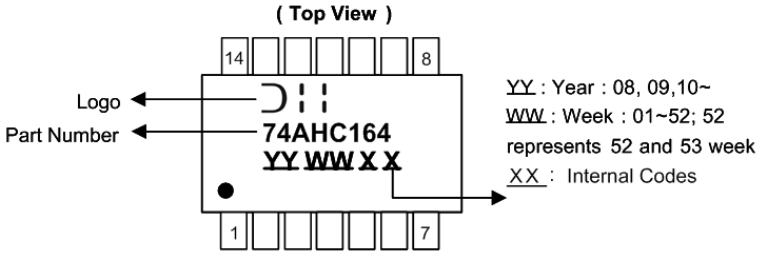
Ordering Information



Device	Package Code	Packaging	Packing	
			Quantity	Part Number Suffix
74AHC164S14-13	S14	SO-14	2,500/Tape & Reel	-13
74AHC164T14-13	T14	TSSOP-14	2,500/Tape & Reel	-13
74AHC164D14	D14	PDIP-14	Tube	

Marking Information

(1) SO-14, TSSOP-14, PDIP-14

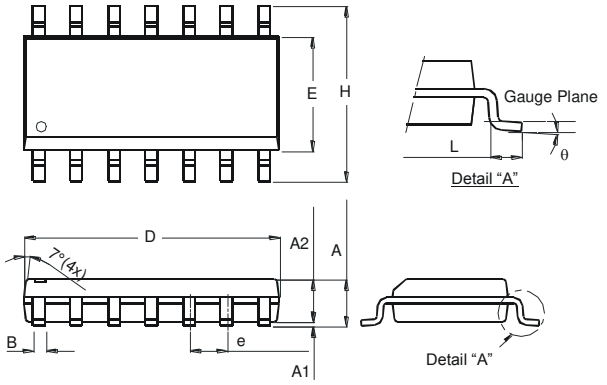


Part Number	Package
74AHC164S14-13	SO-14
74AHC164T14-13	TSSOP-14
74AHC164D14	PDIP-14

Package Outline Dimensions (All dimensions in mm.)

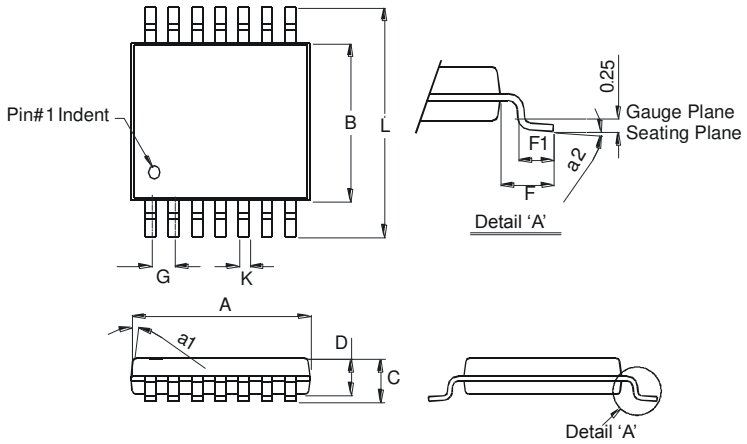
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

Package Type: SO-14



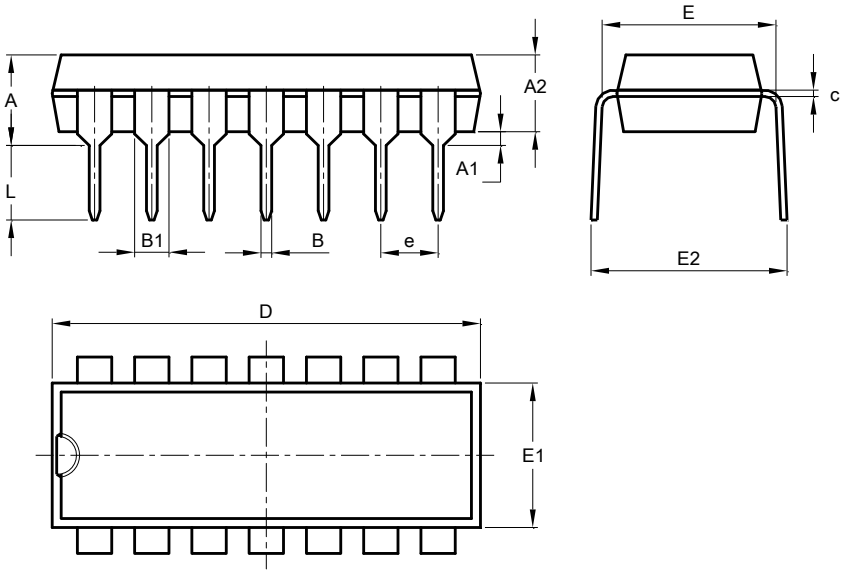
SO-14		
Dim	**Min**	**Max**
A	1.47	1.73
A1	0.10	0.25
A2	1.45 Typ	
B	0.33	0.51
D	8.53	8.74
E	3.80	3.99
e	1.27 Typ	
H	5.80	6.20
L	0.38	1.27
θ	0°	8°
All Dimensions in mm		

Package Type: TSSOP-14



TSSOP-14		
Dim	**Min**	**Max**
a1	7° (4X)	
a2	0°	8°
A	4.9	5.10
B	4.30	4.50
C	—	1.2
D	0.8	1.05
F	1.00 Typ	
F1	0.45	0.75
G	0.65 Typ	
K	0.19	0.30
L	6.40 Typ	
All Dimensions in mm		

Package Type: PDIP-14

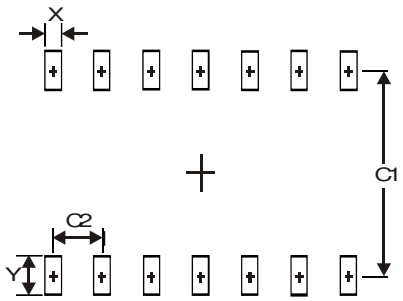


PDIP-14		
Dim	**Min**	**Max**
A	3.710	4.310
A1	0.510	-
A2	3.200	3.600
B	0.380	0.570
B1	1.524 (BSC)	
c	0.204	0.360
D	18.800	19.200
E	6.200	6.600
E1	7.320	7.920
E2	8.400	9.000
e	2.540 (BSC)	
L	3.000	3.600
All Dimensions in mm		

Suggested Pad Layout

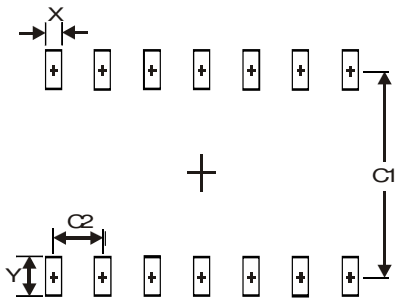
Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

Package Type: SO-14



Dimensions	Value (in mm)
X	0.60
Y	1.50
C1	5.4
C2	1.27

Package Type: TSSOP-14



Dimensions	Value (in mm)
X	0.45
Y	1.45
C1	5.9
C2	0.65

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