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Kind regards,

Team Nexperia

DATA SHEET

74ALVC02
Quad 2-input NOR gate

Product specification
Supersedes data of 2003 Feb 05

2003 Jul 14

Philips
Semiconductors

PHILIPS

Quad 2-input NOR gate 74ALVC02

FEATURES

- Wide supply voltage range from 1.65 to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standard:
  JESD8-7 (1.65 to 1.95 V)
  JESD8-5 (2.3 to 2.7 V)
  JESD8B/JESD36 (2.7 to 3.6 V).
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.

DESCRIPTION

The 74ALVC02 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall times.

The 74ALVC02 provides the 2-input NOR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	V_{CC} = 1.8 V; C_L = 30 pF; R_L = 1 kΩ	2.8	ns
		V_{CC} = 2.5 V; C_L = 30 pF; R_L = 500 Ω	2.0	ns
		V_{CC} = 2.7 V; C_L = 50 pF; R_L = 500 Ω	2.5	ns
		V_{CC} = 3.3 V; C_L = 50 pF; R_L = 500 Ω	2.2	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	V_{CC} = 3.3 V; notes 1 and 2	32	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74ALVC02D	−40 to +85 °C	14	SO14	plastic	SOT108-1
74ALVC02PW	−40 to +85 °C	14	TSSOP14	plastic	SOT402-1
74ALVC02BQ	−40 to +85 °C	14	DHVQFN14	plastic	SOT762-1

FUNCTION TABLE

See note 1.

INPUT		OUTPUT
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level

PINNING

Pin	SYMBOL	DESCRIPTION
1	1Y	data output
2	1A	data input
3	1B	data input
4	2Y	data output
5	2A	data input
6	2B	data input
7	GND	ground (0 V)
8	3A	data input
9	3B	data input
10	3Y	data output
11	4A	data input
12	4B	data input
13	4Y	data output
14	V_{CC}	supply voltage

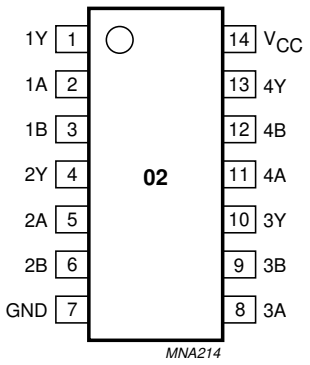
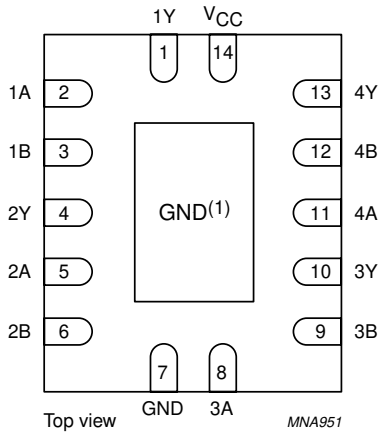


Fig.1 Pin configuration SO14 and TSSOP14.



(1) (1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN14.

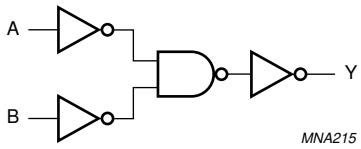


Fig.3 Logic diagram (one gate).

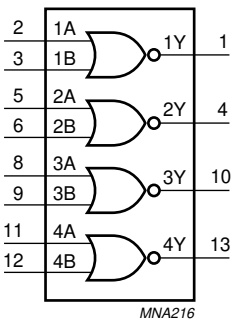


Fig.4 Function diagram.

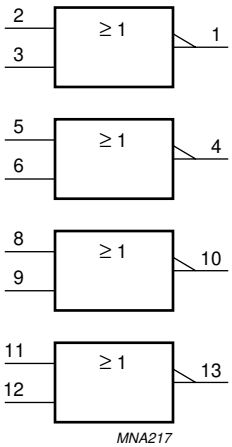


Fig.5 IEC logic symbol.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	V_{CC} = 1.65 to 3.6 V	0	V_{CC}	V
		V_{CC} = 0 V; Power-down mode	0	4.6	V
T_{amb}	operating ambient temperature		–40	+85	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.65 to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+4.6	V
I_{IK}	input diode current	$V_I < 0$	–	–50	mA
V_I	input voltage		–0.5	+4.6	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	output voltage	notes 1 and 2	–0.5	V_{CC} + 0.5	V
		Power-down mode; note 2	–0.5	+4.6	V
I_O	output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 to +85 °C; note 3	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When V_{CC} = 0 V (Power-down mode), the output voltage can be 3.6 V in normal operation.
3. For SO14 packages: above 70 °C derate linearly with 8 mW/K.
   For TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.
   For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C							
V_{IH}	HIGH-level input voltage		1.65 to 1.95	0.65 × V_{CC}	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2	–	–	V
V_{IL}	LOW-level input voltage		1.65 to 1.95	–	–	0.35 × V_{CC}	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA	1.65 to 3.6	–	–	0.2	V
		I_O = 6 mA	1.65	–	0.11	0.3	V
		I_O = 12 mA	2.3	–	0.17	0.4	V
		I_O = 18 mA	2.3	–	0.25	0.6	V
		I_O = 12 mA	2.7	–	0.16	0.4	V
		I_O = 18 mA	3.0	–	0.23	0.4	V
		I_O = 24 mA	3.0	–	0.30	0.55	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 μA	1.65 to 3.6	V_{CC} − 0.2	–	–	V
		I_O = −6 mA	1.65	1.25	1.51	–	V
		I_O = −12 mA	2.3	1.8	2.10	–	V
		I_O = −18 mA	2.3	1.7	2.01	–	V
		I_O = −12 mA	2.7	2.2	2.53	–	V
		I_O = −18 mA	3.0	2.4	2.76	–	V
		I_O = −24 mA	3.0	2.2	2.68	–	V
I_{LI}	input leakage current	V_I = 3.6 V or GND	3.6	–	±0.1	±5	μA
I_{off}	power OFF leakage current	V_I or V_O = 3.6 V	0.0	–	±0.1	±10	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	3.6	–	0.2	20	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} − 0.6 V; I_O = 0	3.0 to 3.6	–	5	750	μA

Note

1. All typical values are measured at T_{amb} = 25 °C.

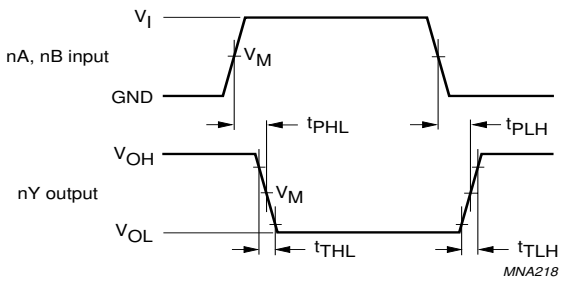
AC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to +85 °C							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 6 and 7	1.65 to 1.95	1.0	2.8	4.7	ns
			2.3 to 2.7	1.0	2.0	3.1	ns
			2.7	1.0	2.5	2.9	ns
			3.0 to 3.6	1.0	2.2	2.8	ns

Note

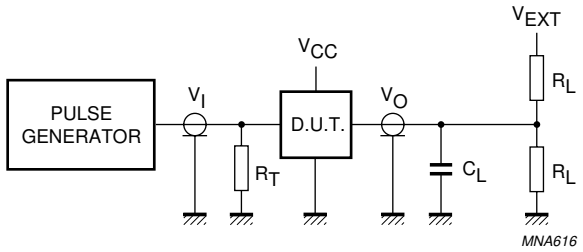
1. All typical values are measured at T_{amb} = 25 °C.

AC WAVEFORMS



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 to 1.95 V	0.5 × V_{CC}	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	0.5 × V_{CC}	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

Fig.6 Inputs nA, nB to output nY propagation delay times.



V_{CC}	V_I	C_L	R_L	V_{EXT}		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.65 to 1.95 V	V_{CC}	30 pF	1 kΩ	open	GND	$2 \times V_{CC}$
2.3 to 2.7 V	V_{CC}	30 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V

Definitions for test circuit:

R_L = Load resistor.

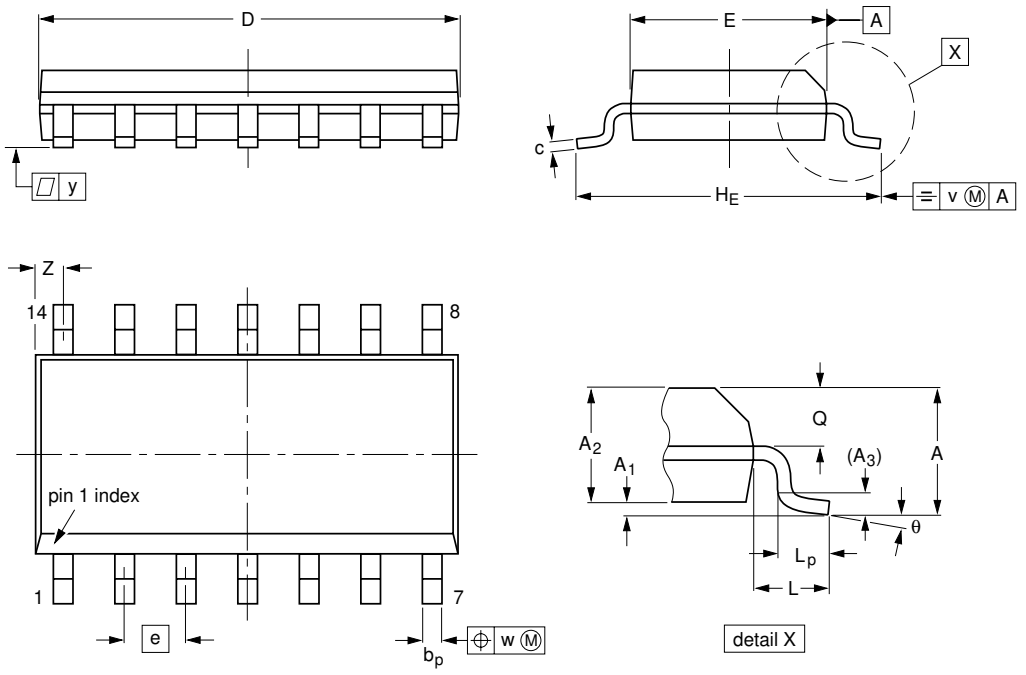
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

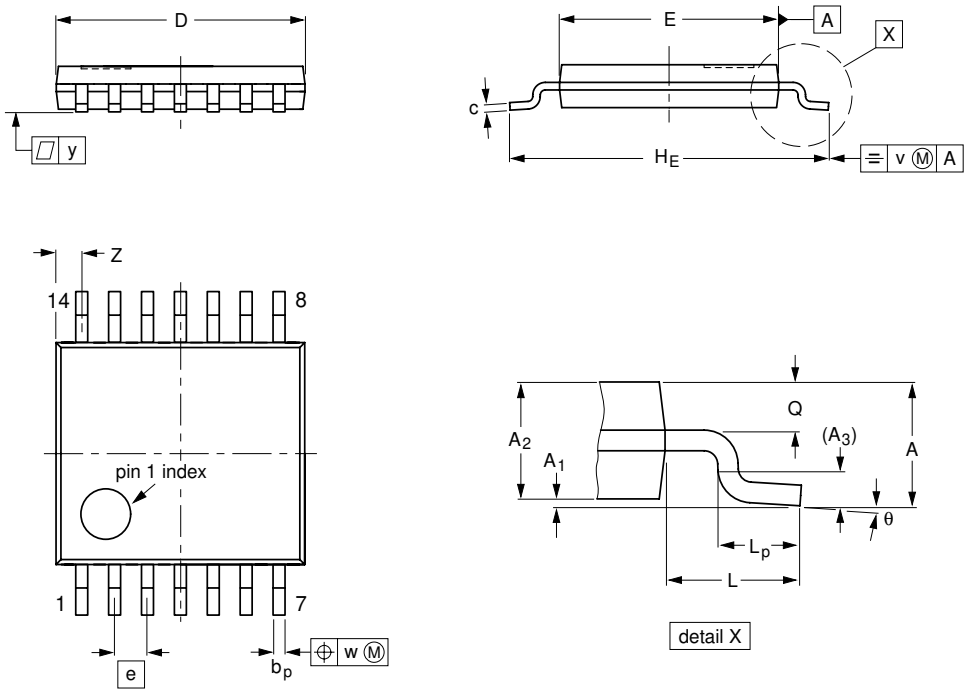
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

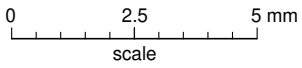
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**





DIMENSIONS (mm are the original dimensions)

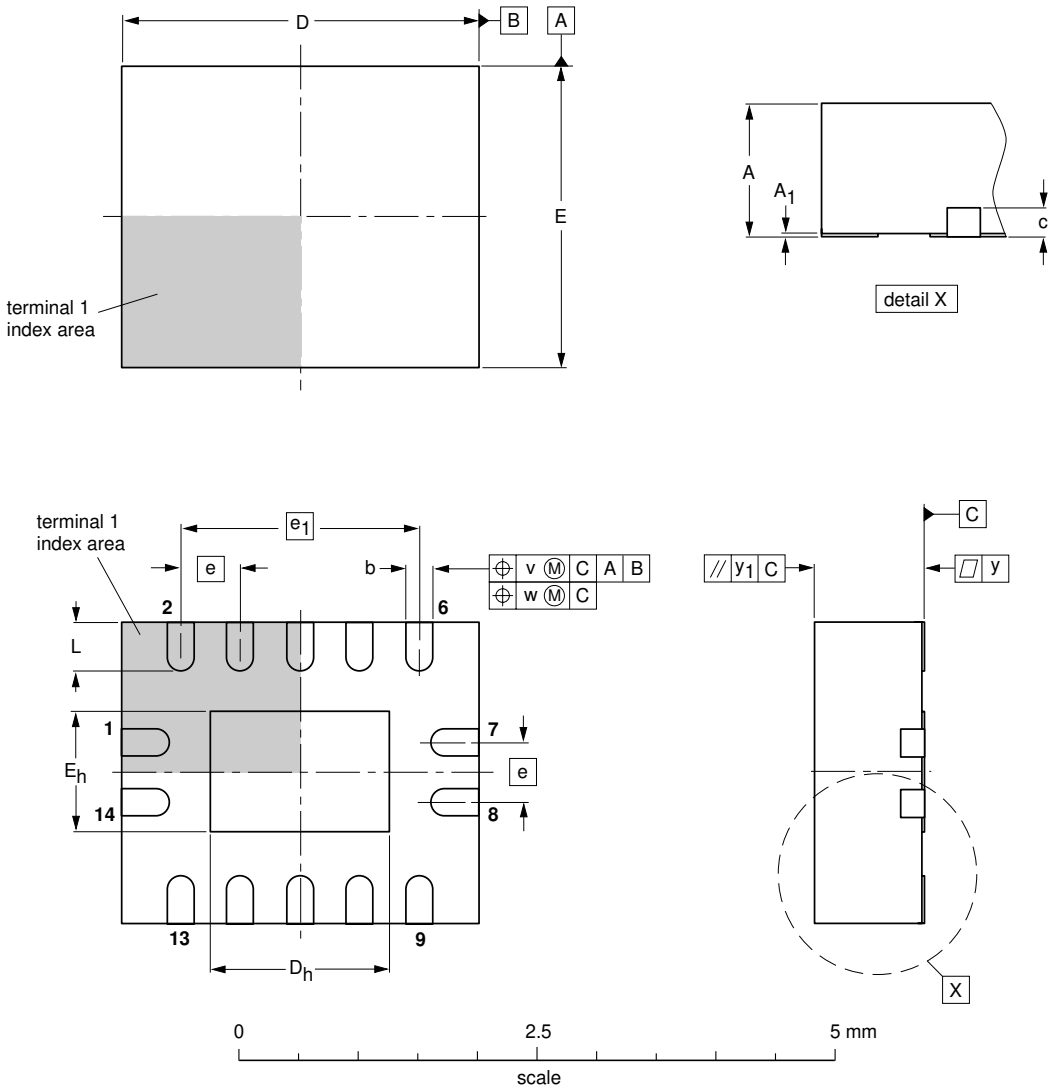
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

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LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Printed in The Netherlands 613508/02/pp13 Date of release: 2003 Jul 14 Document order number: 9397 750 11272

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