



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: [info@chipsmall.com](mailto:info@chipsmall.com) Web: [www.chipsmall.com](http://www.chipsmall.com)

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

### **Important notice**

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <http://www.nxp.com>, <http://www.philips.com> or <http://www.semiconductors.philips.com> , use <http://www.nexperia.com>

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com) (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © **Nexperia B.V. (year). All rights reserved.**

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

# DATA SHEET

**74ALVC16244; 74ALVCH16244**  
2.5 V/3.3 V 16-bit buffer/line driver  
(3-state)

Product specification  
Supersedes data of 1998 Jun 29

2003 May 14

## 2.5 V/3.3 V 16-bit buffer/line driver (3-state)

**74ALVC16244;  
74ALVCH16244**

### FEATURES

- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- MultiByte flow-through standard pin-out architecture
- Low inductance multiple  $V_{CC}$  and GND pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bus hold on data inputs (74ALVCH16244 only)
- Output drive capability 50  $\Omega$  transmission lines at 85 °C
- Current drive  $\pm 24$  mA at 3.0 V
- Complies with JEDEC standard no. 8-1 A
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.

### DESCRIPTION

The 74ALVC16244; 74ALVCH16244 is a 16-bit non-inverting buffer/line driver with 3-state outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The 3-state outputs are controlled by the output enable inputs  $1\bar{OE}$ ,  $2\bar{OE}$ ,  $3\bar{OE}$  and  $4\bar{OE}$ . A HIGH on  $n\bar{OE}$  causes the outputs to assume a high-impedance OFF-state.

The 74ALVCH16244 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

The 74ALVC16244 has 5 V tolerant inputs.

### QUICK REFERENCE DATA

$GND = 0$  V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETERS	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay $nAn$ to $nYn$	$V_{CC} = 2.5$ V; $C_L = 30$ pF	1.9	ns
		$V_{CC} = 3.3$ V; $C_L = 50$ pF	1.9	ns
$C_I$	input capacitance		5.0	pF
$C_{PD}$	power dissipation capacitance per buffer	notes 1 and 2 outputs enabled outputs disabled	25 4	pF pF

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$$\sum(C_L \times V_{CC}^2 \times f_o) = \text{sum of the outputs.}$$

2. The condition is  $V_I = GND$  to  $V_{CC}$ .

2.5 V/3.3 V 16-bit buffer/line driver  
(3-state)

74ALVC16244;  
74ALVCH16244

## FUNCTION TABLE

See note 1

INPUT		OUTPUT
$n\bar{O}E$	$nA_n$	$nY_n$
L	L	L
L	H	H
H	X	Z

### Note

1. H = HIGH voltage level;
- L = LOW voltage level;
- X = don't care;
- Z = high-impedance OFF-state.

## ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74ALVC16244DL	–40 °C to +85 °C	48	SSOP48	plastic	SOT370-1
74ALVCH16244DL	–40 °C to +85 °C	48	SSOP48	plastic	SOT370-1
74ALVC16244DGG	–40 °C to +85 °C	48	TSSOP48	plastic	SOT362-1
74ALVCH16244DGG	–40 °C to +85 °C	48	TSSOP48	plastic	SOT362-1

2.5 V/3.3 V 16-bit buffer/line driver  
(3-state)

74ALVC16244;  
74ALVCH16244

### PINNING

PIN	SYMBOL	DESCRIPTION
1	1 $\bar{OE}$	output enable input (active LOW)
2	1Y0	data output
3	1Y1	data output
4	GND	ground (0 V)
5	1Y2	data output
6	1Y3	data output
7	V <sub>CC</sub>	supply voltage
8	2Y0	data output
9	2Y1	data output
10	GND	ground (0 V)
11	2Y2	data output
12	2Y3	data output
13	3Y0	data output
14	3Y1	data output
15	GND	ground (0 V)
16	3Y2	data output
17	3Y3	data output
18	V <sub>CC</sub>	supply voltage
19	4Y0	data output
20	4Y1	data output
21	GND	ground (0 V)
22	4Y2	data output
23	4Y3	data output
24	4 $\bar{OE}$	output enable input (active LOW)

PIN	SYMBOL	DESCRIPTION
25	3 $\bar{OE}$	output enable input (active LOW)
26	4A3	data input
27	4A2	data input
28	GND	ground (0 V)
29	4A1	data input
30	4A0	data input
31	V <sub>CC</sub>	supply voltage
32	3A3	data input
33	3A2	data input
34	GND	ground (0 V)
35	3A1	data input
36	3A0	data input
37	2A3	data input
38	2A2	data input
39	GND	ground (0 V)
40	2A1	data input
41	2A0	data input
42	V <sub>CC</sub>	supply voltage
43	1A3	data input
44	1A2	data input
45	GND	ground (0 V)
46	1A1	data input
47	1A0	data input
48	2 $\bar{OE}$	output enable input (active LOW)

**2.5 V/3.3 V 16-bit buffer/line driver  
(3-state)**

**74ALVC16244;  
74ALVCH16244**

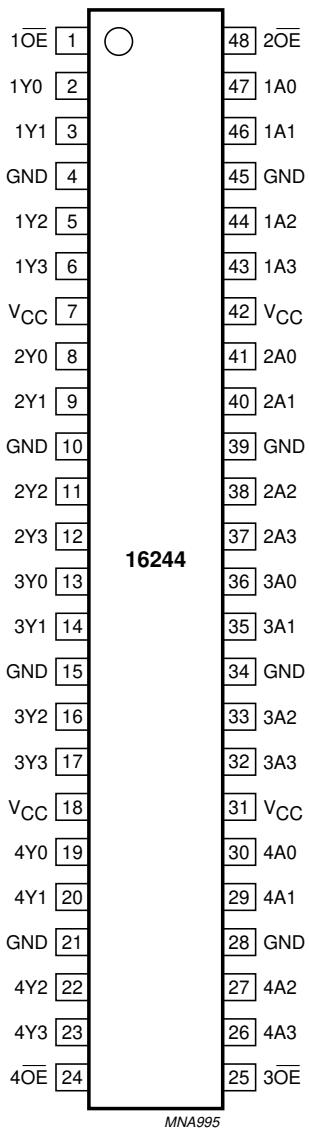


Fig.1 Pin configuration.

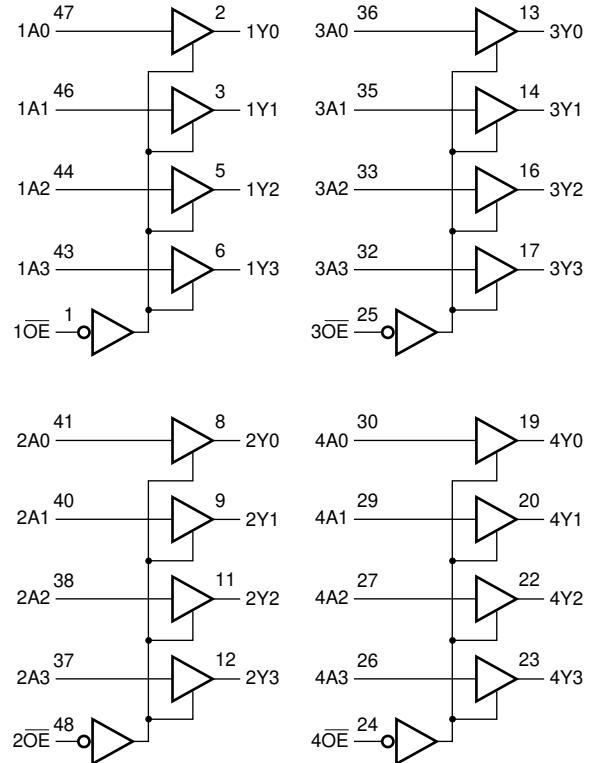


Fig.2 Logic symbol.

**2.5 V/3.3 V 16-bit buffer/line driver  
(3-state)**

**74ALVC16244;  
74ALVCH16244**

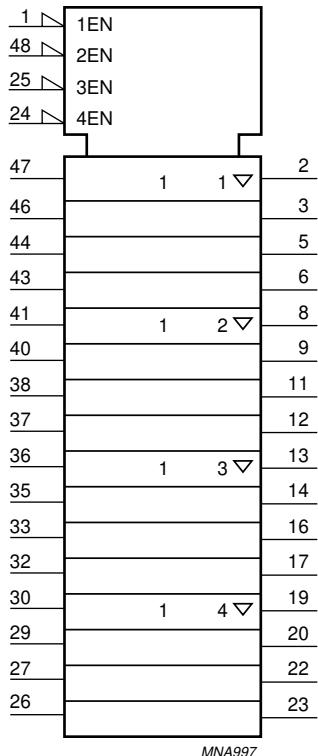


Fig.3 Logic symbol (IEEC/IEC).

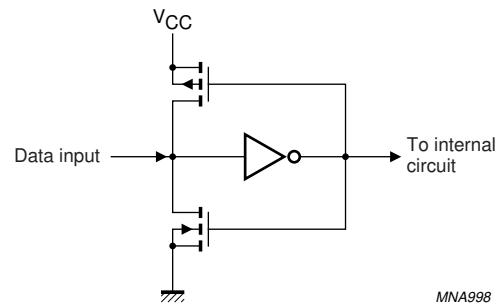


Fig.4 Bus hold circuit.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage	maximum speed performance			
		$V_{CC} = 2.5 \text{ V}; C_L = 30 \text{ pF}$	2.3	2.7	V
		$V_{CC} = 3.3 \text{ V}; C_L = 50 \text{ pF}$	3.0	3.6	V
$V_I$	input voltage	low-voltage applications	1.2	3.6	V
		for pins $nAn$ with bus hold	0	$V_{CC}$	V
		for pins $nAn$ without bus hold	0	5.5	V
$V_O$	output voltage	for pins $n\bar{OE}$	0	5.5	V
			0	$V_{CC}$	V
			-40	+85	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 2.3 \text{ to } 3.0 \text{ V}$	0	20	ns/V
		$V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$	0	10	ns/V

2.5 V/3.3 V 16-bit buffer/line driver  
(3-state)

74ALVC16244;  
74ALVCH16244

### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		-0.5	+4.6	V
$I_{IK}$	input diode current	$V_I < 0$	-	-50	mA
$V_I$	input voltage	for data inputs with bus hold; note 1	-0.5	$V_{CC} + 0.5$	V
		for data inputs without bus hold; note 1	-0.5	+5.5	V
		for control pins; note 1	-0.5	+5.5	V
$I_{OK}$	output diode current	$V_O > V_{CC}$ or $V_O < 0$	-	$\pm 50$	mA
$V_O$	output voltage	note 1	-0.5	$V_{CC} + 0.5$	V
$I_O$	output source or sink current	$V_O = 0$ to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		-	$\pm 100$	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40$ to $+85$ °C; note 2			
		SSOP48 package	-	850	mW
		TSSOP48 package	-	600	mW

### Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SSOP48 packages: above 55 °C the value of  $P_{tot}$  derates linearly with 11.3 mW/K.  
For TSSOP48 packages: above 55 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.

2.5 V/3.3 V 16-bit buffer/line driver  
(3-state)74ALVC16244;  
74ALVCH16244

## DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2 1.8 2.3 to 2.7 2.7 to 3.6	V <sub>CC</sub> 0.7 × V <sub>CC</sub> 1.7 2.0	— 0.9 1.2 1.5	— — — —	V V V V
V <sub>IL</sub>	LOW-level input voltage		1.2 1.8 2.3 to 2.7 2.7 to 3.6	— — — —	— 0.9 1.2 1.5	GND 0.2 × V <sub>CC</sub> 0.7 0.8	V V V V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 µA I <sub>O</sub> = -6 mA I <sub>O</sub> = -6 mA I <sub>O</sub> = -12 mA I <sub>O</sub> = -18 mA I <sub>O</sub> = -12 mA I <sub>O</sub> = -24 mA	1.8 to 3.6	V <sub>CC</sub> - 0.2 V <sub>CC</sub> - 0.4 V <sub>CC</sub> - 0.3 V <sub>CC</sub> - 0.5 V <sub>CC</sub> - 0.6 V <sub>CC</sub> - 0.5 V <sub>CC</sub> - 1.0	V <sub>CC</sub> V <sub>CC</sub> - 0.10 V <sub>CC</sub> - 0.08 V <sub>CC</sub> - 0.17 V <sub>CC</sub> - 0.26 V <sub>CC</sub> - 0.14 V <sub>CC</sub> - 0.28	— — — — — — —	V V V V V V V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 µA I <sub>O</sub> = 6 mA I <sub>O</sub> = 6 mA I <sub>O</sub> = 12 mA I <sub>O</sub> = 18 mA I <sub>O</sub> = 12 mA I <sub>O</sub> = 24 mA	1.8 to 3.6	—	GND	0.20 0.30 0.20 0.40 0.60 0.40 0.55	V V V V V V V
I <sub>LI</sub>	input leakage current	data pin with bus hold; V <sub>I</sub> = V <sub>CC</sub> or GND	1.8 to 3.6	—	0.1	5	µA
		data pin without bus hold; V <sub>I</sub> = 5.5 V or GND	1.8 to 3.6	—	0.1	5	µA
		control pin; V <sub>I</sub> = 5.5 V or GND	1.8 to 3.6	—	0.1	5	µA
I <sub>IHZ</sub> , I <sub>ILZ</sub>	3-state input current for common I/O pins	V <sub>I</sub> = V <sub>CC</sub> or GND	1.8 to 2.7	—	0.1	10	µA
			3.6	—	0.1	15	µA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	1.8 to 2.7	—	0.1	5	µA
			3.6	—	0.1	10	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	1.8 to 2.7	—	0.1	20	µA
			2.3 to 3.6	—	0.2	40	µA

2.5 V/3.3 V 16-bit buffer/line driver  
(3-state)74ALVC16244;  
74ALVCH16244

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
ΔI <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> – 0.6 V; I <sub>O</sub> = 0 data pin with bus hold data pin without bus hold control pin	2.7 to 3.6 2.7 to 3.6 2.7 to 3.6	– – –	150 5 5	750 500 500	μA μA μA
I <sub>BHL</sub>	bus hold LOW sustaining current	V <sub>I</sub> = 0.7 V; note 2 V <sub>I</sub> = 0.8 V; note 2	2.3 3.0	45 75	– 150	– –	μA μA
I <sub>BHH</sub>	bus hold HIGH sustaining current	V <sub>I</sub> = 1.7 V; note 2 V <sub>I</sub> = 2.0 V; note 2	2.3 3.0	–45 –75	– –175	– –	μA μA
I <sub>BHLO</sub>	bus hold LOW overdrive current	note 2	2.7 3.6	300 450	– –	– –	μA μA
I <sub>BHHO</sub>	bus hold HIGH overdrive current		2.7 3.6	–300 –450	– –	– –	μA μA

## Notes

1. All typical values are measured at T<sub>amb</sub> = 25 °C.
2. Valid for data inputs of bus hold parts.

2.5 V/3.3 V 16-bit buffer/line driver  
(3-state)74ALVC16244;  
74ALVCH16244

## AC CHARACTERISTICS

 $V_{CC} = 0 \text{ V}$ ;  $t_r = t_f \leq 2.0 \text{ ns}$  and  $C_L = 30 \text{ pF}$  for  $V_{CC} < 2.7 \text{ V}$ ;  $t_r = t_f \leq 2.5 \text{ ns}$  and  $C_L = 50 \text{ pF}$  for  $V_{CC} \geq 2.7 \text{ V}$ .

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	$V_{CC} (\text{V})$				
$T_{amb} = -40 \text{ to } +85 \text{ }^{\circ}\text{C}$ ; note 1							
$t_{PHL}/t_{PLH}$	propagation delay nAn to nYn	see Figs 5 and 7	1.2	—	5.8	—	ns
			1.8	1.5	2.8	5.1	ns
			2.3 to 2.7	1.0	1.9	3.7	ns
			2.7	1.0	2.1	3.6	ns
			3.0 to 3.6	1.0	1.9	3.0	ns
$t_{PZH}/t_{PLZ}$	3-state output enable time nOE to nYn	see Figs 6 and 7	1.2	—	8.4	—	ns
			1.8	1.5	3.8	7.1	ns
			2.3 to 2.7	1.0	2.5	4.9	ns
			2.7	1.0	2.9	4.9	ns
			3.0 to 3.6	1.0	2.3	4.0	ns
$t_{PHZ}/t_{PLZ}$	3-state output disable time nOE to nYn	see Figs 6 and 7	1.2	—	5.9	—	ns
			1.8	1.5	3.1	5.4	ns
			2.3 to 2.7	1.0	2.1	4.1	ns
			2.7	1.0	3.0	4.5	ns
			3.0 to 3.6	1.0	2.7	4.1	ns

## Note

1. All typical values are measured at  $T_{amb} = 25 \text{ }^{\circ}\text{C}$ .Typical values for  $V_{CC} = 2.3 \text{ to } 2.7 \text{ V}$  are measured at  $V_{CC} = 2.5 \text{ V}$ .Typical values for  $V_{CC} = 3.3 \text{ to } 3.6 \text{ V}$  are measured at  $V_{CC} = 3.3 \text{ V}$ .

## AC WAVEFORMS

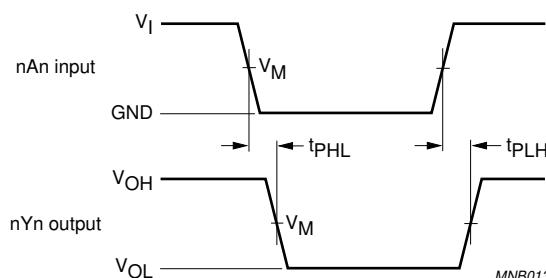
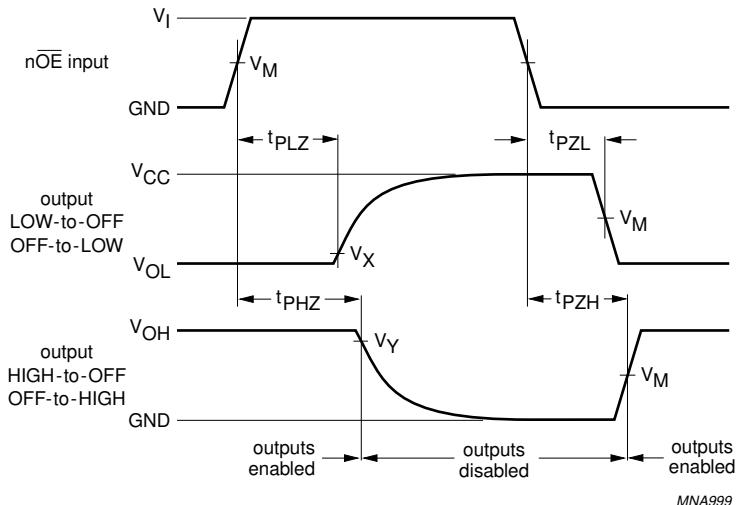
 $V_M = 0.5V_{CC}$  at  $V_{CC} < 2.7 \text{ V}$  and  $V_M = 1.5 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$ . $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

Fig.5 Input (nAn) to output (nYn) propagation delays.

## 2.5 V/3.3 V 16-bit buffer/line driver (3-state)

74ALVC16244;  
74ALVCH16244



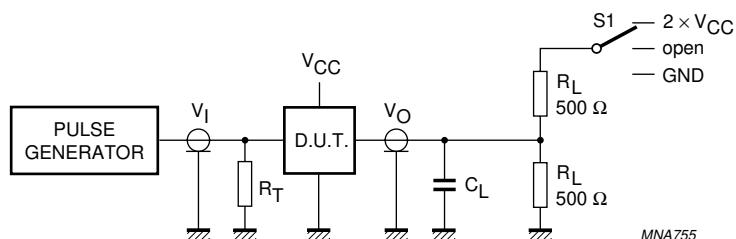
$$V_M = 0.5V_{CC} \text{ at } V_{CC} < 2.7 \text{ V and } V_M = 1.5 \text{ V at } V_{CC} \geq 2.7 \text{ V.}$$

$$V_X = V_{OL} + 0.15 \text{ V at } V_{CC} < 2.7 \text{ V and } V_X = V_{OL} + 0.3 \text{ V at } V_{CC} \geq 2.7 \text{ V.}$$

$$V_Y = V_{OH} - 0.15 \text{ V at } V_{CC} < 2.7 \text{ V and } V_Y = V_{OH} - 0.3 \text{ V at } V_{CC} \geq 2.7 \text{ V.}$$

$V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

Fig.6 3-state enable and disable times.



TEST	S1
$t_{PLH}/t_{PHL}$	open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$V_I$
<2.7 V	$V_{CC}$
2.7 to 3.6 V	2.7 V

Definitions for test circuit:

$R_L$  = Load resistor.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to  $Z_o$  of the pulse generator.

Fig.7 Load circuitry for switching times.

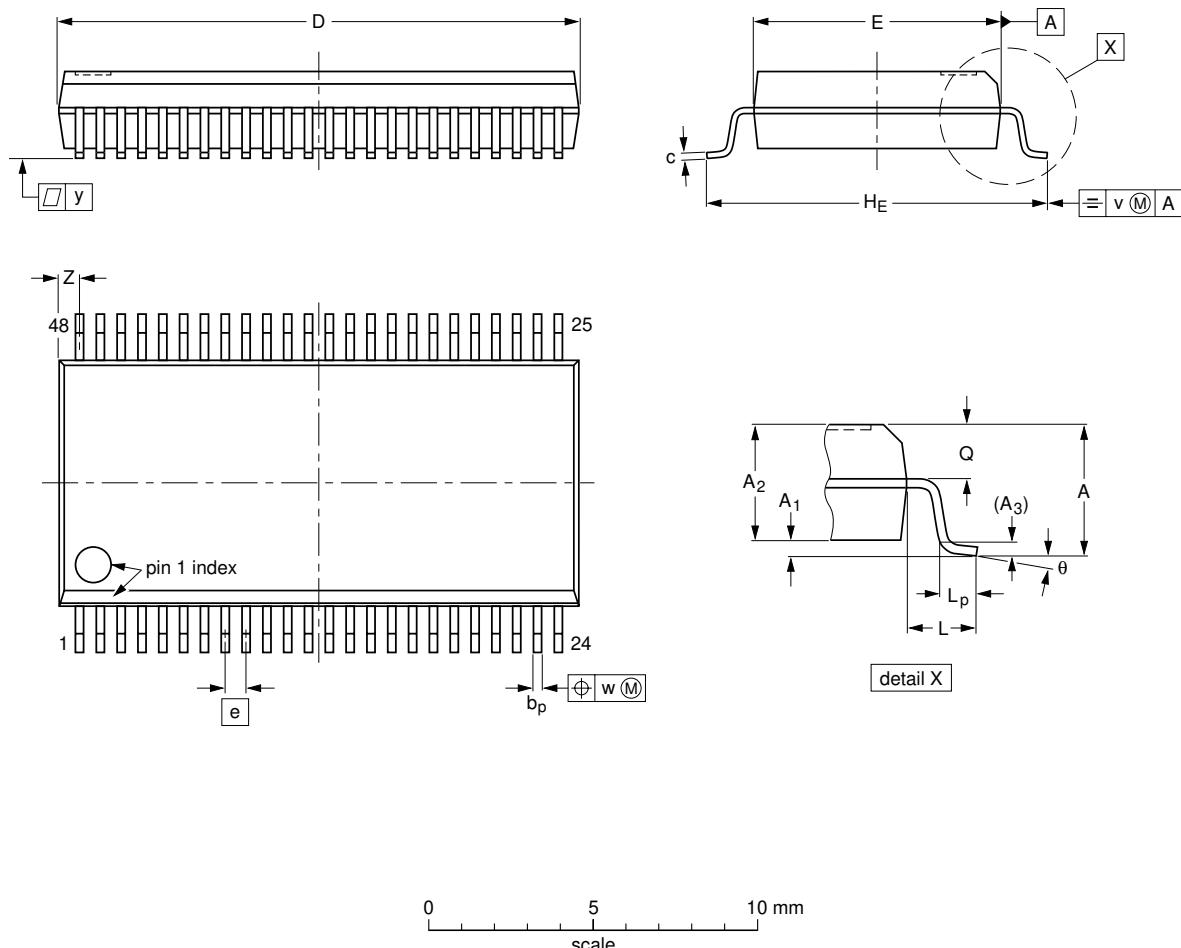
## 2.5 V/3.3 V 16-bit buffer/line driver (3-state)

74ALVC16244;  
74ALVCH16244

## PACKAGE OUTLINES

**SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm**

SOT370-1



**DIMENSIONS (mm are the original dimensions)**

DIMENSIONS (mm are the original dimensions)																		
UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.8 0.2	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

## Note

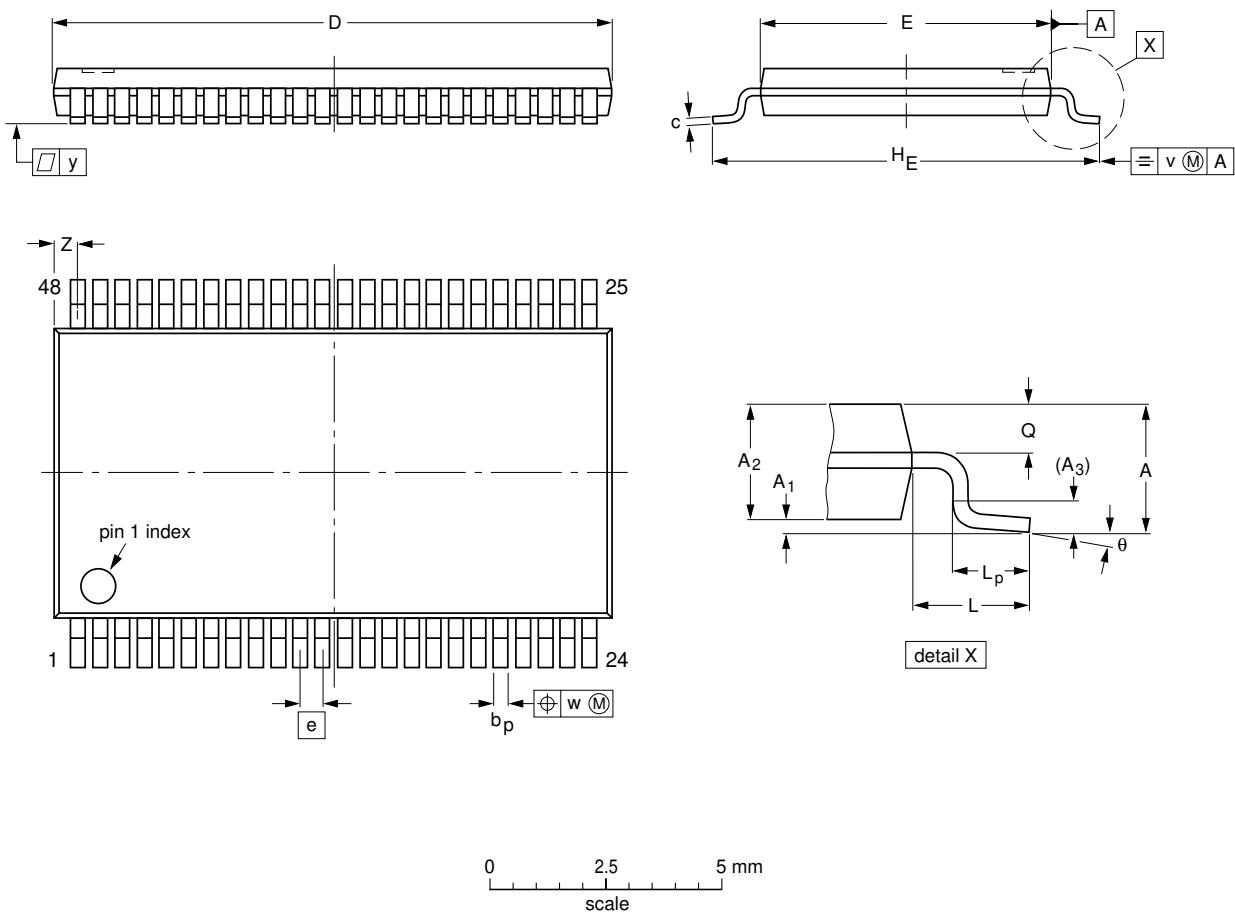
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				99-12-27 03-02-19

2.5 V/3.3 V 16-bit buffer/line driver  
(3-state)74ALVC16244;  
74ALVCH16244

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



## DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z	θ
mm	1.2 0.05	0.15 0.85	1.05	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

## Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				-99-12-27 03-02-19

## 2.5 V/3.3 V 16-bit buffer/line driver (3-state)

74ALVC16244;  
74ALVCH16244

### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all the BGA packages
  - for packages with a thickness  $\geq$  2.5 mm
  - for packages with a thickness  $<$  2.5 mm and a volume  $\geq$  350 mm<sup>3</sup> so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness  $<$  2.5 mm and a volume  $<$  350 mm<sup>3</sup> so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

2.5 V/3.3 V 16-bit buffer/line driver  
(3-state)

74ALVC16244;  
74ALVCH16244

### Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE <sup>(1)</sup>	SOLDERING METHOD	
	WAVE	REFLOW <sup>(2)</sup>
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable not suitable <sup>(3)</sup>	suitable suitable
PLCC <sup>(4)</sup> , SO, SOJ LQFP, QFP, TQFP	suitable not recommended <sup>(4)(5)</sup>	suitable suitable
SSOP, TSSOP, VSO, VSSOP	not recommended <sup>(6)</sup>	suitable

### Notes

1. For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

2.5 V/3.3 V 16-bit buffer/line driver  
(3-state)

74ALVC16244;  
74ALVCH16244

## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

### Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## DEFINITIONS

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## DISCLAIMERS

**Life support applications** — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes** — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

---

2.5 V/3.3 V 16-bit buffer/line driver  
(3-state)

74ALVC16244;  
74ALVCH16244

---

**NOTES**

---

2.5 V/3.3 V 16-bit buffer/line driver  
(3-state)

74ALVC16244;  
74ALVCH16244

---

**NOTES**

---

2.5 V/3.3 V 16-bit buffer/line driver  
(3-state)

74ALVC16244;  
74ALVCH16244

---

**NOTES**

# **Philips Semiconductors – a worldwide company**

## **Contact information**

For additional information please visit <http://www.semiconductors.philips.com>. Fax: +31 40 27 24825  
For sales offices addresses send e-mail to: [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com).

© Koninklijke Philips Electronics N.V. 2003

SCA75

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

613508/03/0020

Date of release: 2003 May 14

Document order number: 9397 750 10793

*Let's make things better.*

**Philips  
Semiconductors**



**PHILIPS**