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# DATA SHEET

## 74ALVCH16500
## 18-bit universal bus transceiver (3-State)

Product specification
Supersedes data of 1998 Aug 31
IC24 Data Handbook

1998 Sep 24

Philips
Semiconductors

PHILIPS

# 18-bit universal bus transceiver (3-State) 74ALVCH16500

## FEATURES

- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- All inputs have bushold circuitry
- Output drive capability 50Ω transmission lines @ 85°C
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple $V_{CC}$ and ground pins for minimum noise and ground bounce

## DESCRIPTION

The 74ALVCH16500 is a high-performance CMOS product. This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ($OE_{AB}$ and $\overline{OE}_{BA}$), latch enable ($LE_{AB}$ and $LE_{BA}$), and clock ($\overline{CP}_{AB}$ and $\overline{CP}_{BA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when $LE_{AB}$ is High. When $LE_{AB}$ is Low, the A data is latched if $\overline{CP}_{AB}$ is held at a High or Low logic level. If $LE_{AB}$ is Low, the A-bus data is stored in the latch/flip-flop on the High-to-Low transition of $\overline{CP}_{AB}$. When $OE_{AB}$ is High, the outputs are active. When $OE_{AB}$ is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OE}_{BA}$, $LE_{BA}$ and $\overline{CP}_{BA}$. The output enables are complimentary ($OE_{AB}$ is active High, and $\overline{OE}_{BA}$ is active Low).

To ensure the high impedance state during power up or power down, $\overline{OE}_{BA}$ should be tied to $V_{CC}$ through a pullup resistor and $OE_{AB}$ should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

## QUICK REFERENCE DATA

GND = 0V; $T_{amb}$ = 25°C; $t_r = t_f$ = 2.5ns

| SYMBOL | PARAMETER | CONDITIONS | | TYPICAL | UNIT |
|---|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation delay<br>An, Bn to Bn, An | $V_{CC}$ = 2.5V, $C_L$ = 30pF<br>$V_{CC}$ = 3.3V, $C_L$ = 50pF | | 3.1<br>2.9 | ns |
| $C_{I/O}$ | Input/output capacitance | | | 8.0 | pF |
| $C_I$ | Input capacitance | | | 4.0 | pF |
| $C_{PD}$ | Power dissipation capacitance per latch | $V_I$ = GND to $V_{CC}$[1] | Outputs enabled | 21 | pF |
| | | | Outputs disabled | 3 | |

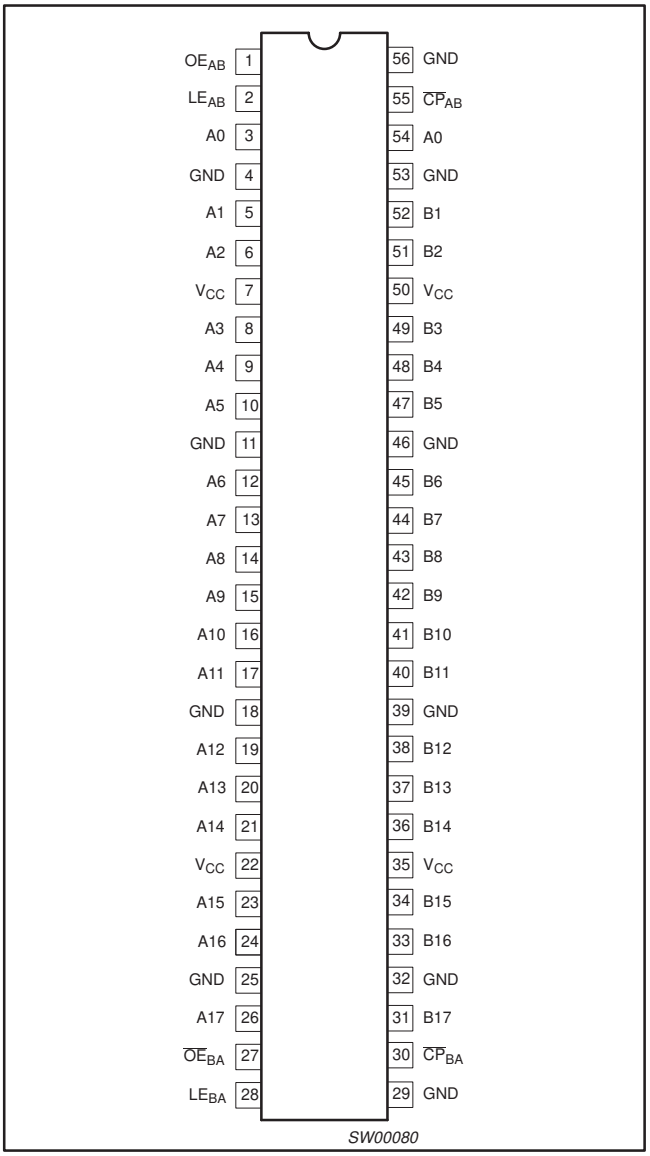
**NOTES:**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: $f_i$ = input frequency in MHz; $C_L$ = output load capacitance in pF; $f_o$ = output frequency in MHz; $V_{CC}$ = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | DWG NUMBER |
|---|---|---|---|
| 56-Pin Plastic TSSOP Type II | –40°C to +85°C | 74ALVCH16500 DGG | SOT364-1 |

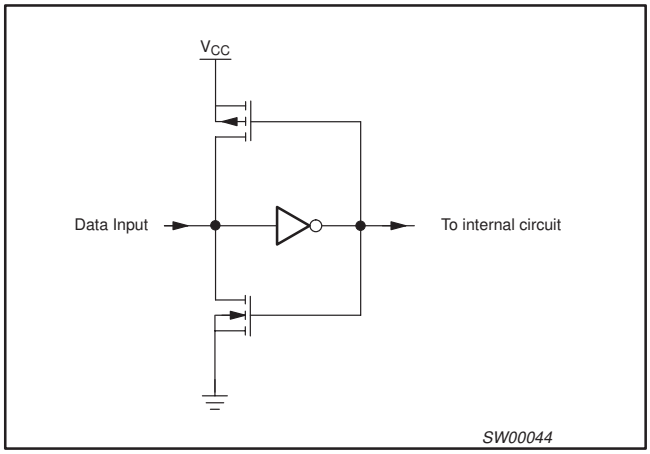
## PIN CONFIGURATION



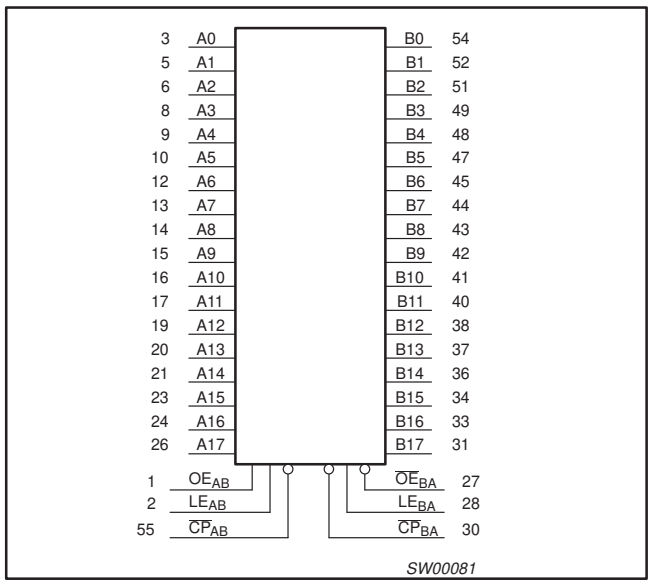

## PIN DESCRIPTION

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1 | $OE_{AB}$ | Output enable A-to-B |
| 2 | $LE_{AB}$ | Latch enable A-to-B |
| 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26 | A0 to A17 | Data inputs/outputs |
| 4, 11, 18, 25, 29, 32, 39, 46, 53, 56 | GND | Ground (0V) |
| 7, 22, 35, 50 | $V_{CC}$ | Positive supply voltage |
| 27 | $\overline{OE}_{BA}$ | Output enable B-to-A |
| 28 | $LE_{BA}$ | Latch enable B-to-A |
| 30 | $\overline{CP}_{BA}$ | Clock input B-to-A |
| 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31 | B0 to B17 | Data inputs/outputs |
| 55 | $\overline{CP}_{AB}$ | Clock input A-to-B |

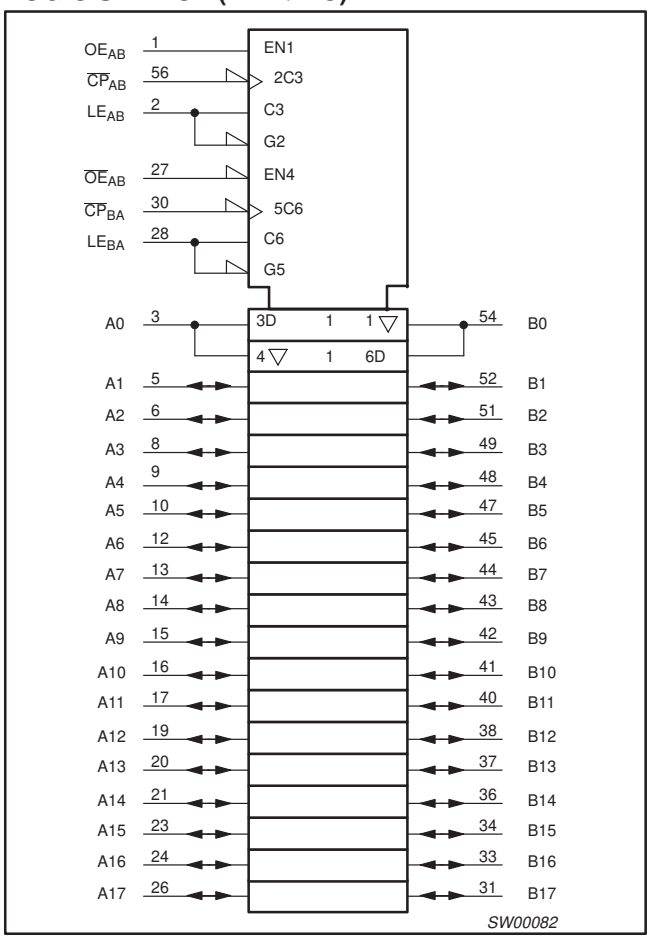
## BUS HOLD CIRCUIT



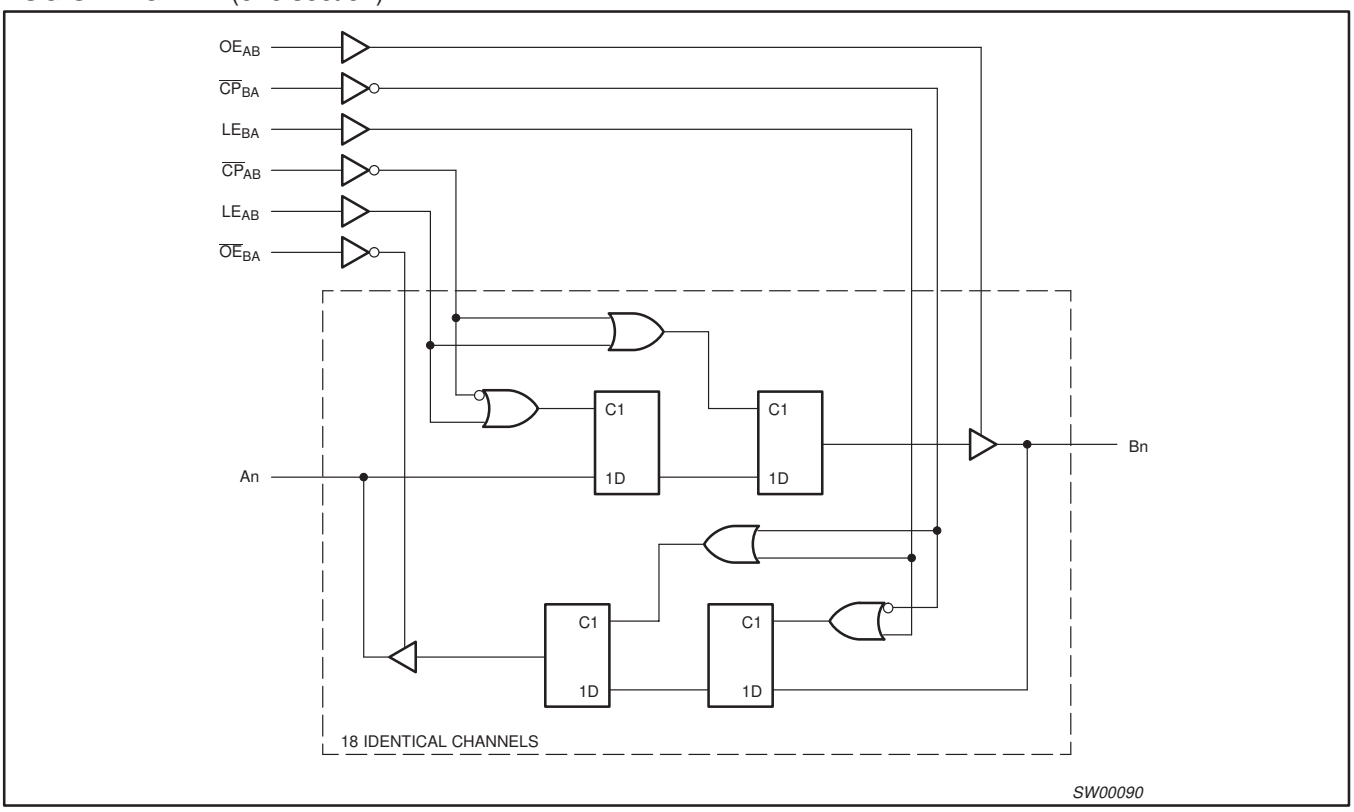
## LOGIC SYMBOL




## LOGIC SYMBOL (IEEE/IEC)



## LOGIC DIAGRAM (one section)




## FUNCTION TABLE

| INPUTS | | | | OUTPUTS | OPERATING MODE |
|---|---|---|---|---|---|
| OEAB | LEAB | $\overline{CPAB}$ | An | Bn | |
| L | H | X | X | Z | Disabled |
| H | H | X | H | H | Transparent |
| H | H | X | L | L | |
| H | ↓ | X | h | H | Latch data & display |
| H | ↓ | X | I | L | |
| H | L | ↓ | h | H | Clock data & display |
| H | L | ↓ | I | L | |
| H | L | H or L | X | H | Hold data & display |
| H | L | H or L | X | L | |

**NOTE:** A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CPBA}$.

H = High voltage level
h = High voltage level one set-up time prior to the Enable or Clock transition
L = Low voltage level
I = Low voltage level one set-up time prior to the Enable or Clock transition
NC= No Change
X = Don't care
Z = High Impedance "off" state
↓ = High-to-Low Enable or Clock transition

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $V_{CC}$ | DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load) | | 2.3 | 2.7 | V |
| | DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load) | | 3.0 | 3.6 | |
| $V_I$ | DC Input voltage range | | 0 | $V_{CC}$ | V |
| $V_O$ | DC output voltage range | | 0 | $V_{CC}$ | V |
| $T_{amb}$ | Operating free-air temperature range | | –40 | +85 | °C |
| $t_r$, $t_f$ | Input rise and fall times | $V_{CC}$ = 2.3 to 3.0V<br>$V_{CC}$ = 3.0 to 3.6V | 0<br>0 | 20<br>10 | ns/V |

## ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | –0.5 to +4.6 | V |
| $I_{IK}$ | DC input diode current | $V_I < 0$ | –50 | mA |
| $V_I$ | DC input voltage | For control pins[1] | –0.5 to +4.6 | V |
| | | For data inputs[1] | –0.5 to $V_{CC}$ +0.5 | |
| $I_{OK}$ | DC output diode current | $V_O > V_{CC}$ or $V_O < 0$ | ± 50 | mA |
| $V_O$ | DC output voltage | Note 1 | –0.5 to $V_{CC}$ +0.5 | V |
| $I_O$ | DC output source or sink current | $V_O$ = 0 to $V_{CC}$ | ± 50 | mA |
| $I_{GND}$, $I_{CC}$ | DC $V_{CC}$ or GND current | | ± 100 | mA |
| $T_{stg}$ | Storage temperature range | | –65 to +150 | °C |
| $P_{TOT}$ | Power dissipation per package –plastic thin-medium-shrink (TSSOP) | For temperature range: –40 to +125 °C above +55°C derate linearly with 8 mW/K | 600 | mW |

**NOTE:**
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Temp = -40°C to +85°C | | | |
| | | | MIN | TYP[1] | MAX | |
| $V_{IH}$ | HIGH level Input voltage | $V_{CC}$ = 2.3 to 2.7V | 1.7 | 1.2 | | V |
| | | $V_{CC}$ = 2.7 to 3.6V | 2.0 | 1.5 | | |
| $V_{IL}$ | LOW level Input voltage | $V_{CC}$ = 2.3 to 2.7V | | 1.2 | 0.7 | V |
| | | $V_{CC}$ = 2.7 to 3.6V | | 1.5 | 0.8 | |
| $V_{OH}$ | HIGH level output voltage | $V_{CC}$ = 2.3 to 3.6V; $V_I = V_{IH}$ or $V_{IL}$; $I_O = -100\mu A$ | $V_{CC} - 0.2$ | $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3V; $V_I = V_{IH}$ or $V_{IL}$; $I_O = -6mA$ | $V_{CC} - 0.3$ | $V_{CC} - 0.08$ | | |
| | | $V_{CC}$ = 2.3V; $V_I = V_{IH}$ or $V_{IL}$; $I_O = -12mA$ | $V_{CC} - 0.6$ | $V_{CC} - 0.26$ | | |
| | | $V_{CC}$ = 2.7V; $V_I = V_{IH}$ or $V_{IL}$; $I_O = -12mA$ | $V_{CC} - 0.5$ | $V_{CC} - 0.14$ | | |
| | | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O = -12mA$ | $V_{CC} - 0.6$ | $V_{CC} - 0.09$ | | |
| | | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O = -24mA$ | $V_{CC} - 1.0$ | $V_{CC} - 0.28$ | | |
| $V_{OL}$ | LOW level output voltage | $V_{CC}$ = 2.3 to 3.6V; $V_I = V_{IH}$ or $V_{IL}$; $I_O = 100\mu A$ | | GND | 0.20 | V |
| | | $V_{CC}$ = 2.3V; $V_I = V_{IH}$ or $V_{IL}$; $I_O = 6mA$ | | 0.07 | 0.40 | V |
| | | $V_{CC}$ = 2.3V; $V_I = V_{IH}$ or $V_{IL}$; $I_O = 12mA$ | | 0.15 | 0.70 | V |
| | | $V_{CC}$ = 2.7V; $V_I = V_{IH}$ or $V_{IL}$; $I_O = 12mA$ | | 0.14 | 0.40 | |
| | | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O = 24mA$ | | 0.27 | 0.55 | |
| $I_I$ | Input leakage current | $V_{CC}$ = 2.3 to 3.6V; $V_I = V_{CC}$ or GND | | 0.1 | 5 | µA |
| $I_{OZ}$ | 3-State output OFF-state current | $V_{CC}$ = 2.7 to 3.6V; $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND | | 0.1 | 10 | µA |
| $I_{CC}$ | Quiescent supply current | $V_{CC}$ = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; $I_O = 0$ | | 0.2 | 40 | µA |
| $\Delta I_{CC}$ | Additional quiescent supply current | $V_{CC}$ = 2.3V to 3.6V; $V_I = V_{CC} - 0.6V$; $I_O = 0$ | | 150 | 750 | µA |
| $I_{BHL}$ | Bus hold LOW sustaining current | $V_{CC}$ = 2.3V; $V_I = 0.7V$[2] | 45 | – | | µA |
| | | $V_{CC}$ = 3.0V; $V_I = 0.8V$[2] | 75 | 150 | | |
| $I_{BHH}$ | Bus hold HIGH sustaining current | $V_{CC}$ = 2.3V; $V_I = 1.7V$[2] | –45 | | | µA |
| | | $V_{CC}$ = 3.0V; $V_I = 2.0V$[2] | –75 | –175 | | |
| $I_{BHLO}$ | Bus hold LOW overdrive current | $V_{CC} = 3.6V$[2] | 500 | | | µA |
| $I_{BHHO}$ | Bus hold HIGH overdrive current | $V_{CC} = 3.6V$[2] | –500 | | | µA |

**NOTES:**
1. All typical values are at $T_{amb}$ = 25°C.
2. Valid for data inputs of bus hold parts.

## AC CHARACTERISTICS FOR $V_{CC}$ = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; $C_L$ = 30pF

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 2.5V ± 0.2V | | | |
| | | | MIN | TYP[1] | MAX | |
| $t_{PHL}/t_{PLH}$ | Propagation delay An, Bn to Bn, An | 1, 2 | 1.0 | 3.1 | 5.2 | ns |
| | Propagation delay $LE_{AB}$, $LE_{BA}$ to Bn, An | | 1.0 | 3.6 | 6.2 | |
| | Propagation delay $\overline{CP}_{AB}$, $\overline{CP}_{BA}$ to Bn, An | | 1.0 | 3.7 | 6.6 | |
| $t_{PZH}/t_{PZL}$ | 3-State output enable time $\overline{OE}_{BA}$ to An | 3 | 1.0 | 3.1 | 6.2 | ns |
| | 3-State output enable time $OE_{AB}$ to Bn | | 1.0 | 2.7 | 5.7 | |
| $t_{PHZ}/t_{PLZ}$ | 3-State output enable time $\overline{OE}_{BA}$ to An | 3 | 1.0 | 2.8 | 5.4 | ns |
| | 3-State output enable time $OE_{AB}$ to Bn | | 1.0 | 2.7 | 6.1 | |
| $t_W$ | Pulse width HIGH $LE_{AB}$, $LE_{BA}$ | 2 | 3.3 | 0.8 | – | ns |
| | Pulse width HIGH or LOW $\overline{CP}_{AB}$, $\overline{CP}_{BA}$ | | 3.3 | 2.0 | – | |
| $t_{SU}$ | Set-up time An, Bn to $\overline{CP}_{AB}$, $\overline{CP}_{BA}$ | 4 | 1.7 | 0.1 | – | ns |
| | Set-up time An, Bn to $LE_{AB}$, $LE_{BA}$ | | 1.9 | 0.1 | – | |
| $t_h$ | Hold time An, Bn to $\overline{CP}_{AB}$, $\overline{CP}_{BA}$ | 4 | 1.7 | 0.2 | – | ns |
| | Hold time An, Bn to $LE_{AB}$, $LE_{BA}$ | | 2.0 | 0.2 | – | |
| $f_{MAX}$ | Maximum clock frequency | | 150 | 333 | – | MHz |

**NOTE:**

1. All typical values are at $V_{CC}$ = 2.5V and $T_{amb}$ = 25°C.

## AC CHARACTERISTICS FOR $V_{CC}$ = 3.0V TO 3.6V RANGE AND $V_{CC}$ = 2.7V

GND = 0V; $t_r = t_f$ = 2.5ns; $C_L$ = 50pF

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3V ±0.3V | | | $V_{CC}$ = 2.7V | | | |
| | | | MIN | TYP[1] | MAX | MIN | TYP | MAX | |
| $t_{PHL}/t_{PLH}$ | Propagation delay An, Bn to Bn, An | 1, 2 | 1.0 | 2.9 | 4.2 | | 3.1 | 4.7 | ns |
| | Propagation delay $LE_{AB}$, $LE_{BA}$ to Bn, An | | 1.0 | 3.1 | 4.9 | | 3.4 | 5.5 | |
| | Propagation delay $\overline{CP}_{AB}$, $\overline{CP}_{BA}$ to Bn, An | | 1.1 | 3.3 | 5.5 | | 3.8 | 6.6 | |
| $t_{PZH}/t_{PZL}$ | 3-State output enable time $\overline{OE}_{BA}$ to An | 3 | 1.0 | 2.8 | 5.2 | | 3.3 | 6.2 | ns |
| | 3-State output enable time $OE_{AB}$ to Bn | | 1.0 | 2.5 | 4.6 | | 2.7 | 5.4 | |
| $t_{PHZ}/t_{PLZ}$ | 3-State output disable time $\overline{OE}_{BA}$ to An | 3 | 1.0 | 3.2 | 4.3 | | 3.3 | 4.6 | ns |
| | 3-State output disable tiime $OE_{AB}$ to Bn | | 1.5 | 3.2 | 5.0 | | 3.6 | 5.7 | |
| $t_W$ | LE pulse width $LE_{AB}$, $LE_{BA}$ to $\overline{CP}_{AB}$, $\overline{CP}_{BA}$ | 2 | 3.3 | 0.9 | | 3.3 | 0.7 | | ns |
| | LE pulse width HIGH or LOW $\overline{CP}_{AB}$, $\overline{CP}_{BA}$ | | 3.3 | 1.1 | | 3.3 | 1.4 | | |
| $t_{SU}$ | Set-up time An, Bn to $\overline{CP}_{AB}$, $\overline{CP}_{BA}$ | 4 | 1.3 | 0.2 | | 1.4 | 0.1 | | ns |
| | Set-up time An, Bn to $LE_{AB}$, $LE_{BA}$ | | 1.4 | 0.3 | | 1.6 | –0.2 | | |
| $t_h$ | Hold time An, Bn to $\overline{CP}_{AB}$, $\overline{CP}_{BA}$ | 4 | 1.3 | –0.1 | | 1.6 | 0.3 | | ns |
| | Hold time An, Bn to $LE_{AB}$, $LE_{BA}$ | | 1.5 | 0.1 | | 1.8 | 0.1 | | |
| $f_{MAX}$ | Maximum clock frequency | | 150 | 340 | | 150 | 333 | | MHz |

**NOTE:**

1. All typical values are at $V_{CC}$ = 3.3V and $T_{amb}$ = 25°C.

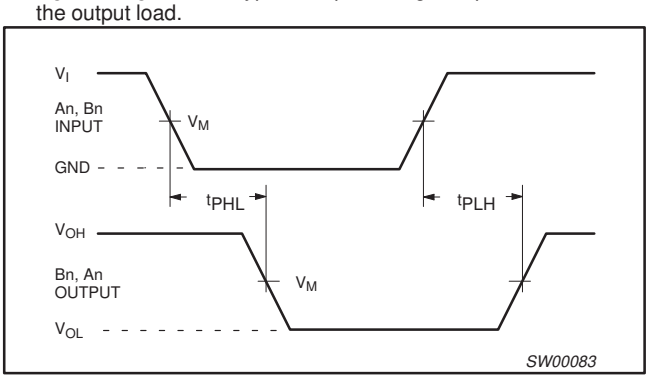
## AC WAVEFORMS

**$V_{CC}$ = 2.3 TO 2.7 V RANGE**

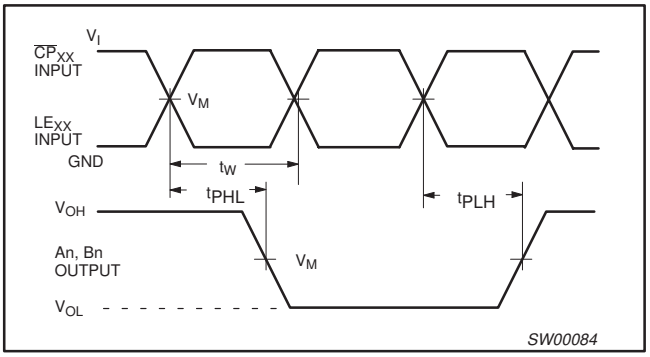
1. $V_M$ = 0.5 V
2. $V_X = V_{OL}$ + 0.15V
3. $V_Y = V_{OH}$ – 0.15V
4. $V_I = V_{CC}$
5. $V_{OL}$ and $V_{OH}$ are the typical output voltage drop that occur with the output load.

**$V_{CC}$ = 3.0 TO 3.6 V RANGE AND $V_{CC}$ = 2.7 V**

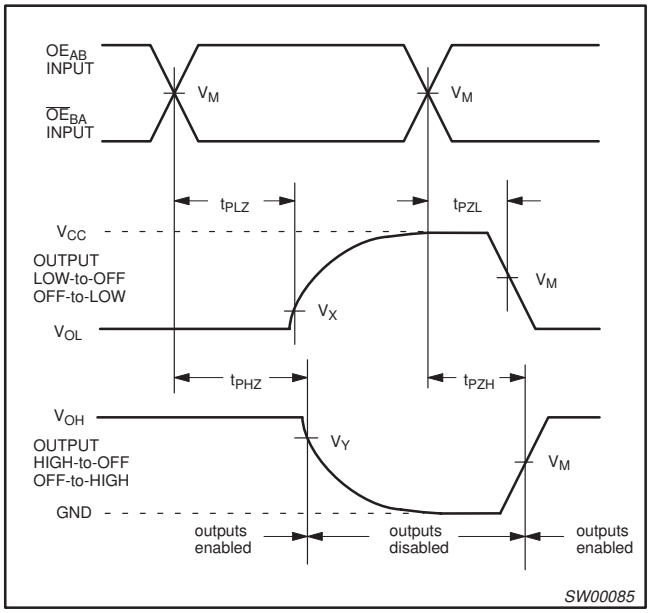
1. $V_M$ = 1.5 V
2. $V_X = V_{OL}$ + 0.3V
3. $V_Y = V_{OH}$ – 0.3V
4. $V_I$ = 2.7 V
5. $V_{OL}$ and $V_{OH}$ are the typical output voltage drop that occur with the output load.



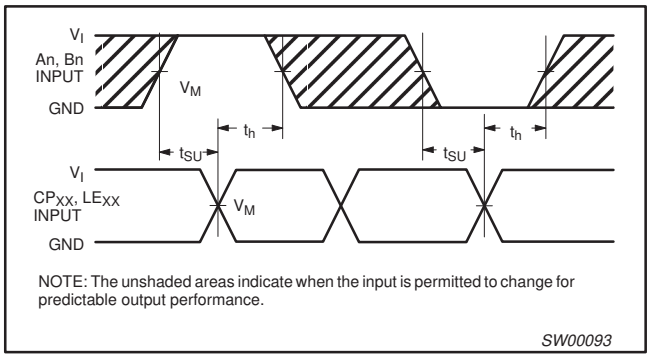

**Waveform 1. Input (An, Bn) to output (Bn, An) propagation times**




**Waveform 2. Latch enable input ($LE_{AB}$, $LE_{BA}$) and clock pulse input ($\overline{CP}_{AB}$, $\overline{CP}_{BA}$) to output (An, Bn) propagation delays and latch enable pulse width**

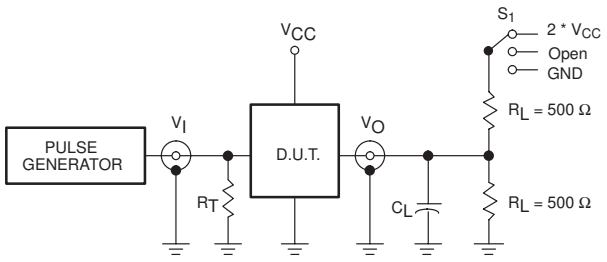



**Waveform 3. 3-State enable and disable times**




**Waveform 4. Data set-up and hold times for the An and Bn inputs to the $LE_{AB}$, $LE_{BA}$, $\overline{CP}_{AB}$ and $\overline{CP}_{BA}$ inputs**

## TEST CIRCUIT




**Test Circuit for switching times**

**DEFINITIONS**

$R_L$ = Load resistor

$C_L$ = Load capacitance includes jig and probe capacitance

$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.

**SWITCH POSITION**

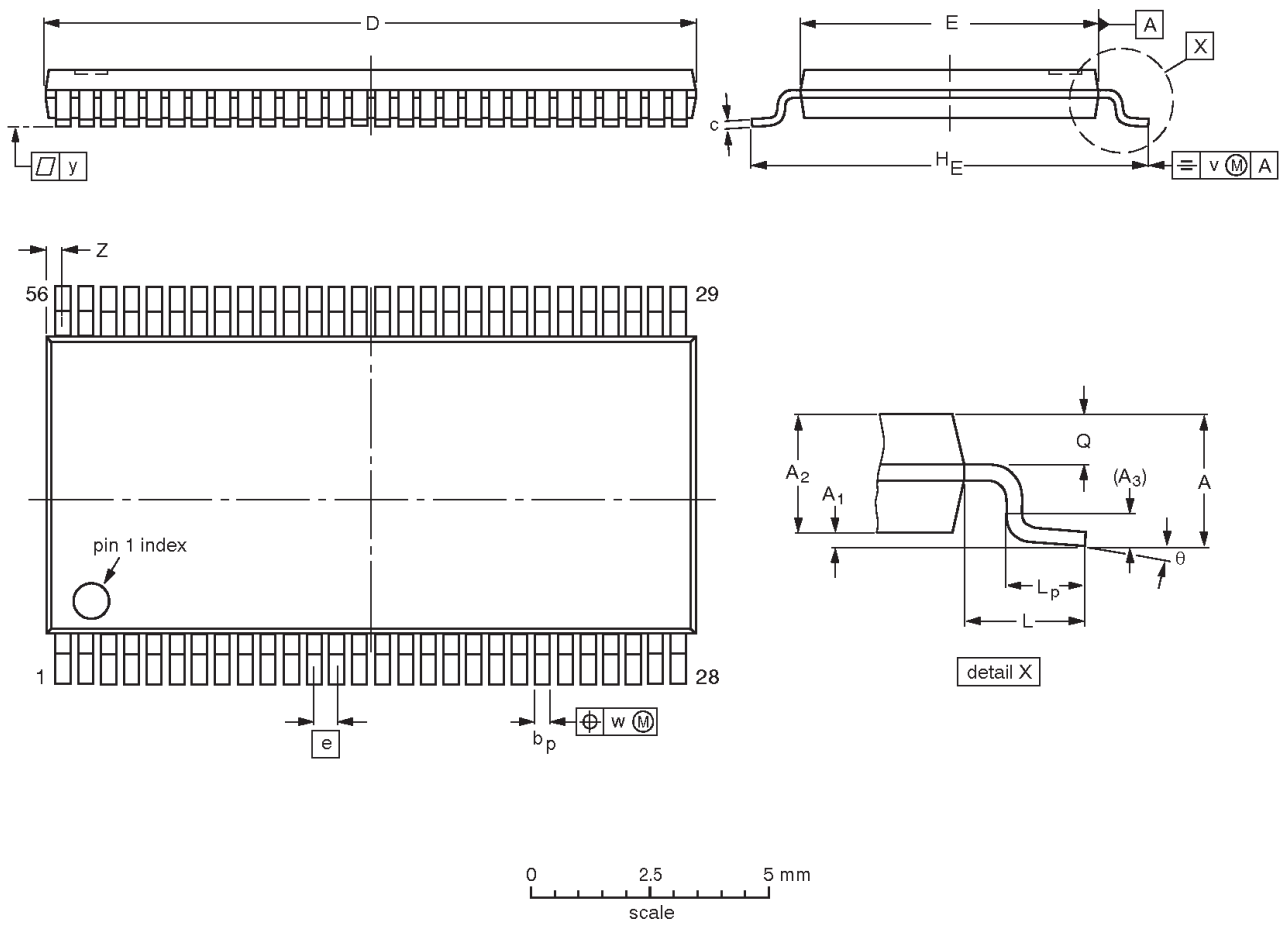
| TEST | $S_1$ |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 * $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

| $V_{CC}$ | $V_I$ |
|---|---|
| < 2.7V | $V_{CC}$ |
| 2.7–3.6V | 2.7V |

*SV00906*

**Waveform 5. Load circuitry for switching times**

**TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm** **SOT364-1**




**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.85 | 0.25 | 0.28<br>0.17 | 0.2<br>0.1 | 14.1<br>13.9 | 6.2<br>6.0 | 0.5 | 8.3<br>7.9 | 1.0 | 0.8<br>0.4 | 0.50<br>0.35 | 0.25 | 0.08 | 0.1 | 0.5<br>0.1 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | | |
| SOT364-1 | | MO-153EE | | | | | ~~93-02-03~~<br>95-02-10 |

**NOTES**

## DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|---|---|---|
| *Objective Specification* | Formative or in Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| *Preliminary Specification* | Preproduction Product | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| *Product Specification* | Full Production | This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product. |



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