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74ALVT16240

16-bit inverting buffer/driver; 3-state

Rev. 03 — 4 July 2005

Product data sheet

1. General description

The 74ALVT16240 is a high-performance BiCMOS device designed for V_{CC} operation at 2.5 V or 3.3 V with I/O compatibility up to 5 V.

The 74ALVT16240 is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four output enable inputs ($\overline{1OE}$, $\overline{2OE}$, $\overline{3OE}$, $\overline{4OE}$), each controlling four of the 3-state outputs.

2. Features

- 5 V I/O compatible
- Live insertion and extraction permitted
- 3-state buffers
- Power-up 3-state
- Output capability: +64 mA and -32 mA
- Latch-up protection:
 - ◆ JESD 78 exceeds 500 mA
- Electrostatic discharge protection:
 - ◆ MIL STD 883 method 3015: exceeds 2000 V
 - ◆ Machine model: exceeds 200 V
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- 16-bit bus interface
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- No bus current loading when output is tied to 5 V bus

3. Quick reference data

Table 1: Quick reference data

$T_{amb} = 25^\circ C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	propagation delay nAx to $n\overline{Y}_x$	$C_L = 50 \text{ pF}; V_{CC} = 2.5 \text{ V}$	1.0	2.5	3.7	ns
		$C_L = 50 \text{ pF}; V_{CC} = 3.3 \text{ V}$	0.5	1.7	3.0	ns
t_{PHL}	propagation delay nAx to $n\overline{Y}_x$	$C_L = 50 \text{ pF}; V_{CC} = 2.5 \text{ V}$	1.0	1.9	2.9	ns
		$C_L = 50 \text{ pF}; V_{CC} = 3.3 \text{ V}$	0.5	1.7	2.6	ns
C_i	input capacitance on $n\overline{OE}$	$V_I = 0 \text{ V or } V_{CC}$	-	3	-	pF

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Table 1: Quick reference data ...continued
 $T_{amb} = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_o	output capacitance	$V_{I/O} = 0 \text{ V or } V_{CC}$	-	9	-	pF
I_{CC}	supply current	outputs disabled; $V_{CC} = 2.5 \text{ V}$	-	40	100	μA
		outputs disabled; $V_{CC} = 3.3 \text{ V}$	-	60	100	μA

4. Ordering information

Table 2: Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74ALVT16240DL	-40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm		SOT370-1
74ALVT16240DGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm		SOT362-1

5. Functional diagram

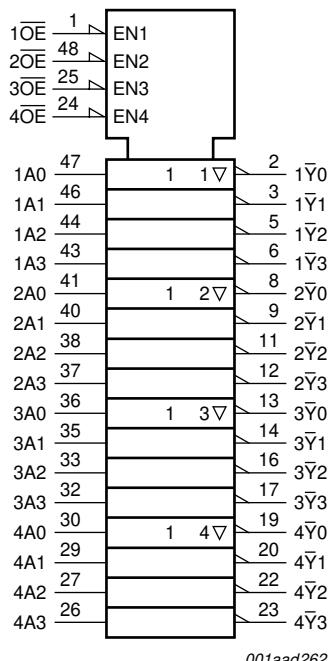


Fig 1. Logic symbol

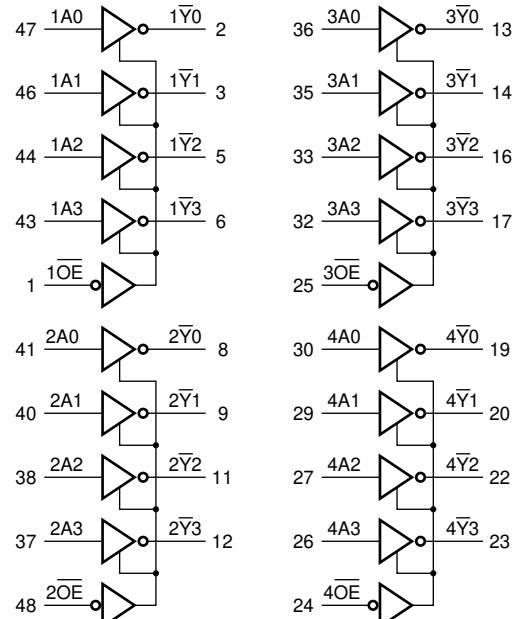
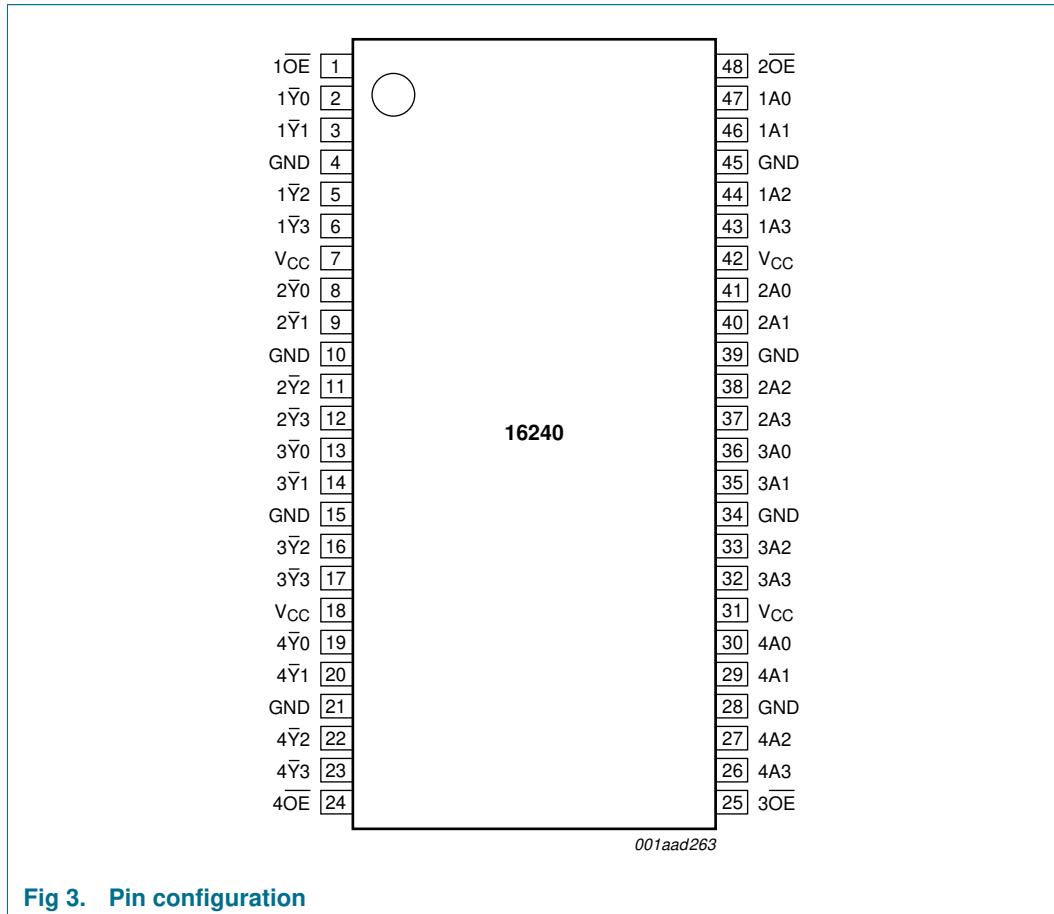


Fig 2. Logic diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
1OE	1	output enable input (active LOW)
1Y0	2	data output
1Y1	3	data output
GND	4	ground (0 V)
1Y2	5	data output
1Y3	6	data output
VCC	7	supply voltage
2Y0	8	data output
2Y1	9	data output
GND	10	ground (0 V)
2Y2	11	data output

Table 3: Pin description ...continued

Symbol	Pin	Description
2 \bar{Y} 3	12	data output
3 \bar{Y} 0	13	data output
3 \bar{Y} 1	14	data output
GND	15	ground (0 V)
3 \bar{Y} 2	16	data output
3 \bar{Y} 4	17	data output
V _{CC}	18	supply voltage
4 \bar{Y} 0	19	data output
4 \bar{Y} 1	20	data output
GND	21	ground (0 V)
4 \bar{Y} 2	22	data output
4 \bar{Y} 3	23	data output
4 \bar{OE}	24	output enable input (active LOW)
3 \bar{OE}	25	output enable input (active LOW)
4A3	26	data input
4A2	27	data input
GND	28	ground (0 V)
4A1	29	data input
4A0	30	data input
V _{CC}	31	supply voltage
3A3	32	data input
3A2	33	data input
GND	34	ground (0 V)
3A1	35	data input
3A0	36	data input
2A3	37	data input
2A2	38	data input
GND	39	ground (0 V)
2A1	40	data input
2A0	41	data input
V _{CC}	42	supply voltage
1A3	43	data input
1A2	44	data input
GND	45	ground (0 V)
1A1	46	data input
1A0	47	data input
2 \bar{OE}	48	output enable input (active LOW)

7. Functional description

7.1 Function table

Table 4: Function table [1]

Input		Output
$n\bar{O}E$	nAx	$n\bar{Y}x$
L	L	H
L	H	L
H	X	Z

- [1] H = HIGH voltage level;
- L = LOW voltage level;
- X = don't care;
- Z = high-impedance OFF-state.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to ground.

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{CC}	supply voltage		-0.5	+4.6	V	
I_{IK}	input diode current	$V_I < 0$ V	-	-50	mA	
V_I	input voltage		[1]	-0.5	+7.0	V
I_{OK}	output diode current	$V_O < 0$ V	-	-50	mA	
V_O	output voltage	output in OFF-state or HIGH-state	[1]	-0.5	+7.0	V
I_O	output current	output in LOW-state	-	128	mA	
		output in HIGH-state	-	-64	mA	
T_{stg}	storage temperature		-65	+150	°C	
T_j	junction temperature		[2]	-	+150	°C

- [1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$						
V_{CC}	supply voltage		2.3	-	2.7	V
V_I	input voltage		0	-	5.5	V
V_{IH}	HIGH-level input voltage		1.7	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.7	V
I_{OH}	HIGH-level output current		-	-	-8	mA
I_{OL}	LOW-level output current	none	-	-	8	mA
		current duty cycle $\leq 50\%$; $f \geq 1 \text{ kHz}$	-	-	24	mA
$\Delta t/\Delta V$	input transition rise or fall rate	outputs enabled	-	-	10	ns/V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$						
V_{CC}	supply voltage		3.0	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-	-	-32	mA
I_{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle $\leq 50\%$; $f \geq 1 \text{ kHz}$	-	-	64	mA
$\Delta t/\Delta V$	input transition rise or fall rate	outputs enabled	-	-	10	ns/V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C

10. Static characteristics

Table 7: Static characteristicsAt recommended operating conditions; voltages are referred to GND (ground = 0 V); $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ [1]							
V_{IK}	input diode voltage	$V_{CC} = 2.3 \text{ V}; I_{IK} = -18 \text{ mA}$	-	-0.85	-1.2	V	
V_{OH}	HIGH-level output voltage	$V_{CC} = 2.3 \text{ V}$ to $3.6 \text{ V}; I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$	V_{CC}	-	V	
		$V_{CC} = 2.3 \text{ V}; I_{OH} = -8 \text{ mA}$	1.8	2.5	-	V	
V_{OL}	LOW-level output voltage	$V_{CC} = 2.3 \text{ V}$					
		$I_{OL} = 100 \mu\text{A}$	-	0.07	0.2	V	
		$I_{OL} = 24 \text{ mA}$	-	0.3	0.5	V	
		$I_{OL} = 8 \text{ mA}$	-	-	0.4	V	
I_{LI}	input leakage current						
	control pins	$V_{CC} = 2.7 \text{ V}; V_I = V_{CC}$ or GND	-	0.1	± 1	μA	
		$V_{CC} = 0 \text{ V}$ or $2.7 \text{ V}; V_I = 5.5 \text{ V}$	-	0.1	10	μA	
	data pins	$V_{CC} = 2.7 \text{ V}; V_I = V_{CC}$	[2]	-	0.1	1	μA
		$V_{CC} = 2.7 \text{ V}; V_I = 0 \text{ V}$	[2]	-	+0.1	-5	μA
I_{OFF}	power-down output current	$V_{CC} = 0 \text{ V}; V_O = 0 \text{ V}$ to 4.5 V	-	0.1	± 100	μA	
I_{HOLD}	bus hold current on data inputs	$V_{CC} = 2.3 \text{ V}; V_I = 0.7 \text{ V}$	[3]	-	90	-	μA
		$V_{CC} = 2.3 \text{ V}; V_I = 1.7 \text{ V}$	[3]	-	-10	-	μA
I_{EX}	external current into output	output HIGH-state; $V_O = 5.5 \text{ V}$; $V_{CC} = 2.3 \text{ V}$	-	10	125	μA	
I_{PU}	power-up 3-state output current	$V_{CC} \leq 1.2 \text{ V}; V_O = 0.5 \text{ V}$ to V_{CC} ; $V_I = \text{GND}$ or V_{CC}	[4]	-	1	± 100	μA
I_{PD}	power-down 3-state output current	$V_{CC} \leq 1.2 \text{ V}; V_O = 0.5 \text{ V}$ to V_{CC} ; $V_I = \text{GND}$ or V_{CC}	[4]	-	1	± 100	μA
I_{OZ}	3-state output current	$V_{CC} = 2.7 \text{ V}; V_I = V_{IL}$ or V_{IH}					
		output HIGH-state; $V_O = 2.3 \text{ V}$	-	0.5	5	μA	
		output LOW-state; $V_O = 0.5 \text{ V}$	-	+0.5	-5	μA	
I_{CC}	supply current	$V_{CC} = 2.7 \text{ V}; V_I = \text{GND}$ or $V_{CC}; I_O = 0 \text{ A}$					
		outputs HIGH-state	-	0.04	0.1	mA	
		outputs LOW-state	-	2.7	4.5	mA	
		outputs disabled	[5]	-	0.04	0.1	mA
ΔI_{CC}	additional supply current per input pin	$V_{CC} = 2.3 \text{ V}$ to 2.7 V ; one input at $V_{CC} - 0.6 \text{ V}$; other inputs at V_{CC} or GND	[6]	-	0.04	0.4	mA
C_i	input capacitance on $n\overline{OE}$	$V_I = 0 \text{ V}$ or V_{CC}	-	3	-	pF	
C_o	output capacitance	$V_{I/O} = 0 \text{ V}$ or V_{CC}	-	9	-	pF	
$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ [7]							
V_{IK}	input diode voltage	$V_{CC} = 3.0 \text{ V}; I_{IK} = -18 \text{ mA}$	-	-0.85	-1.2	V	
V_{OH}	HIGH-level output voltage	$V_{CC} = 3.0 \text{ V}$ to $3.6 \text{ V}; I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$	V_{CC}	-	V	
		$V_{CC} = 3.0 \text{ V}; I_{OH} = -32 \text{ mA}$	2.0	2.3	-	V	

Table 7: Static characteristics ...continuedAt recommended operating conditions; voltages are referred to GND (ground = 0 V); $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V_{OL}	LOW-level output voltage	$V_{CC} = 3.0\text{ V}$					
		$I_{OL} = 100\text{ }\mu\text{A}$	-	0.07	0.2	V	
		$I_{OL} = 16\text{ mA}$	-	0.25	0.4	V	
		$I_{OL} = 32\text{ mA}$	-	0.3	0.5	V	
		$I_{OL} = 64\text{ mA}$	-	0.4	0.55	V	
I_{LI}	input leakage current	$V_{CC} = 3.6\text{ V}; V_I = V_{CC}$ or GND	-	0.1	± 1	μA	
		$V_{CC} = 0\text{ V}$ or $3.6\text{ V}; V_I = 5.5\text{ V}$	-	0.1	10	μA	
		$V_{CC} = 3.6\text{ V}; V_I = V_{CC}$	[2]	-	0.5	1	μA
		$V_{CC} = 3.6\text{ V}; V_I = 0\text{ V}$	[2]	-	+0.1	-5	μA
I_{OFF}	power-down output current	$V_{CC} = 0\text{ V}; V_I$ or $V_O = 0\text{ V}$ to 4.5 V	-	0.1	± 100	μA	
I_{HOLD}	bus hold current on data inputs	$V_{CC} = 3\text{ V}; V_I = 0.8\text{ V}$	[3]	75	130	-	μA
		$V_{CC} = 3\text{ V}; V_I = 2.0\text{ V}$	[3]	-75	-140	-	μA
		$V_{CC} = 0\text{ V}$ to $3.6\text{ V}; V_I = 3.6\text{ V}$	[3]	± 500	-	-	μA
I_{PU}	power-up 3-state output current	$V_{CC} \leq 1.2\text{ V}; V_O = 0.5\text{ V}$ to V_{CC} ; $V_I = \text{GND}$ or V_{CC}	[8]	-	1	± 100	μA
I_{PD}	power-down 3-state output current	$V_{CC} \leq 1.2\text{ V}; V_O = 0.5\text{ V}$ to V_{CC} ; $V_I = \text{GND}$ or V_{CC}	[8]	-	1	± 100	μA
I_{OZ}	3-state output current	$V_{CC} = 3.6\text{ V}; V_I = V_{IL}$ or V_{IH}					
		output HIGH-state; $V_O = 3.0\text{ V}$	-	0.5	5	μA	
		output LOW-state; $V_O = 0.5\text{ V}$	-	+0.5	-5	μA	
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}; V_I = \text{GND}$ or V_{CC} ; $I_O = 0\text{ A}$					
		outputs HIGH-state	-	0.05	0.1	mA	
		outputs LOW-state	-	3.9	5.5	mA	
		outputs disabled	[5]	-	0.06	0.1	mA
ΔI_{CC}	additional supply current per input pin	$V_{CC} = 3\text{ V}$ to 3.6 V ; one input at $V_{CC} - 0.6\text{ V}$; other inputs at V_{CC} or GND	[6]	-	0.04	0.4	mA

[1] All typical values are at $V_{CC} = 2.5\text{ V}$ and $T_{amb} = 25^{\circ}\text{C}$.[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms . From $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ a transition time of $100\text{ }\mu\text{s}$ is permitted. This parameter is valid for $T_{amb} = 25^{\circ}\text{C}$ only.[5] I_{CC} is measured with outputs pulled up to V_{CC} or pulled down to ground.[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.[7] All typical values are at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25^{\circ}\text{C}$.[8] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms . From $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ a transition time of $100\text{ }\mu\text{s}$ is permitted. This parameter is valid for $T_{amb} = 25^{\circ}\text{C}$ only.

11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$; for test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ [1]						
t_{PLH}	propagation delay nAx to n \bar{Y}_x	see Figure 4	1.0	2.5	3.7	ns
t_{PHL}	propagation delay nAx to n \bar{Y}_x	see Figure 4	1.0	1.9	2.9	ns
t_{PZH}	output enable time to HIGH-level	see Figure 5	1.0	3.3	5.3	ns
t_{PZL}	output enable time to LOW-level	see Figure 5	1.0	2.6	4.2	ns
t_{PHZ}	output disable time from HIGH-level	see Figure 5	1.0	2.5	4.0	ns
t_{PLZ}	output disable time from LOW-level	see Figure 5	1.0	1.8	3.0	ns
$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ [2]						
t_{PLH}	propagation delay nAx to n \bar{Y}_x	see Figure 4	0.5	1.7	3.0	ns
t_{PHL}	propagation delay nAx to n \bar{Y}_x	see Figure 4	0.5	1.7	2.6	ns
t_{PZH}	output enable time to HIGH-level	see Figure 5	1.0	2.5	3.2	ns
t_{PZL}	output enable time to LOW-level	see Figure 5	1.0	1.9	3.1	ns
t_{PHZ}	output disable time from HIGH-level	see Figure 5	1.5	2.8	4.1	ns
t_{PLZ}	output disable time from LOW-level	see Figure 5	1.5	2.3	3.4	ns

[1] All typical values are at $V_{CC} = 2.5 \text{ V}$ and $T_{amb} = 25^{\circ}\text{C}$.

[2] All typical values are at $V_{CC} = 3.3 \text{ V}$ and $T_{amb} = 25^{\circ}\text{C}$.

12. Waveforms

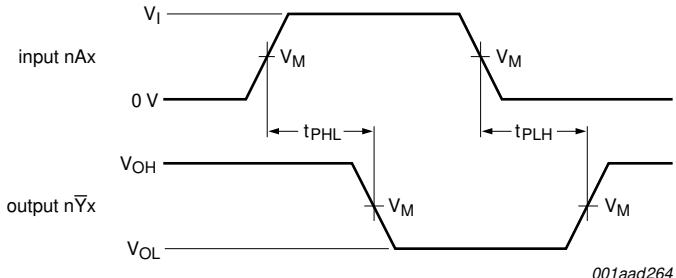


Fig 4. Input (nAx) to output (nYx) propagation delays

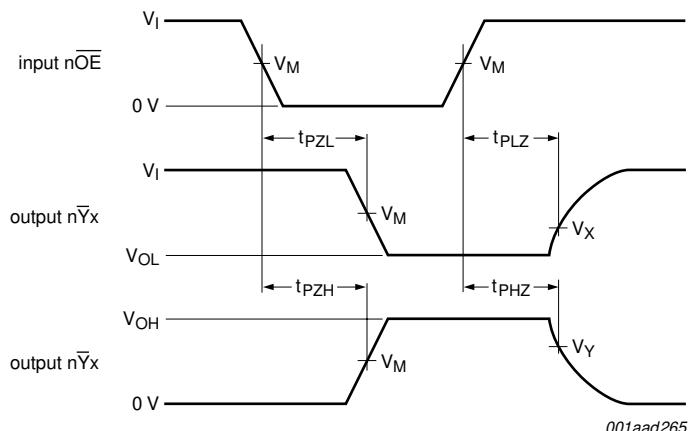
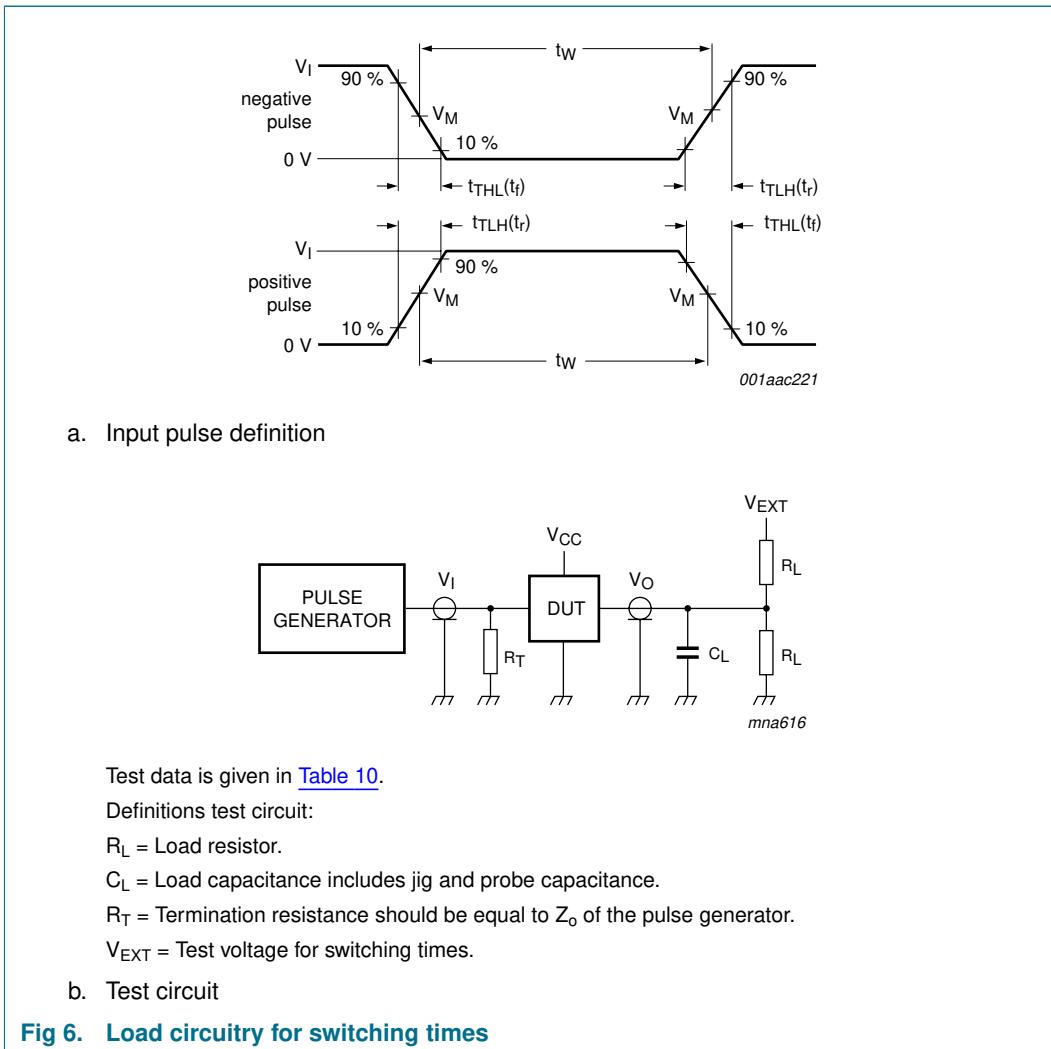


Fig 5. 3-state output enable and disable times

Table 9: Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
$\geq 3 \text{ V}$	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
$\leq 2.7 \text{ V}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$

**Table 10: Test data**

Input				Load		V_{EXT}			
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}	
3.0 V or V_{CC} whichever is less	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V or $2 \times V_{CC}$	open	

13. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

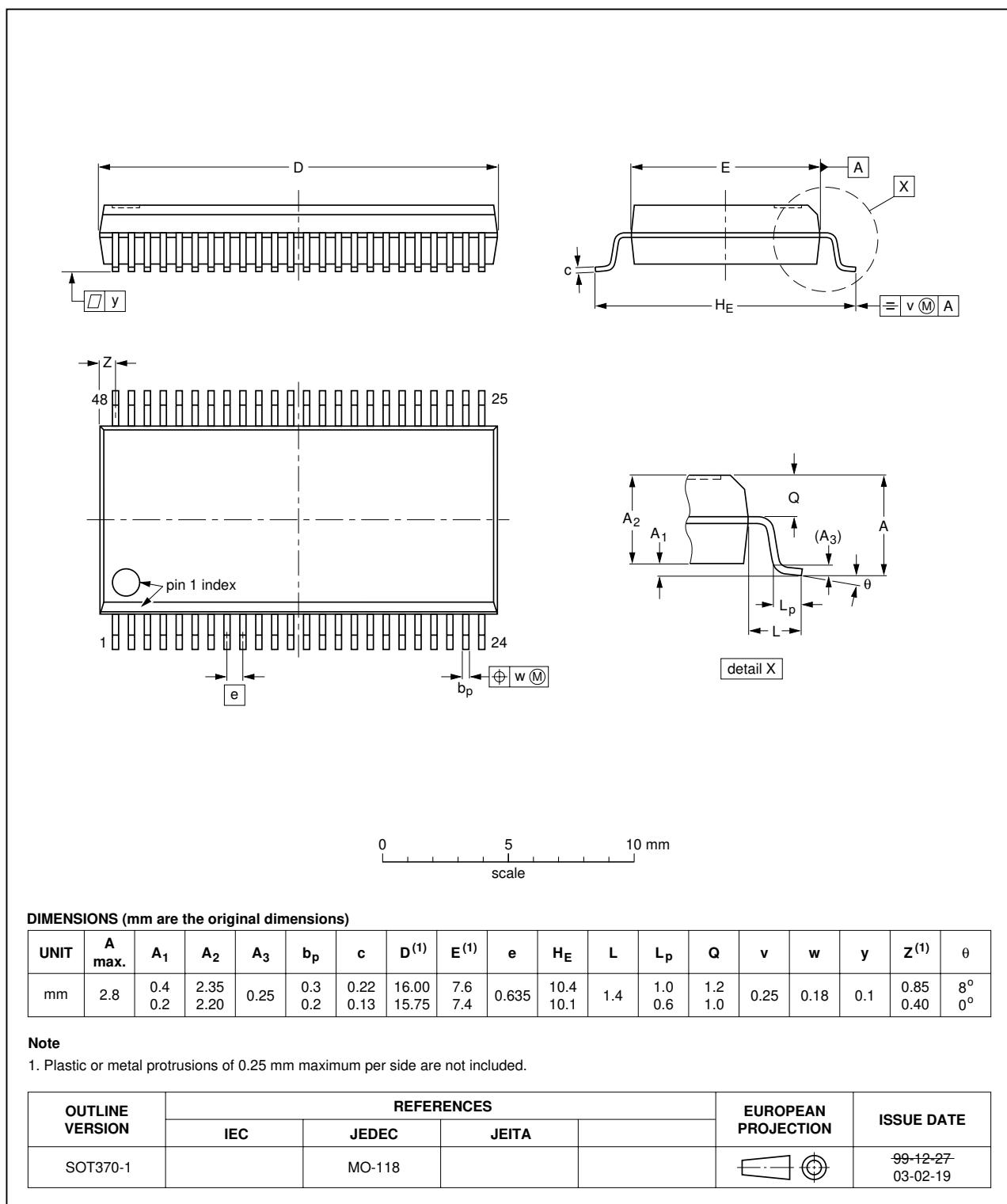
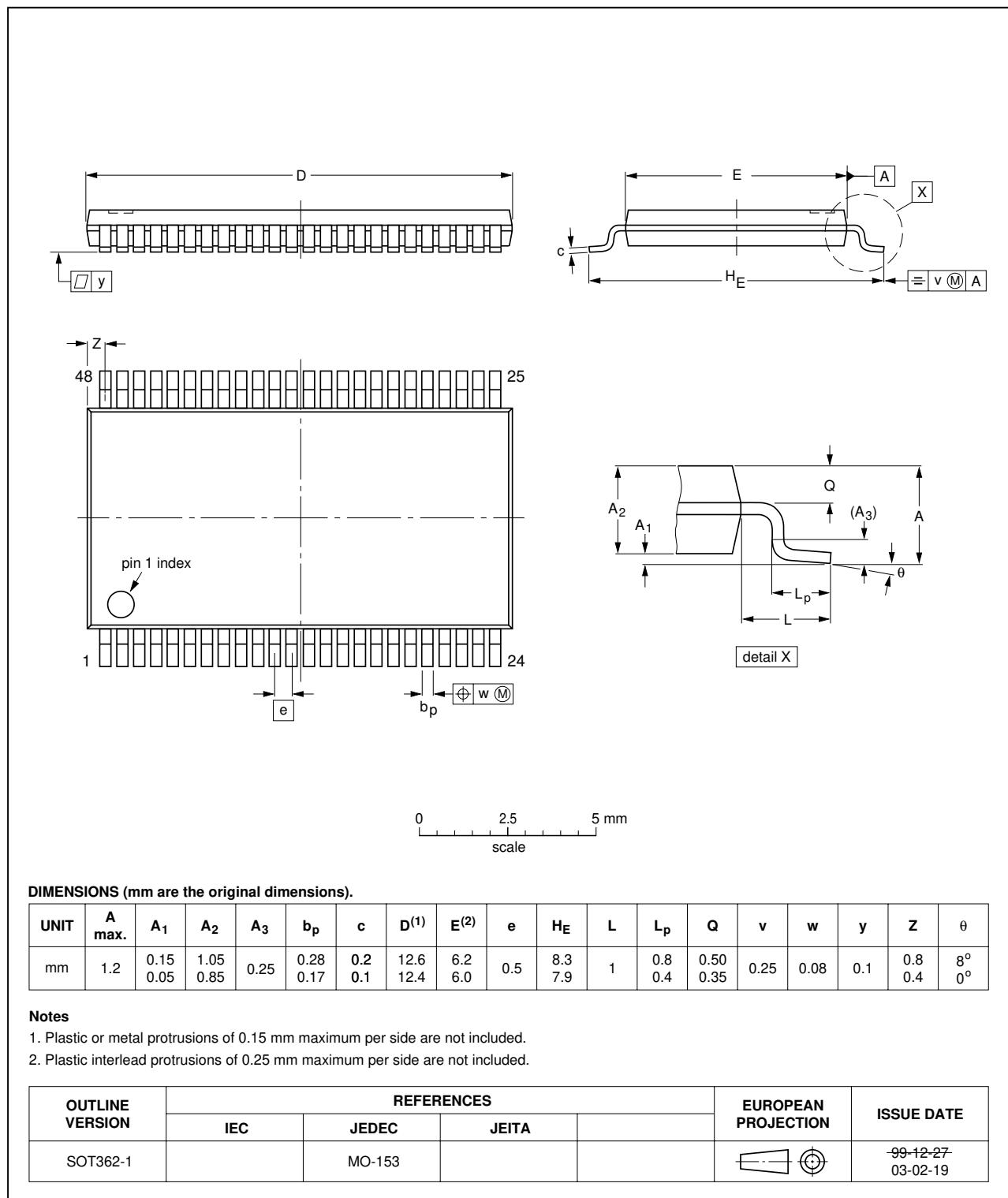


Fig 7. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				-99-12-27 03-02-19

Fig 8. Package outline SOT362-1 (TSSOP48)

14. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74ALVT16240_3	20050704	Product data sheet	-	9397 750 15192	74ALVT16240_2
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.In Table 8; update of the typical and maximum value of t_{PZH} at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$				
74ALVT16240_2	19980213	Product specification	-	9397 750 03615	74ALVT16240_1
74ALVT16240_1	19970502	-	-	-	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

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