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Team Nexperia

DATA SHEET

74ALVT16373

2.5V/3.3V 16-bit transparent
D-type latch (3-State)

Product specification
Supersedes data of 1998 Feb 13
IC23 Data Handbook

1999 Oct 18

Philips Semiconductors

PHILIPS

2.5V/3.3V 16-bit transparent D-type latch (3-State) 74ALVT16373

FEATURES

- 16-bit transparent latch
- 5V I/O compatibile
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16373 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

This device is a 16-bit transparent D-type latch with non-inverting 3-State bus compatible outputs. The device can be used as two 8-bit latches or one 16-bit latch. When latch enable (LE) input is High, the Q outputs follow the data (D) inputs. When latch enable is taken Low, the Q outputs are latched at the levels of the D inputs one setup time prior to the High-to-Low transition.

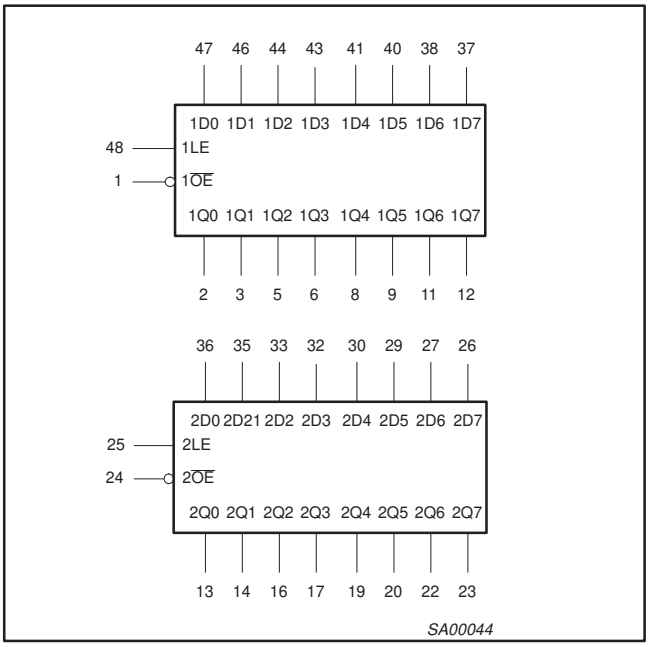
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	C_L = 50pF	2.0 2.4	1.6 1.8	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

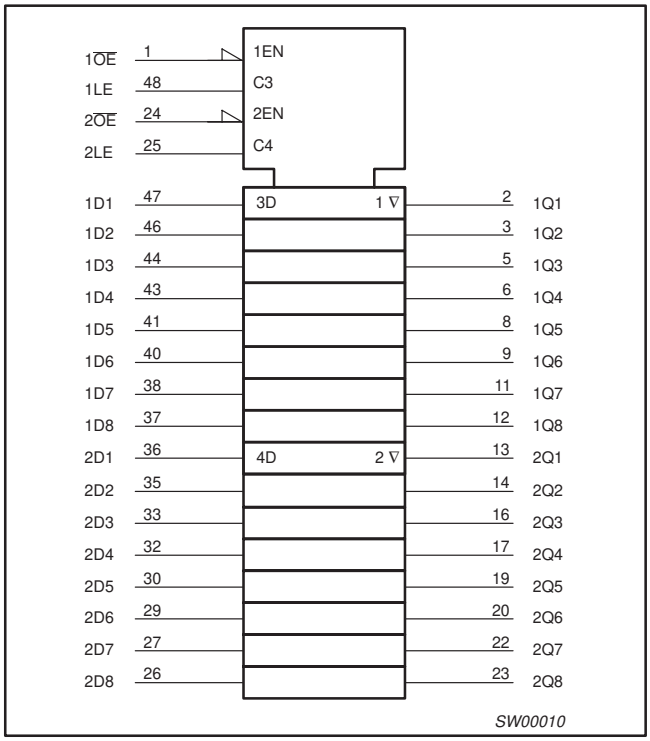
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16373 DL	AV16373 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16373 DGG	AV16373 DGG	SOT362-1

LOGIC SYMBOL



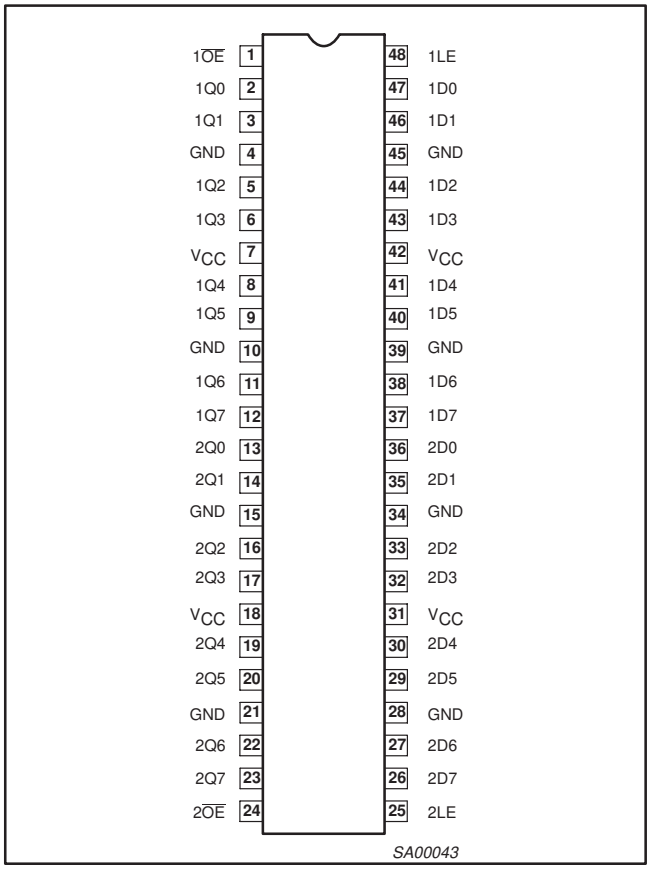
LOGIC SYMBOL (IEEE/IEC)



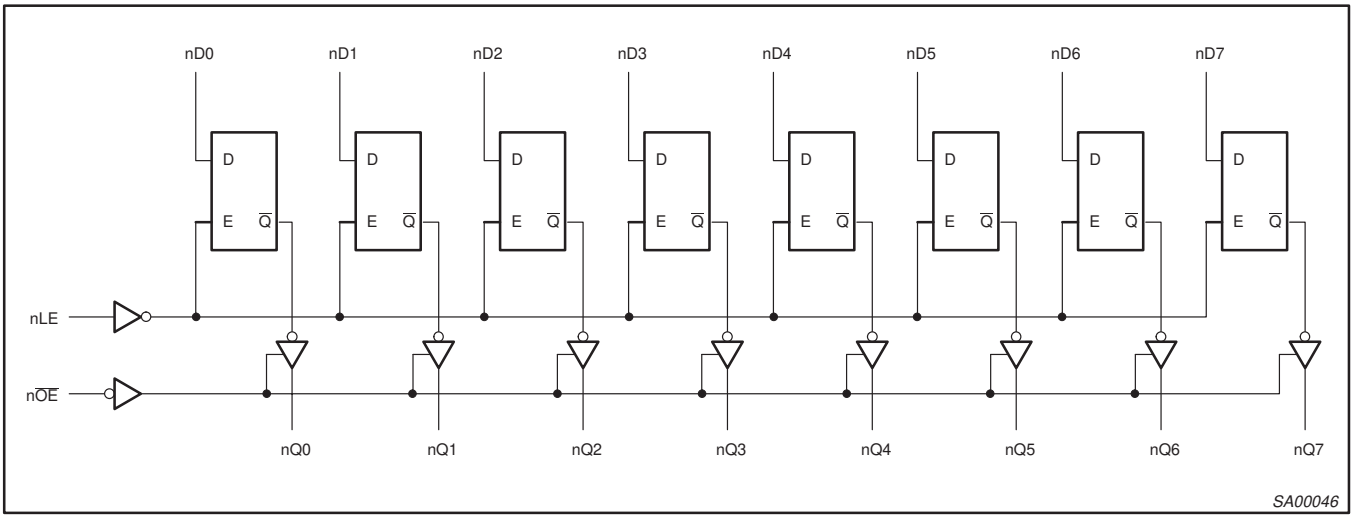
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
48, 25	1LE, 2LE	Enable inputs (active-High)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nLE	nDx	REGISTER	nQ0 – nQ7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X nDx	NC nDx	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.5	5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.05	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	0.5 0.5	1.6 1.8	2.5 2.9	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQx	1	1.0 1.0	2.0 2.3	3.1 3.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.5 1.0	2.3 1.9	4.0 3.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	4 5	1.5 1.5	2.9 2.3	4.5 3.7	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2			V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8			
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.3	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	1.0 1.0	2.0 2.4	3.2 4.2	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQx	1	1.5 1.5	2.6 2.8	4.2 4.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	2.0 1.5	3.5 2.6	5.5 4.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	4 5	1.5 1.0	2.7 2.0	4.5 3.5	ns

NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

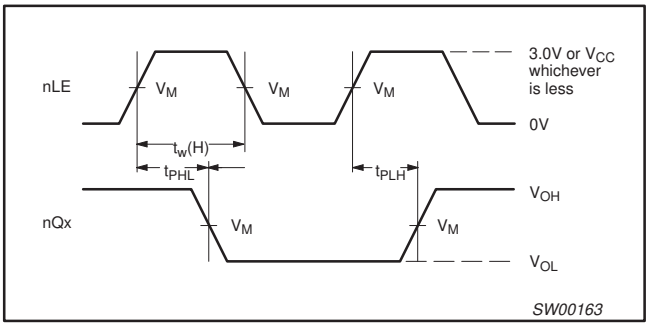
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

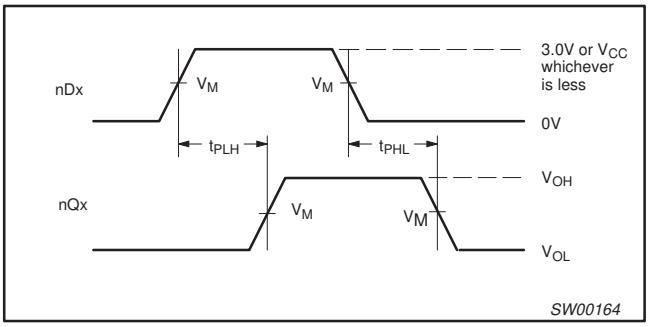
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 2.5V ±0.2V		V_{CC} = 3.3V ±0.3V		
			MIN	TYP	MIN	TYP	
$t_S(H)$ $t_S(L)$	Setup time nDx to nLE	3	0 1.5	–0.7 0.2	0.5 0.8	–0.2 0.2	ns
$t_h(H)$ $t_h(L)$	Hold time nDx to nLE	3	0.5 1.5	–0.2 0.7	0.8 1.0	0 0.2	ns
$t_W(H)$	nLE pulse width High	1	1.5 1.5		1.5 1.5		ns

AC WAVEFORMS

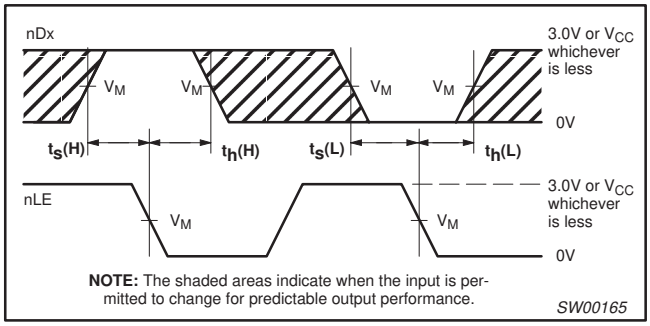
For all waveforms
V_M = 1.5V for $V_{CC} \geq$ 3.0V; $V_M = V_{CC}/2$ for $V_{CC} \leq$ 2.7V
V_M = 1.5V for $V_{CC} \geq$ 3.0V; $V_M = V_{CC}/2$ for $V_{CC} \leq$ 2.7V
$V_X = V_{OL}$ + 0.3V for $V_{CC} \geq$ 3.0V; $V_X = V_{OL}$ + 0.15V for $V_{CC} \leq$ 2.7V
$V_Y = V_{OH}$ – 0.3V for $V_{CC} \geq$ 3.0V; $V_Y = V_{OH}$ – 0.15V for $V_{CC} \leq$ 2.7V



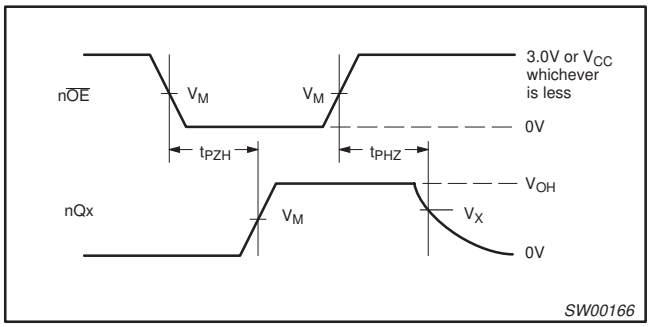
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



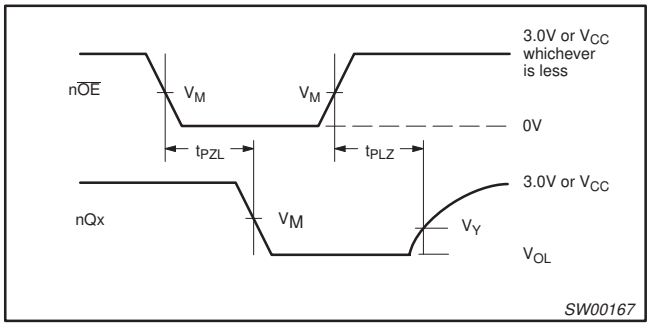
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times

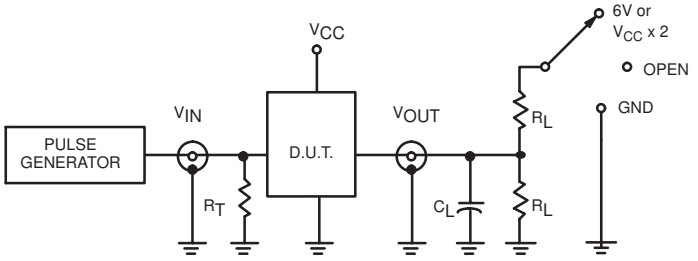


Waveform 4. 3-State Output Enable time to High Level and Output Disable Time from High Level

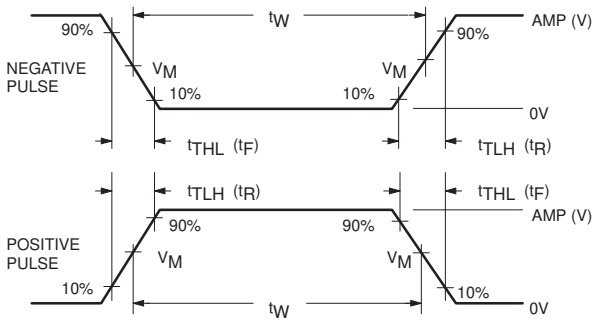


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V or V_{CC} / 2, whichever is less
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

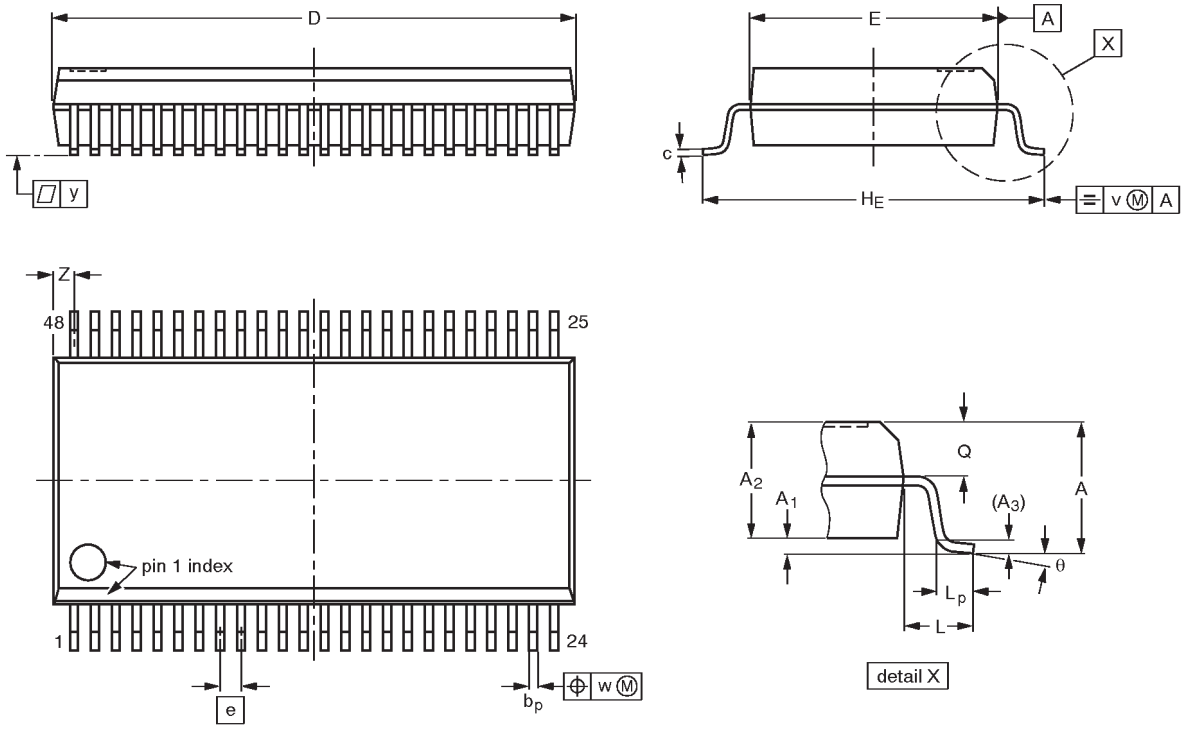
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

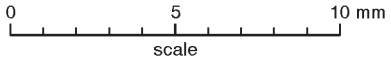
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00162

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**





DIMENSIONS (mm are the original dimensions)

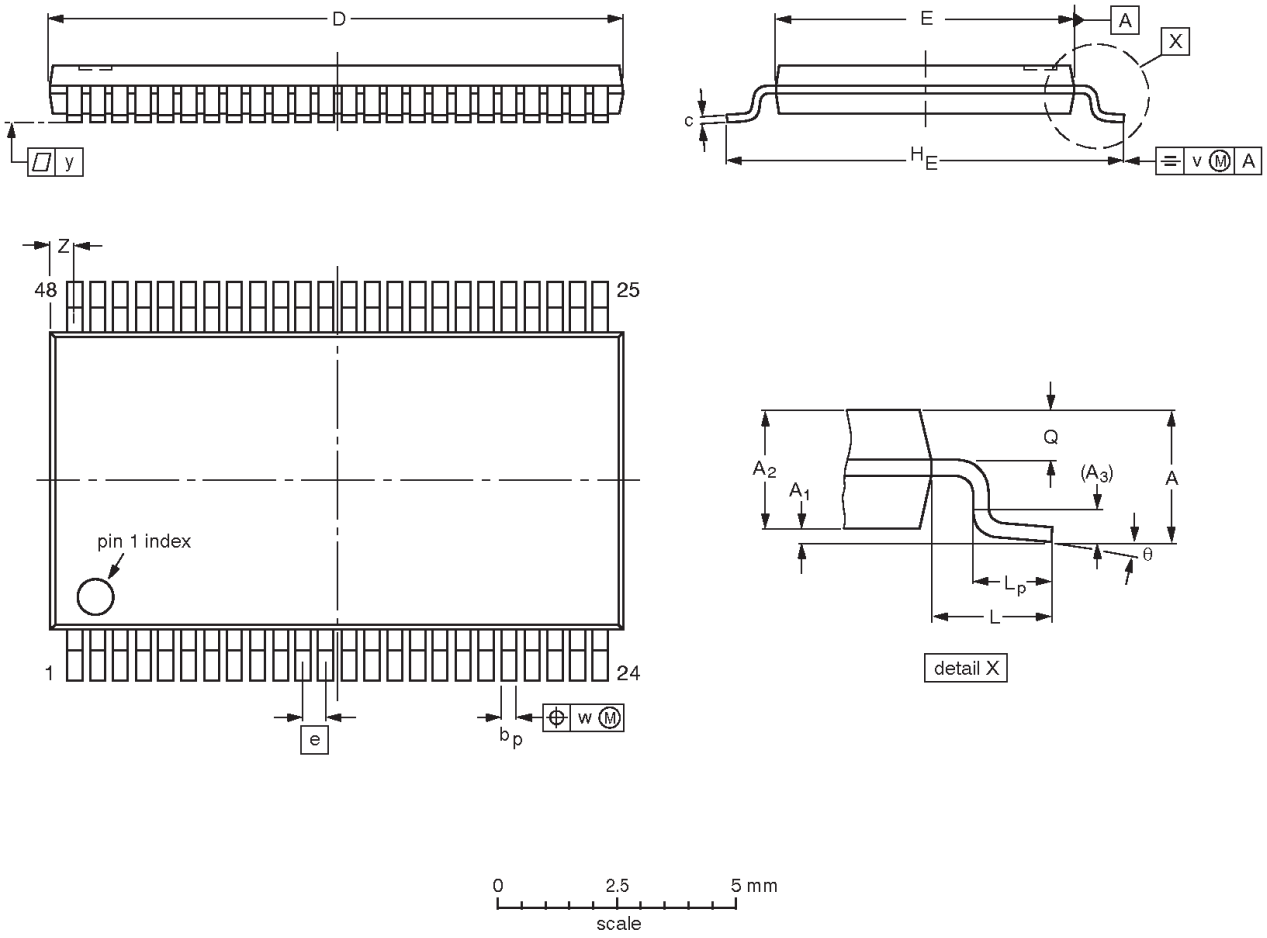
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				~~93-11-02~~ 95-02-04

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153ED					~~93-02-03~~ 95-02-10

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

print code Date of release: 10-99

Document order number: 9397-750-06516

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