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Team Nexperia

DATA SHEET

74ALVT16543

2.5 V/3.3 V ALVT 16-bit registered transceiver (3-State)

Product data sheet
Supersedes data of 1998 Feb 13

2004 Sep 14

Philips
Semiconductors

PHILIPS

2.5 V/3.3 V 16-bit registered transceiver (3-State) 74ALVT16543

FEATURES

- 16-bit universal bus interface
- 5 V I/O Compatible
- 3-State buffers
- Output capability: +64 mA/–32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- No bus current loading when output is tied to 5 V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ALVT16543 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5 V or 3.3 V with I/O compatibility up to 5 V. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74ALVT16543 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($n\overline{EAB}$) input and the A-to-B Latch Enable ($n\overline{LEAB}$) input are LOW, the A-to-B path is transparent.

A subsequent LOW-to-HIGH transition of the $n\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $n\overline{EAB}$ and $n\overline{OEAB}$ both LOW, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $n\overline{EBA}$, $n\overline{LEBA}$, and $n\overline{OEBA}$ inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

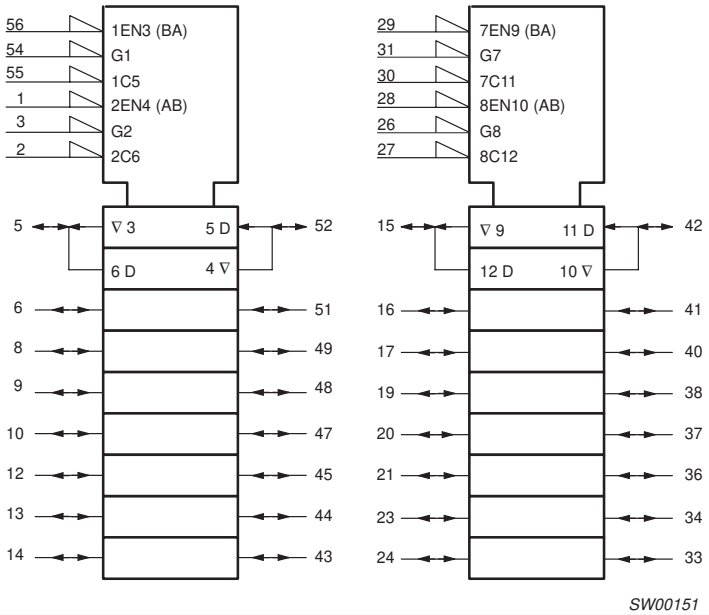
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL		UNIT
			2.5 V	3.3 V	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50 pF	1.8 2.7	1.6 1.8	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0 V or V_{CC}	3	3	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0 V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	μA

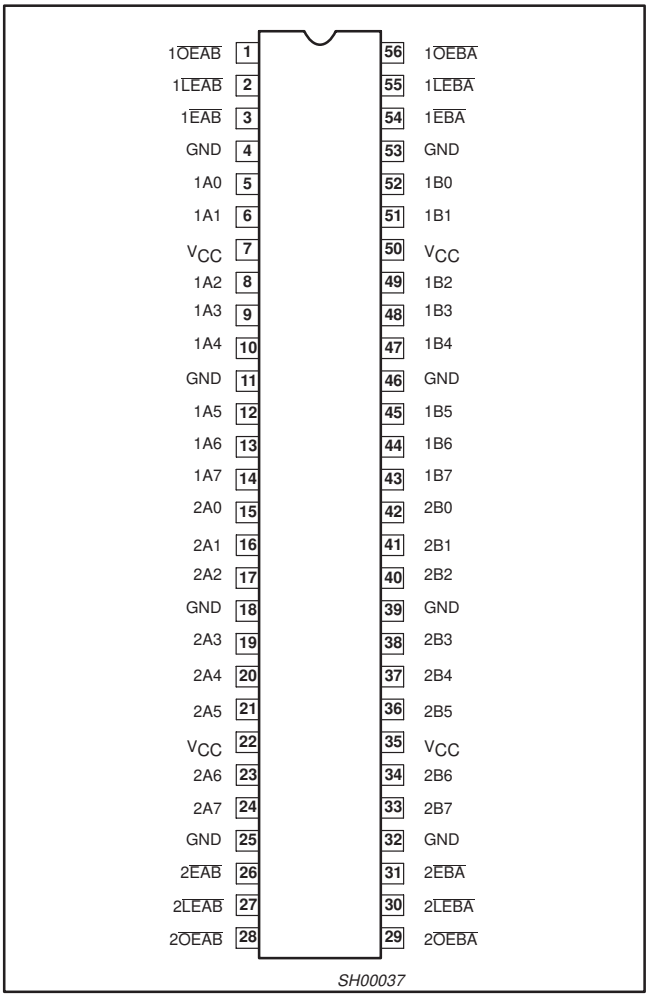
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	TYPE NUMBER	DWG NUMBER
56-Pin Plastic SSOP Type III	–40 °C to +85 °C	74ALVT16543DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40 °C to +85 °C	74ALVT16543DGG	SOT364-1

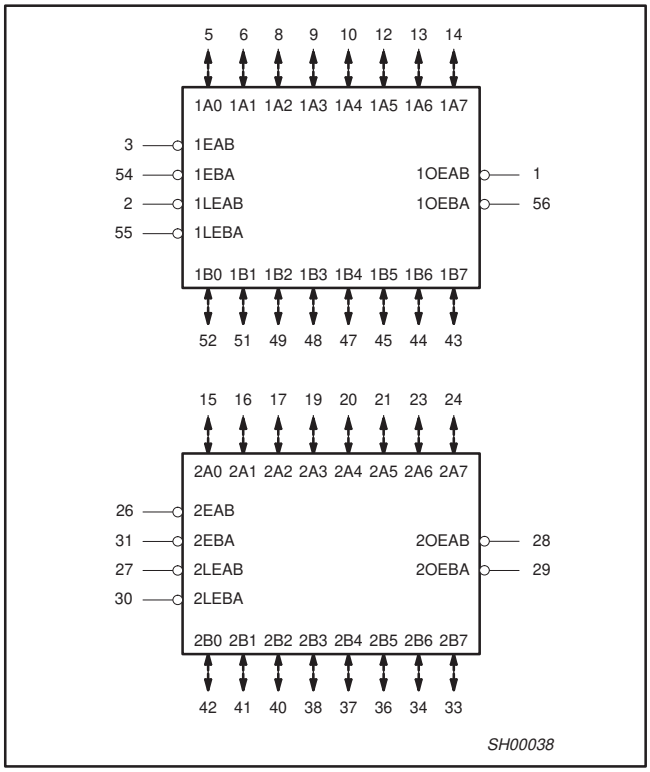
LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



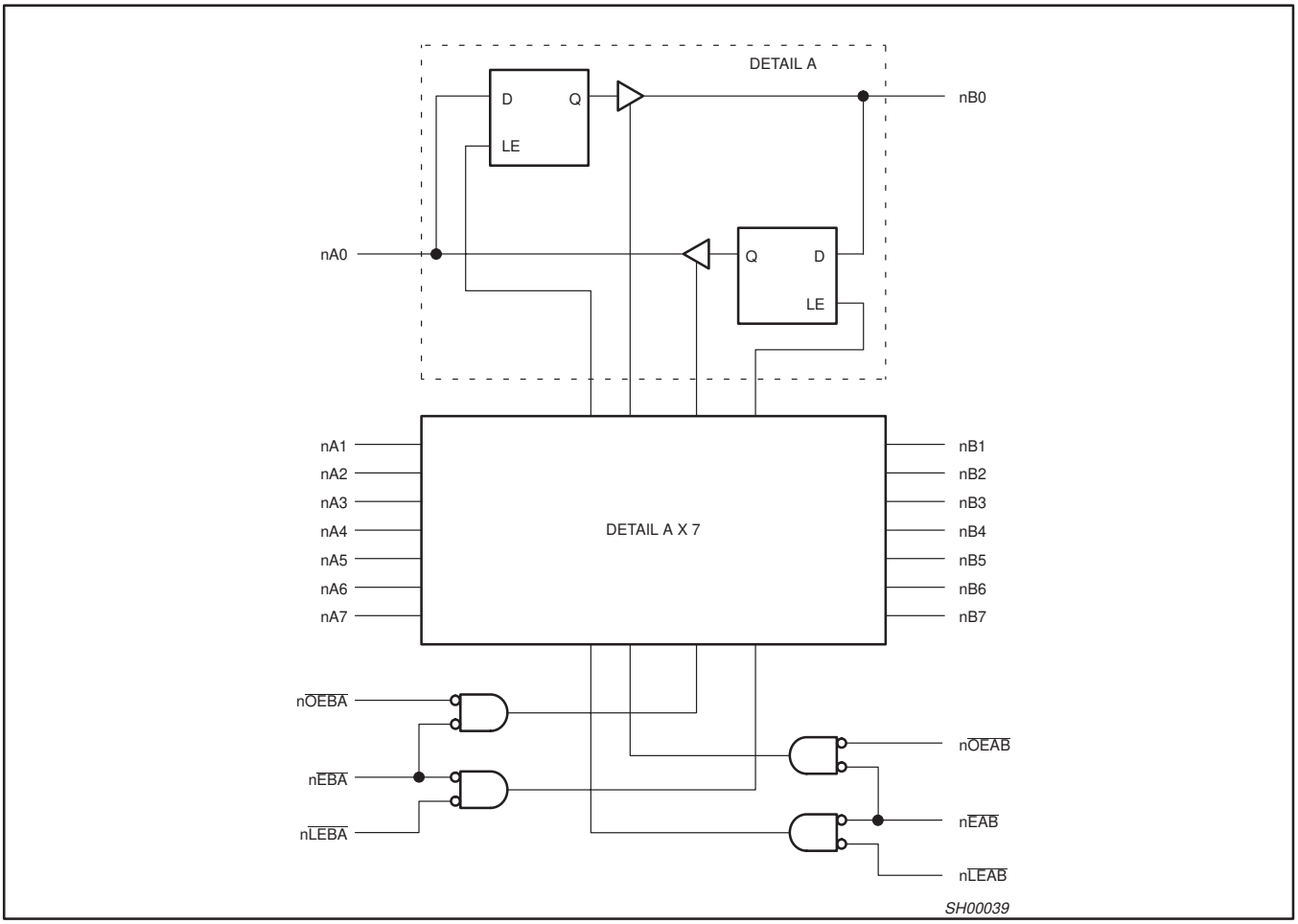
LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	A Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40,38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	B Data inputs/outputs
1, 56 28, 29	$1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$	A to B / B to A Output Enable inputs (active-LOW)
3, 54 26, 31	$1\overline{EAB}$, $1\overline{EBA}$, $2\overline{EAB}$, $2\overline{EBA}$	A to B / B to A Enable inputs (active-LOW)
2, 55 27, 30	$1\overline{LEAB}$, $1\overline{LEBA}$, $2\overline{LEAB}$, $2\overline{LEBA}$	A to B / B to A Latch Enable inputs (active-LOW)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0 V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$nOE\overline{XX}$	$nE\overline{XX}$	$nLE\overline{XX}$	nAx or nBx	nBx or nAx	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH transition of $nLE\overline{XX}$ or $nE\overline{XX}$ (XX = AB or BA)
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH transition of $nLE\overline{XX}$ or $nE\overline{XX}$ (XX = AB or BA)
X = Don't care
↑ = LOW-to-HIGH transition of $nLE\overline{XX}$ or $nE\overline{XX}$ (XX = AB or BA)
NC = No change
Z = High-impedance or "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$ V	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$ V	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or HIGH state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in LOW state	128	mA
		Output in HIGH state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5 V RANGE LIMITS		3.3 V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	HIGH-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	HIGH-level output current		–8		–32	mA
I_{OL}	LOW-level output current		8		32	mA
	LOW-level output current; current duty cycle ≤ 50 %; f ≥ 1 kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3 V ± 0.3 V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = –40 °C to +85 °C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0 V; I_{IK} = –18 mA		–	–0.85	–1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 3.0 V to 3.6 V; I_{OH} = –100 µA		V_{CC} – 0.2	V_{CC}	–	V
		V_{CC} = 3.0 V; I_{OH} = –32 mA		2.0	2.3	–	
V_{OL}	LOW–level output voltage	V_{CC} = 3.0 V; I_{OL} = 100 µA		–	0.07	0.2	V
		V_{CC} = 3.0 V; I_{OL} = 16 mA		–	0.25	0.4	
		V_{CC} = 3.0 V; I_{OL} = 32 mA		–	0.3	0.5	
		V_{CC} = 3.0 V; I_{OL} = 64 mA		–	0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6 V; I_O = 1 mA; V_I = V_{CC} or GND		–	–	0.55	V
I_I	Input leakage current	V_{CC} = 3.6 V; V_I = V_{CC} or GND	Control pins	–	0.1	± 1	µA
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V		–	0.1	10	
		V_{CC} = 3.6 V; V_I = V_{CC}	Data pins[4]	–	0.5	1	
		V_{CC} = 3.6 V; V_I = 0 V		–	0.1	–5	
		V_{CC} = 3.6 V; V_I = 5.5 V		–	0.1	20	
I_{OFF}	Off current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V		–	0.1	± 100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3 V; V_I = 0.8 V		75	130	–	µA
		V_{CC} = 3 V; V_I = 2.0 V		–75	–140	–	
		V_{CC} = 0 V to 3.6 V; V_{CC} = 3.6 V		± 500	–	–	
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5 V; V_{CC} = 3.0 V		–	50	125	µA
$I_{PU/PD}$	Power-up/down 3-State output current[3]	$V_{CC} \leq$ 1.2 V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care		–	40	± 100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6 V; Outputs HIGH; V_I = GND or V_{CC}; I_O = 0 mA		–	0.07	0.1	mA
I_{CCL}		V_{CC} = 3.6 V; Outputs LOW; V_I = GND or V_{CC}; I_O = 0 mA		–	3.6	5	
I_{CCZ}		V_{CC} = 3.6 V; Outputs disabled; V_I = GND or V_{CC}, I_O = 0 mA[5]		–	0.07	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3 V to 3.6 V; One input at V_{CC} – 0.6 V; Other inputs at V_{CC} or GND		–	0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
3. This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 msec. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µsec is permitted. This parameter is valid for T_{amb} = 25 °C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

DC ELECTRICAL CHARACTERISTICS (2.5 V ± 0.2 V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = –40 °C to +85 °C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3 V; I_{IK} = –18 mA		–	–0.85	–1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 2.3 V to 3.6 V; I_{OH} = –100 µA		V_{CC} – 0.2	V_{CC}	–	V
		V_{CC} = 2.3 V; I_{OH} = –8 mA		1.8	2.1	–	
V_{OL}	LOW-level output voltage	V_{CC} = 2.3 V; I_{OL} = 100 µA		–	0.07	0.2	V
		V_{CC} = 2.3 V; I_{OL} = 24 mA		–	0.3	0.5	
		V_{CC} = 2.3 V; I_{OL} = 8 mA		–	–	0.4	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7 V; I_O = 1 mA; V_I = V_{CC} or GND		–	–	0.55	V
I_I	Input leakage current	V_{CC} = 2.7 V; V_I = V_{CC} or GND	Control pins	–	0.1	± 1	µA
		V_{CC} = 0 V or 2.7 V; V_I = 5.5 V		–	0.1	10	
		V_{CC} = 2.7 V; V_I = 5.5 V	Data pins[4]	–	0.1	20	
		V_{CC} = 2.7 V; V_I = V_{CC}		–	0.1	10	
		V_{CC} = 2.7 V; V_I = 0 V		–	0.1	–5	
I_{OFF}	Off current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V		–	0.1	± 100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3 V; V_I = 0.7 V		–	120	–	µA
		V_{CC} = 2.3 V; V_I = 1.7 V		–	–6	–	
I_{EX}	Current into an output in the HIGH state when V_O > V_{CC}	V_O = 5.5 V; V_{CC} = 2.3 V		–	50	125	µA
$I_{PU/PD}$	Power-up/down 3-State output current[3]	$V_{CC} \leq$ 1.2 V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care		–	40	100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7 V; Outputs HIGH, V_I = GND or V_{CC}; I_O = 0 mA		–	0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7 V; Outputs LOW, V_I = GND or V_{CC}; I_O = 0 mA		–	2.6	4.5	
I_{CCZ}		V_{CC} = 2.7 V; Outputs disabled; V_I = GND or V_{CC}; $I_{O=}$ 0 mA[5]		–	0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3 V to 2.7 V; One input at V_{CC} – 0.6 V; Other inputs at V_{CC} or GND		–	0.01	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5 V and T_{amb} = 25 °C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
3. This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 msec. From V_{CC} = 1.2 V to V_{CC} = 2.5 V ± 0.2 V a transition time of 100 µsec is permitted. This parameter is valid for T_{amb} = 25 °C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (3.3 V ± 0.3 V RANGE)

GND = 0 V; $t_R = t_F$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; T_{amb} = –40 °C to +85 °C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3 V ± 0.3 V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	0.5 0.5	1.6 1.8	2.6 3.0	ns
t_{PLH} t_{PHL}	Propagation delay n$\overline{LEBA}$ to nAx, n$\overline{LEAB}$ to nBx	1 2	1.0 1.0	2.4 2.4	4.0 4.0	ns
t_{PZH} t_{PZL}	Output enable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx	4 5	1.0 1.0	2.3 1.8	4.0 3.1	ns
t_{PHZ} t_{PLZ}	Output disable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx	4 5	1.0 1.0	3.1 2.7	4.8 4.2	ns
t_{PZH} t_{PZL}	Output enable time n$\overline{EBA}$ to nAx, n$\overline{EAB}$ to nBx	4 5	1.0 1.0	2.5 1.9	4.2 3.1	ns
t_{PHZ} t_{PLZ}	Output disable time n$\overline{EBA}$ to nAx, n$\overline{EAB}$ to nBx	4 5	1.0 1.0	2.9 2.4	4.9 4.2	ns

NOTE:
1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

AC SETUP REQUIREMENTS (3.3 V ± 0.3 V RANGE)

GND = 0 V; $t_R = t_F$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; T_{amb} = –40 °C to +85 °C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 3.3 V ± 0.3 V		
			MIN	TYP	
t_s(H) t_s(L)	Setup time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$	3	0.5 0.7	0 –0.4	ns
t_h(H) t_h(L)	Hold time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$	3	1.5 1.5	0.2 –0.3	ns
t_s(H) t_s(L)	Setup time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$	3	0.5 1.1	–0.3 –0.6	ns
t_h(H) t_h(L)	Hold time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$	3	1.2 2.0	0.6 0.1	ns
t_W(L)	Latch enable pulse width, LOW	3	1.5	–	ns

AC CHARACTERISTICS (2.5 V ± 0.2 V RANGE)

GND = 0 V; $t_R = t_F$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; T_{amb} = –40 °C to +85 °C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5 V ± 0.2 V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	1.0 1.0	1.8 2.7	5.1 4.5	ns
t_{PLH} t_{PHL}	Propagation delay n$\overline{LEBA}$ to nAx, n$\overline{LEAB}$ to nBx	1 2	1.5 1.5	3.9 3.6	6.4 5.9	ns
t_{PZH} t_{PZL}	Output enable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx	4 5	1.5 1.5	4.0 2.7	6.5 4.6	ns
t_{PHZ} t_{PLZ}	Output disable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx	4 5	1.5 1.5	3.7 2.6	5.6 4.0	ns
t_{PZH} t_{PZL}	Output enable time n$\overline{EBA}$ to nAx, n$\overline{EAB}$ to nBx	4 5	1.5 1.5	4.2 2.8	7.0 5.0	ns
t_{PHZ} t_{PLZ}	Output disable time n$\overline{EBA}$ to nAx, n$\overline{EAB}$ to nBx	4 5	1.5 1.5	3.6 2.4	5.6 3.9	ns

NOTE:
1. All typical values are at V_{CC} = 2.5 V and T_{amb} = 25 °C.

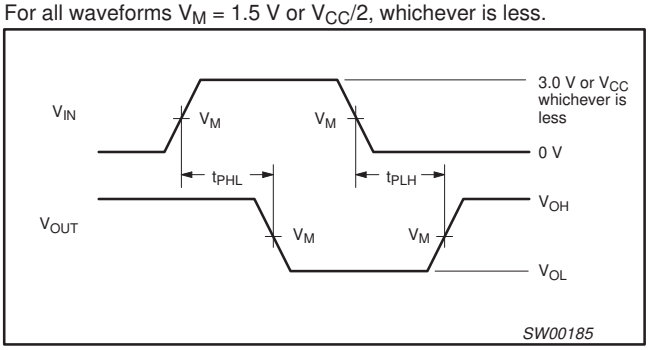
AC SETUP REQUIREMENTS (2.5 V ± 0.2 V RANGE)

GND = 0 V; $t_R = t_F$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; T_{amb} = –40 °C to +85 °C.

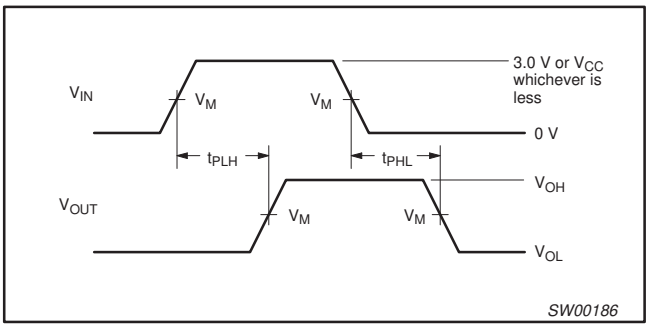
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 2.5 V ± 0.2 V		
			MIN	TYP	
t_s(H) t_s(L)	Setup time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$	3	0.5 1.0	–0.2 –0.5	ns
t_h(H) t_h(L)	Hold time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$	3	1.0 1.0	0.2 –0.2	ns
t_s(H) t_s(L)	Setup time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$	3	0.5 1.5	–0.3 –0.6	ns
t_h(H) t_h(L)	Hold time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$	3	1.2 1.5	0 0.2	ns
t_W(L)	Latch enable pulse width, LOW	3	1.5	–	ns

AC WAVEFORMS

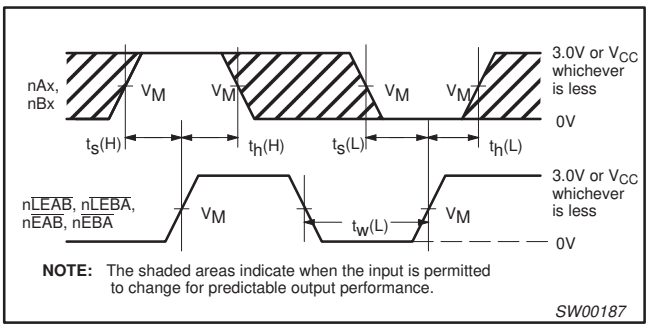
For all waveforms V_M = 1.5 V or V_{CC}/2, whichever is less.



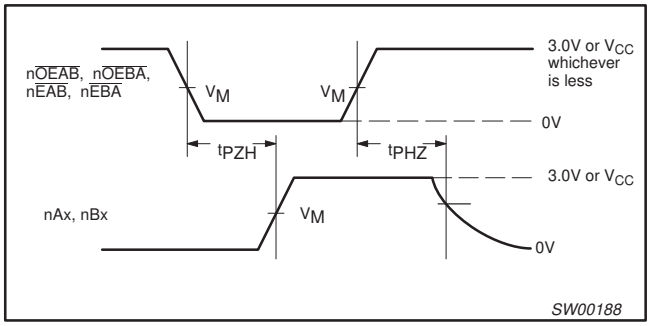
Waveform 1. Propagation Delay For Inverting Output



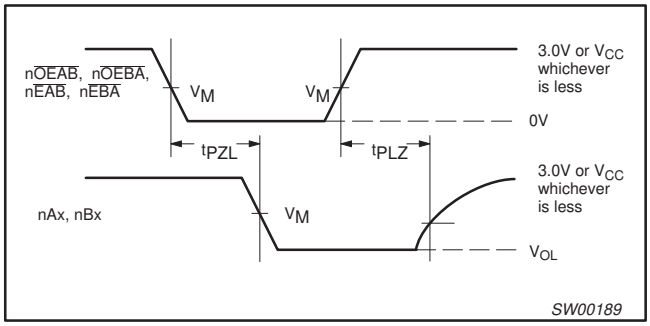
Waveform 2. Propagation Delay For Non-Inverting Output



Waveform 3. Data Setup and Hold Times and Latch Enable Pulse Width

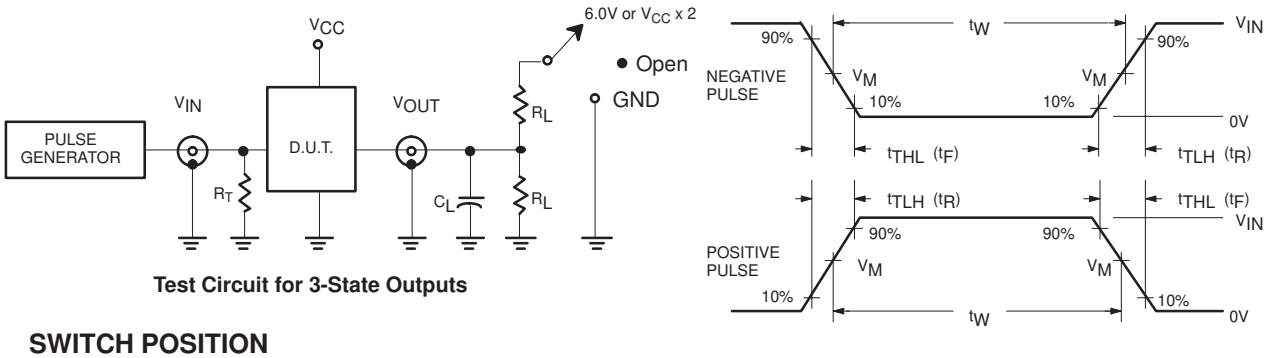


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or $V_{CC\ x\ 2}$
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

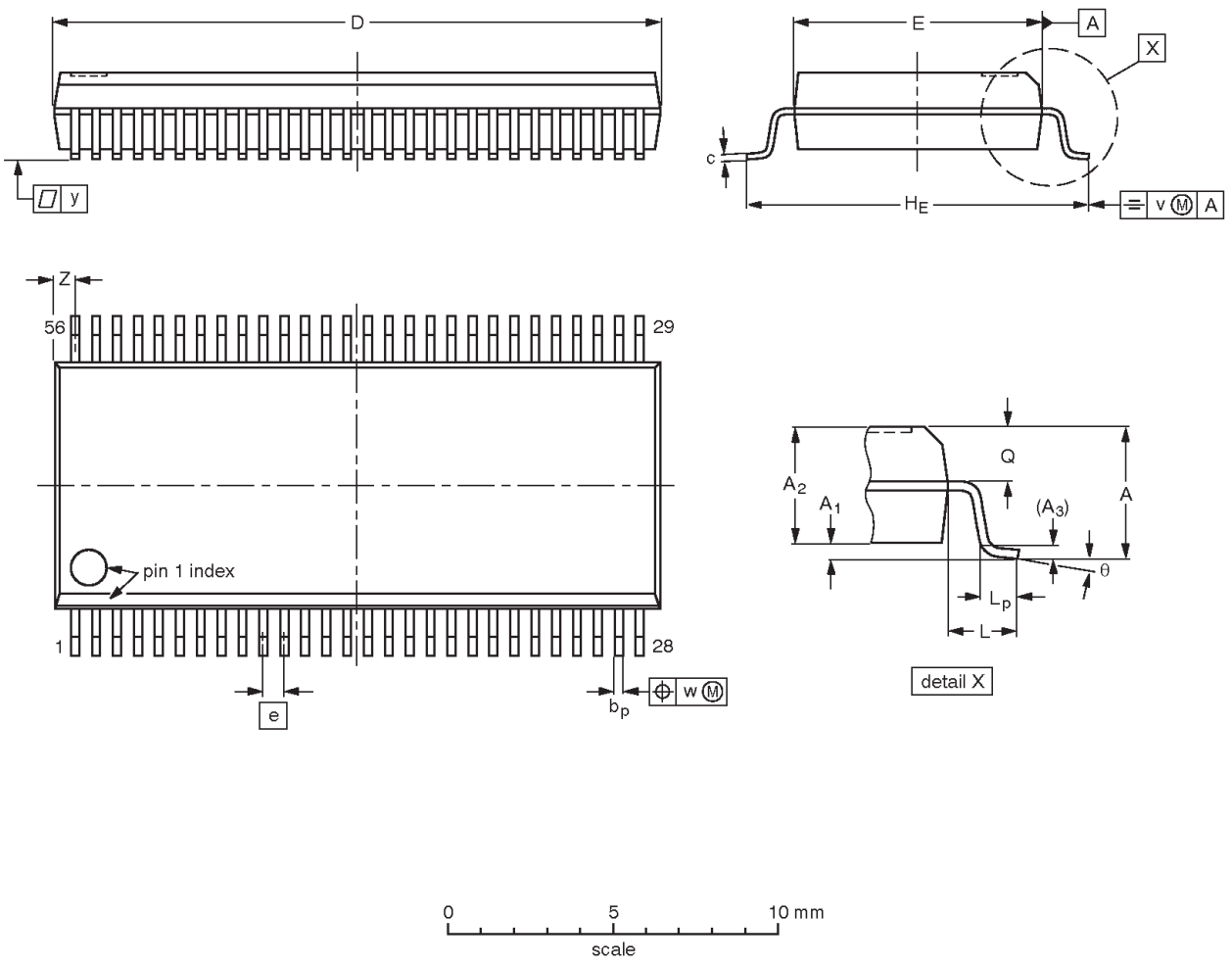
C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SW00025

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

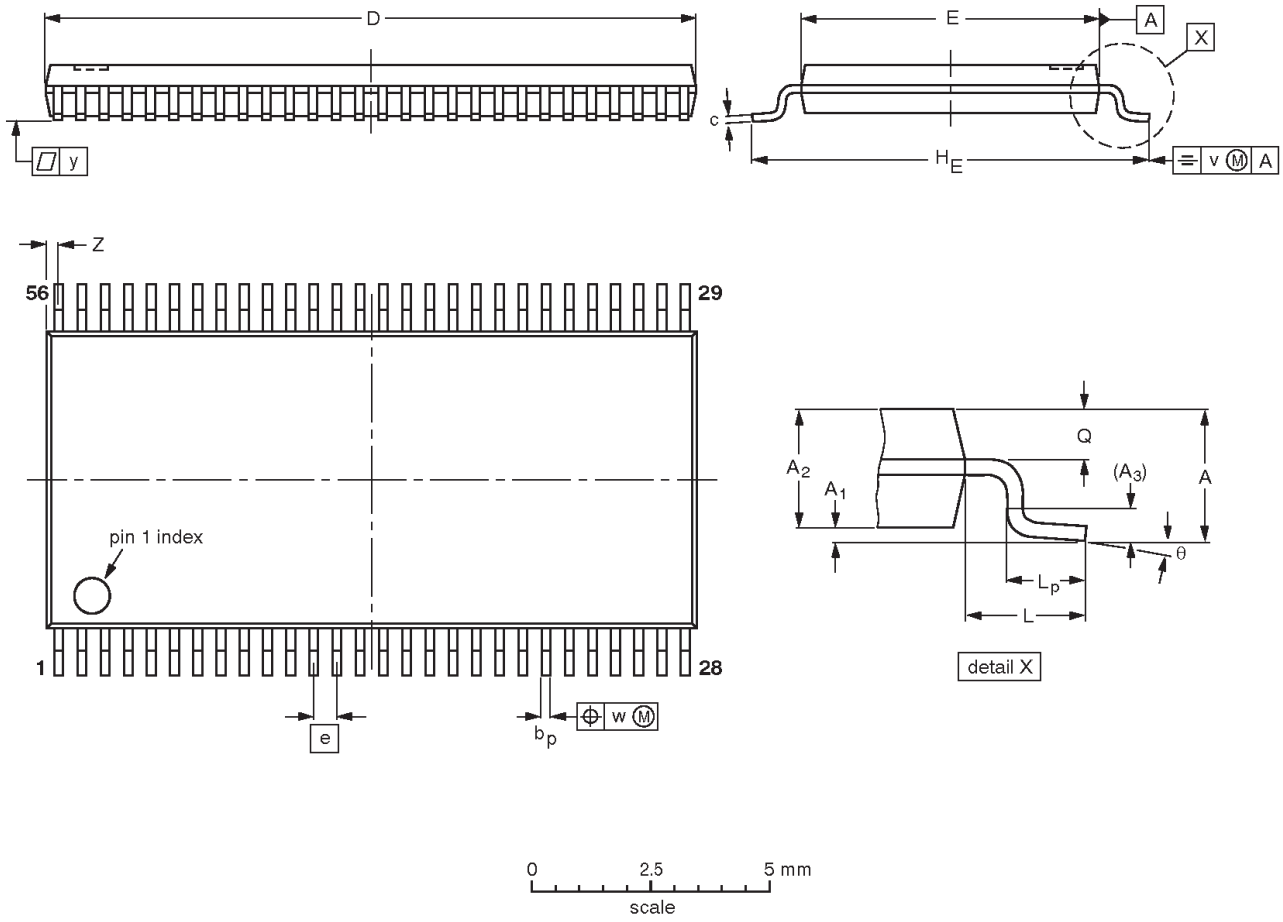
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT371-1		MO-118				~~99-12-27~~ 03-02-18

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

REVISION HISTORY

Rev	Date	Description
_3	20040914	**Product data sheet (9397 750 14059). Supersedes data of 1998 Feb 13 (9397 750 03568).** Modifications: • Ordering information table on page 2: – remove “North America” column; rename third column from “Outside North America” to “Type Number”. • DC Electrical Characteristics (3.3 V ± 0.3 V range) table on page 6: – I_I on Data pins: add condition ‘V_{CC} = 3.6 V; V_I = 5.5 V’ and values 0.1 μA (typ) and 20 μA (max). • AC Characteristics (3.3 V ± 0.3 V range) table on page 8: – change propagation delay nAx to nBx t_{PLH} Max. time from 2.5 ns to 2.6 ns – change output disable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx t_{PHZ} (Max.) time from 4.7 ns to 4.8 ns – change output disable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx t_{PLZ} (Max.) time from 4.0 ns to 4.2 ns – change output disable time n$\overline{EBA}$ to nAx, n$\overline{EAB}$ to nBx t_{PHZ} (Max.) time from 4.5 ns to 4.9 ns – change output disable time n$\overline{EBA}$ to nAx, n$\overline{EAB}$ to nBx t_{PLZ} (Max.) time from 3.8 ns to 4.2 ns • AC Setup Requirements (3.3 V ± 0.3 V range) table on page 8: – change setup time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$ t_s(H) (Min.) from 0.0 ns to 0.5 ns; (Typ.) from –0.8 ns to 0 ns – change setup time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$ t_s(L) (Typ.) from –0.3 ns to –0.4 ns – change hold time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$ t_h(H) (Typ.) from 0.4 ns to 0.2 ns – change hold time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$ t_h(L) (Typ.) from 0.8 ns to –0.3 ns – change setup time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$ t_s(H) (Typ.) from –0.8 ns to –0.3 ns – change setup time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$ t_s(L) (Typ.) from –0.2 ns to –0.6 ns – change hold time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$ t_h(H) (Typ.) from 0.3 ns to 0.6 ns – change hold time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$ t_h(L) (Typ.) from 1.1 ns to 0.1 ns • AC Setup Requirements (2.5 V ± 0.2 V range) table on page 9: – change setup time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$ t_s(H) (Min.) from 0 ns to 0.5 ns; (Typ.) from –0.9 ns to –0.2 ns – change setup time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$ t_s(L) (Typ.) from 0.2 ns to –0.5 ns – change hold time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$ t_h(H) (Min.) from 0.8 ns to 1.0 ns; (Typ.) from –0.2 ns to 0.2 ns – change hold time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$ t_h(L) (Min.) from 1.7 ns to 1.0 ns; (Typ.) from 1.0 ns to –0.2 ns – change setup time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$ t_s(H) (Min.) from 0 ns to 0.5 ns; (Typ.) from –1.0 ns to –0.3 ns – change setup time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$ t_s(L) (Typ.) from 0.4 ns to –0.6 ns – change hold time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$ t_h(H) (Min.) from 0.5 ns to 1.2 ns; (Typ.) from 0.2 ns to 0 ns – change hold time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$ t_h(L) (Min.) from 2.0 ns to 1.5 ns; (Typ.) from 1.3 ns to 0.2 ns
_2	19980213	**Product specification (9397 750 03568). ECN 853-1823 18958 of 13 February 1998. Supersedes data of 1995 Dec 21.**
_1	19951221	

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
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Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

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