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FAIRCHILD SEMICONDUCTOR®

September 2012

74AUP1G59 TinyLogic® Low Power Universal Configurable Two-Input Logic Gate (Open Drain Output)

Features

- 0.8V to 3.6V V_{CC} Supply Operation
- 3.6V Over-Voltage Tolerant I/Os at V_{CC} from 0.8V to 3.6V
- Extremely High Speed t_{PD}
  - 3.2ns: Typical at 3.3V
- Power-Off High-Impedance Inputs and Outputs
- Low Static Power Consumption
  - I_{CC}=0.9µA Maximum
- Low Dynamic Power Consumption
  - C_{PD}=3.0pF Typical at 3.3V
- Ultra-Small MicroPak™ Package

Description

The 74AUP1G59 is a universal, configurable, two-input logic gate with an open drain that provides a high-performance and low-power solution for battery-powered portable applications. This product is designed for a wide low voltage operating range (0.8 V to 3.6 V) and guarantees very low static and dynamic power consumption across the entire voltage range. All inputs are implemented with hysteresis to allow for slower transition input signals and better switching noise immunity.

The 74AUP1G59 provides for multiple functions, as determined by various configurations of the three inputs. The potential logic functions provided are AND, NAND, OR, NOR, XNOR, inverter, and buffer *(see Figure 2 through Figure 8)*.

Ordering Information

Part Number	Top Mark	Package	Packing Method
74AUP1G59L6X	AL	6-Lead, MicroPak™, 1.0 mm Wide	5000 Units on Tape & Reel
74AUP1G59FHX	AL	6-Lead, MicroPak2™, 1x1 mm Body, .35 mm Pitch	5000 Units on Tape & Reel

Pin Configurations

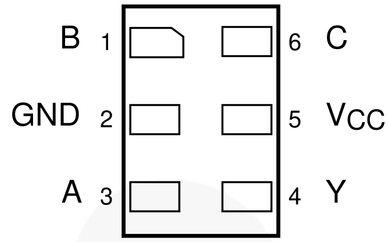


Figure 1. MicroPak™ (Top Through View)

Pin Definitions

Pin #	Name	Description
1	B	Data Input
2	GND	Ground
3	A	Data Input
4	Y	Output (Open Drain)
5	V_{CC}	Supply Voltage
6	C	Data Input

Function Table

Inputs			Y=Output
C	**B**	**A**	
L	L	L	L
L	L	H	H(1)
L	H	L	L
L	H	H	H(1)
H	L	L	H(1)
H	L	H	H(1)
H	H	L	L
H	H	H	L

H = HIGH Logic Level

L = LOW Logic Level

Note:

1. High impedance output state, open drain.

Function Selection Table

2-Input Logic Function	Connection Configuration
2-Input AND with Inverted Input	Figure 3, Figure 4
2-Input NAND	Figure 2
2-Input NAND with Both Inputs Inverted	Figure 5
2-Input OR	Figure 5
2-Input OR Both Inputs Inverted	Figure 2
2-Input NOR with Inverted Input	Figure 3, Figure 4
2-Input XNOR	Figure 6
Inverter	Figure 7
Buffer	Figure 8

Logic Configurations

Figure 2 through Figure 8 show the logical functions that can be implemented using the 74AUP1G59. The diagrams show the DeMorgan's equivalent logic duals for a given two-input function. The logical implementation is next to the board-level physical implementation of how the pins should be connected.

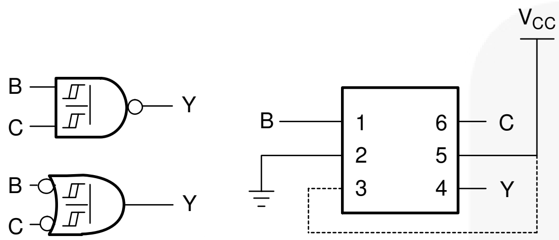


Figure 2. 2-Input NAND Gate or 2-Input OR with Both Inputs Inverted

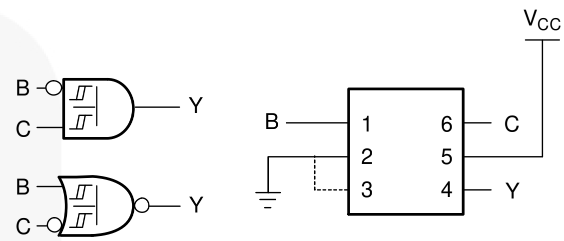


Figure 3. 2-Input AND with Inverted B Input or 2-Input NOR Gate with Inverted C Input

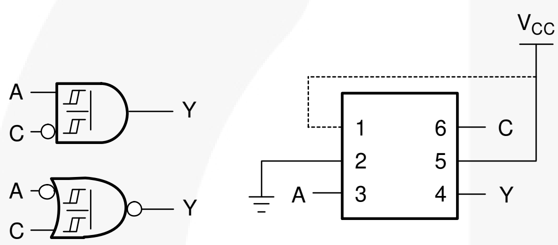


Figure 4. 2-Input AND with Inverted C Input or 2-Input NOR Gate with Inverted A Input

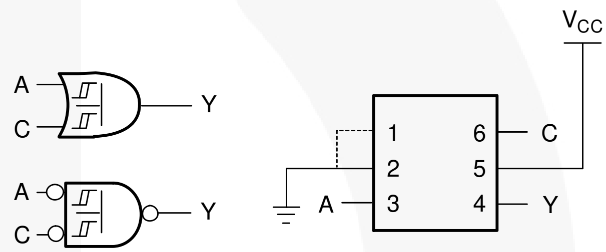


Figure 5. 2-Input OR Gate or 2-Input NAND Gate with Both Inputs Inverted

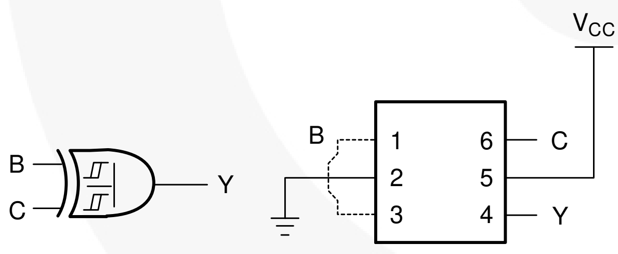


Figure 6. 2-Input XOR Gate

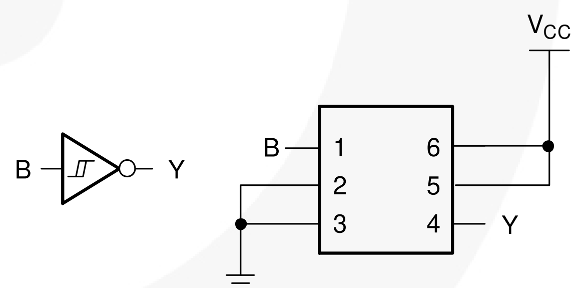


Figure 7. Inverter

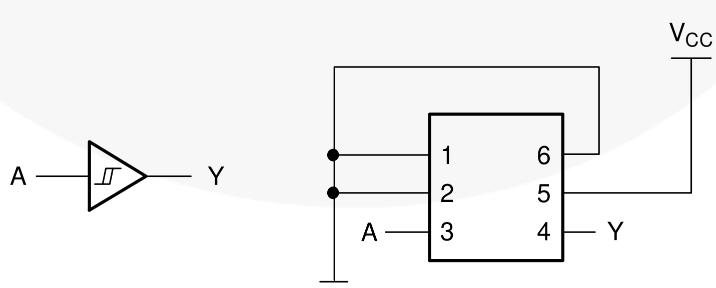


Figure 8. Buffer

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	4.6	V
V_{IN}	DC Input Voltage		-0.5	4.6	V
V_{OUT}[2]	DC Output Voltage		-0.5	4.6	V
I_{IK}	DC Input Diode Current	$V_{IN} < 0V$		-50	mA
I_{OK}	DC Output Diode Current	$V_{OUT} < 0V$		-50	mA
I_{OL}	DC Output Sink Current			+50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Supply Pin			±50	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature Under Bias			+150	°C
T_L	Junction Lead Temperature, Soldering 10s			+260	°C
P_D	Power Dissipation at +85°C	MicroPak™-6		130	mW
		MicroPak2™-6		120	
ESD	Human Body Model, JEDEC:JESD22-A114			5000	V
	Charged Device Model, JEDEC:JESD22-C101			2000	

Note:
2. I_O absolute maximum rating must be observed.

Recommended Operating Conditions[3]

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{CC}	Supply Voltage		0.8	3.6	V
V_{IN}	Input Voltage		0	3.6	V
V_{OUT}	Output Voltage		0	3.6	V
I_{OL}	Output Current	V_{CC}=3.0V to 3.6V		4.0	mA
		V_{CC}=2.3V to 2.7V		3.1	
		V_{CC}=1.65V to 1.95V		1.9	
		V_{CC}=1.4V to 1.6V		1.7	
		V_{CC}=1.1V to 1.3V		1.1	
		V_{CC}=0.8V		20.0	µA
T_A	Operating Temperature, Free Air		-40	+85	°C
θ_{JA}	Thermal Resistance	MicroPak™-6		500	°C/W
		MicroPak2™-6		560	

Note:
3. Unused inputs must be held HIGH or LOW. They may not float.

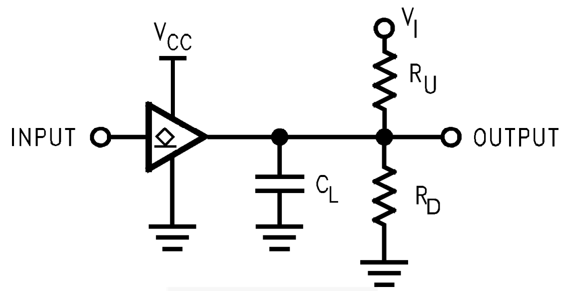
DC Electrical Characteristics

Symbol	Parameter	V_{CC}	Condition	T_A=25°C		T_A=-40 to 85°C		Unit
				Min.	Max.	Min.	Max.	
V_P	Positive Threshold Voltage	0.80		0.30	0.60	0.30	0.60	V
		1.10		0.53	0.90	0.53	0.90	
		1.40		0.74	1.11	0.74	1.11	
		1.65		0.91	1.29	0.91	1.29	
		2.30		1.37	1.77	1.37	1.77	
		3.00		1.88	2.29	1.88	2.29	
V_N	Negative Threshold Voltage	0.80		0.10	0.60	0.10	0.60	V
		1.10		0.26	0.65	0.26	0.65	
		1.40		0.39	0.75	0.39	0.75	
		1.65		0.47	0.84	0.47	0.84	
		2.30		0.69	1.04	0.69	1.04	
		3.00		0.88	1.24	0.88	1.24	
V_H	Hysteresis Voltage	0.80		0.07	0.50	0.07	0.50	V
		1.10		0.08	0.46	0.08	0.46	
		1.40		0.18	0.56	0.18	0.56	
		1.65		0.27	0.66	0.27	0.66	
		2.30		0.53	0.92	0.53	0.92	
		3.00		0.79	1.31	0.79	1.31	
V_{OL}	LOW Level Output Voltage	$0.80 \le V_{CC} \le 3.60$	I_{OL}=20 µA		0.10		0.10	V
		$1.10 \le V_{CC} \le 1.30$	I_{OL}=1.1 mA		0.30 x V_{CC}		0.30 x V_{CC}	
		$1.40 \le V_{CC} \le 1.60$	I_{OL}=1.7 mA		0.31		0.37	
		$1.65 \le V_{CC} \le 1.95$	I_{OL}=1.9 mA		0.31		0.35	
		$2.30 \le V_{CC} \le 2.70$	I_{OL}=3.1 mA		0.44		0.45	
		$2.70 \le V_{CC} \le 3.60$	I_{OL}=4.0 mA		0.44		0.45	
I_{IN}	Input Leakage Current	0V to 3.6 V	$0 \le V_{IN} \le 3.6$ V		±0.1		±0.5	µA
I_{OFF}	Power Off Leakage Current	0V	$0 \le (V_{IN},V_O) \le 3.6$ V		0.2		0.6	µA
ΔI_{OFF}	Additional Power Off Leakage Current	0V to 0.2 V	V_{IN} or V_O=0 V to 3.6 V		0.2		0.6	µA
I_{CC}	Quiescent Supply Current	0.8V to 3.6 V	V_{IN} - V_{CC} or GND		0.5		0.9	µA
			$V_{CC} \le V_{IN} \le 3.6$ V				±0.9	
ΔI_{CC}	Increase in I_{CC} per Input	3.3 V	$V_{IN}=V_{CC}$ -0.6 V		40.0		50.0	µA

AC Electrical Characteristics

Symbol	Parameter	V_{CC}	Condition	T_A=25°C			T_A=-40 to 85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	
t_{PZL}, t_{PLZ}	Propagation Delay	0.80	C_L=15 pF, R_U=R_D=5 KΩ V_I = 2 x (V_{CC}) *(see Figure 9)*		30				
		$1.10 \leq V_{CC} \leq 1.30$		1.0	10.1	18.9	1.0	19.9	
		$1.40 \leq V_{CC} \leq 1.60$		1.0	6.6	11.4	1.0	12.2	
		$1.65 \leq V_{CC} \leq 1.95$		1.0	6.3	8.7	1.0	9.7	
		$2.30 \leq V_{CC} \leq 2.70$		1.0	4.7	6.9	1.0	7.5	
		$3.00 \leq V_{CC} \leq 3.60$		1.0	4.6	6.8	1.0	7.4	
C_{IN}	Input Capacitance	0			0.8				pF
C_{OUT}	Output Capacitance	0			1.7				pF
C_{PD}	Power Dissipation Capacitance	0.80	V_{IN}=0V or V_{CC}, f=10 MHz		3.0				pF
		$1.10 \leq V_{CC} \leq 1.30$			3.1				
		$1.40 \leq V_{CC} \leq 1.60$			3.2				
		$1.65 \leq V_{CC} \leq 1.95$			3.4				
		$2.30 \leq V_{CC} \leq 2.70$			3.8				
		$3.00 \leq V_{CC} \leq 3.60$			4.4				

AC Loadings and Waveforms



Notes:
4. C_L includes load and stray capacitance.
5. Input PRR = 1.0 MHz, t_W = 500 ns.

Figure 9. AC Test Circuit

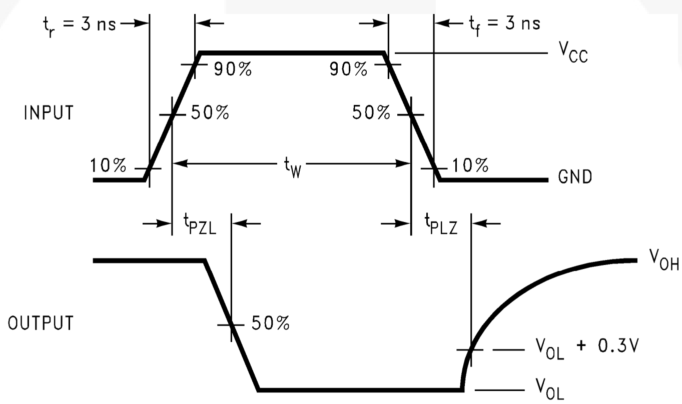
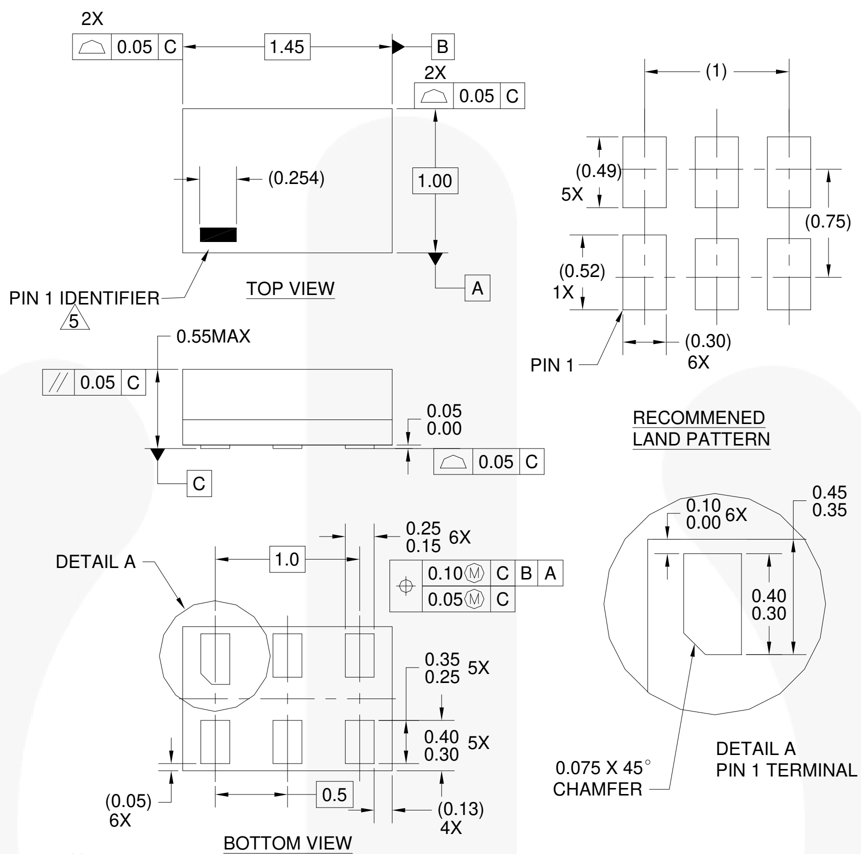


Figure 10. AC Waveforms

Symbol	V_{CC}					
	3.3 V ± 0.3 V	2.5 V ± 0.2 V	1.8 V ± 0.15 V	1.5 V ± 0.10 V	1.2 V ± 0.10 V	0.8 V
V_{mi}	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_X	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V	V_{OL} + 0.1 V	V_{OL} + 0.1 V	V_{OL} + 0.1 V

Physical Dimensions



Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994
4. FILENAME AND REVISION: MAC06AREV4
5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

Figure 11. 6-Lead MicroPak™ 1.0 x 1.45 mm, JEDEC MO-252

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Tape and Reel Specifications

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Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions

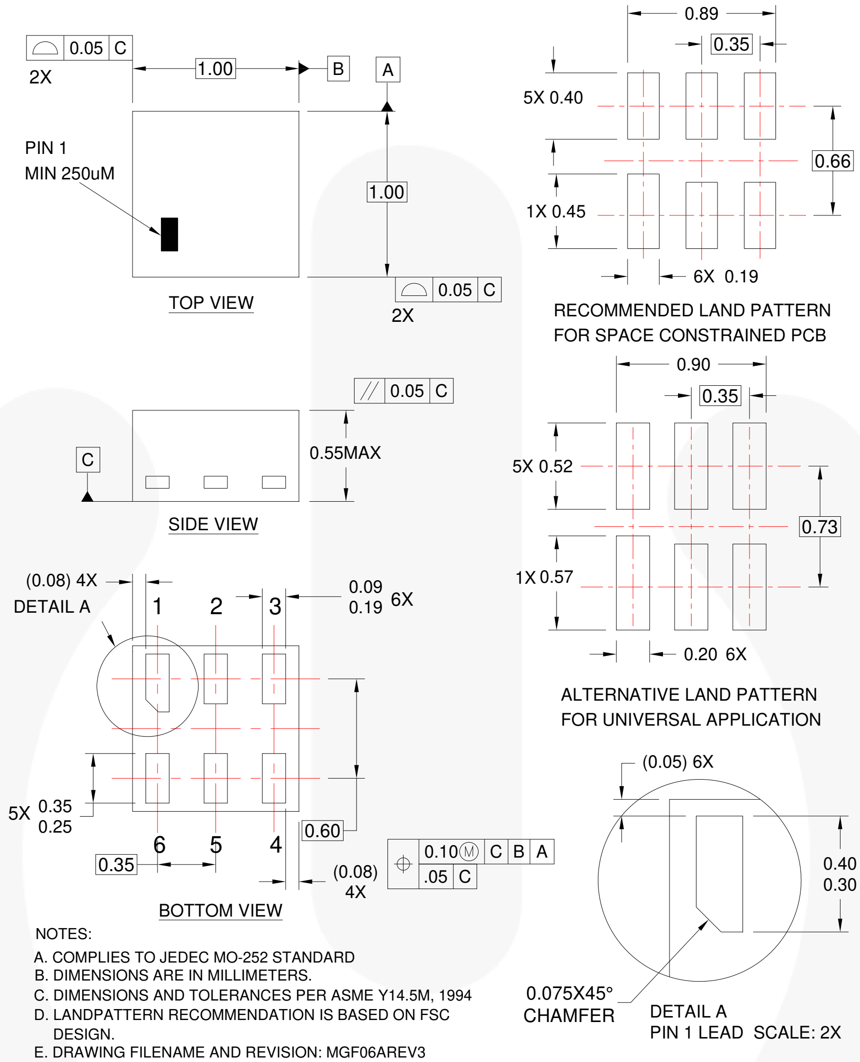

Figure 12.6-Lead, MicroPak2™, 1x1 mm Body, .35 mm Pitch

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Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: *http://www.fairchildsemi.com/packaging/MicroPAK2_6L_tr.pdf*.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

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Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I62

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