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10-bit level-shifting bus switch with output enable

Rev. 4 — 14 December 2011

Product data sheet

1. General description

The 74CBTLVD3861 is a 10-bit 3.3 V to 1.8 V level translating bus switch with one output enable (\overline{OE}) input. When \overline{OE} is LOW, the switch is closed and port A is connected to the B port. When \overline{OE} is HIGH, the switch is disabled.

To ensure the high-impedance OFF-state during power-up or power-down, \overline{OE} should be tied to the V_{CC} through a pull-up resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

Schmitt trigger action at control input makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 3.0 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF}.

2. Features and benefits

- Supply voltage range from 3.0 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-B/JESD36 (3.0 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - CDM AEC-Q100-011 revision B exceeds 1000 V
- 4 Ω switch connection between two ports
- 3.3 V to 1.8 V level translation
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



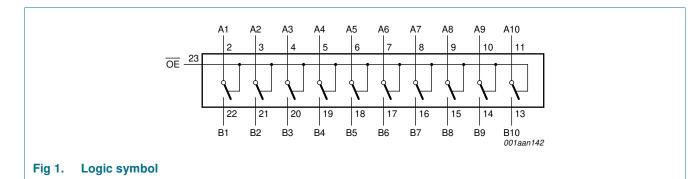
10-bit level-shifting bus switch with output enable

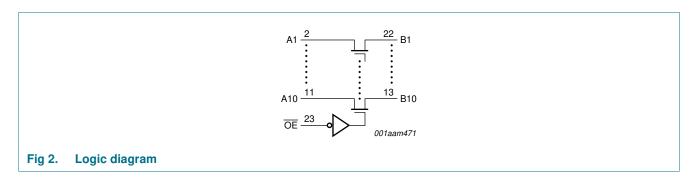
3. Ordering information

Table 1. Ordering	information			
Type number	Package			
	Temperature range	Name	Description	Version
74CBTLVD3861DK	-40 °C to +125 °C	SSOP24[1]	plastic shrink small outline package; 24 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT556-1
74CBTLVD3861PW	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74CBTLVD3861BQ	–40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body $3.5 \times 5.5 \times 0.85$ mm	SOT815-1

[1] Also known as QSOP24 package

4. Functional diagram

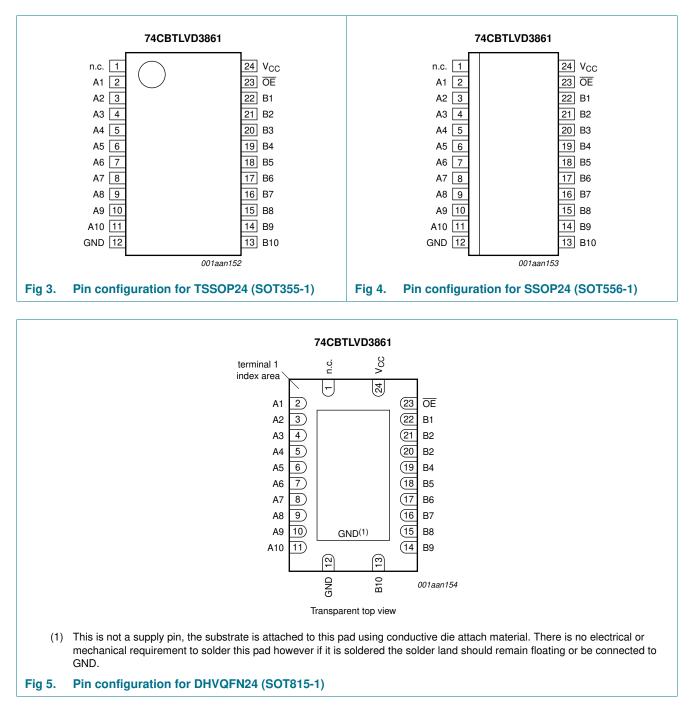




10-bit level-shifting bus switch with output enable

5. Pinning information

5.1 Pinning



10-bit level-shifting bus switch with output enable

5.2 Pin description

Table 2.	Pin description	
Symbol	Pin	Description
nc	1	not connected
A1 to A10	2, 3, 4, 5, 6, 7, 8, 9, 10, 1	data input/output (A port)
GND	12	ground (0 V)
B1 to B10	22, 21, 20, 19, 18, 17, 16,	15, 14, 13 data input/output (B port)
OE	23	output enable input (active LOW)
V _{CC}	24	positive supply voltage

6. Functional description

Table 3. Function selection^[1]

Input OE	Input/output
OE	An, Bn
L	An = Bn
Н	Z

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

7. Limiting values

Table 4.Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
VI	input voltage		<u>[1]</u> –0.5	+4.6	V
V _{SW}	switch voltage	enable and disable mode	<u>[1]</u> –0.5	$V_{CC} + 0.5$	V
I _{IK}	input clamping current	$V_{I} < -0.5 V$	-50	-	mA
I _{SK}	switch clamping current	$V_{I} < -0.5 V$	-50	-	mA
I _{SW}	switch current	$V_{SW} = 0 V \text{ to } V_{CC}$	-	±128	mA
I _{CC}	supply current		-	+100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 \ ^{\circ}C \ to \ +125 \ ^{\circ}C$	<u>[2]</u> _	500	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SSOP24 and TSSOP24 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C. For DHVQFN24 package: P_{tot} derates linearly at 4.5 mW/K above 60 °C.

10-bit level-shifting bus switch with output enable

8. Recommended operating conditions

Table 5.	Recommended operating condition	ons			
Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		3.0	3.6	V
VI	input voltage		0	3.6	V
V _{SW}	switch voltage	enable and disable mode	0	V_{CC}	V
T _{amb}	ambient temperature		-40	+125	°C
$\Delta t / \Delta V$	input transition rise and fall rate	$V_{CC} = 3.0 \text{ V} \text{ to } 3.6 \text{ V}$	<u>[1]</u> _	200	ns/V

[1] Applies to control signal levels.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

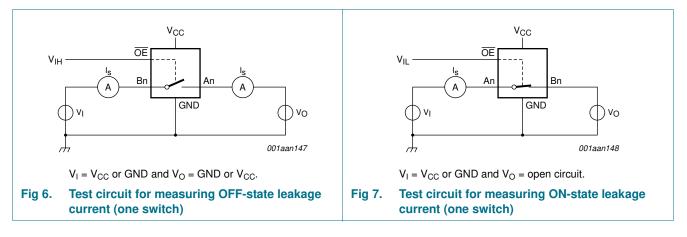
Symbol	Parameter	Conditions	Ta	mb = ·	–40 °C to -	⊦85 °C	T _{amb} = -40 °C	to +125 °C	Unit
			N	lin	Typ <mark>[1]</mark>	Max	Min	Max	1
V _{IH}	HIGH-level input voltage	$V_{CC} = 3.0 V \text{ to } 3.6 V$	2	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V_{CC} = 3.0 V to 3.6 V		-	-	0.9	-	0.9	V
lı	input leakage current	pin \overline{OE} ; V _I = GND to V _{CC} ; V _{CC} = 3.6 V		-	-	±1	-	±20	μA
V _{pass}	pass voltage	$V_I = V_{CC}$; see <u>Figure 8</u> to <u>Figure 12</u>		-	-	-	-	-	V
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 3.6 V$; see Figure 6		-	-	±1	-	±20	μA
I _{S(ON)}	ON-state leakage current	$V_{CC} = 3.6 V$; see Figure 7		-	-	±1	-	±20	μA
I _{OFF}	power-off leakage current	$V_1 \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V}$		-	-	±10	-	±50	μA
I _{CC}	supply current	$\label{eq:VI} \begin{array}{l} V_{I} = V_{CC}; I_{O} = 0 \; A; V_{CC} = 3.6 \; V; \\ V_{SW} = GND \; or \; V_{CC} \end{array}$		-	-	20	-	50	μA
				-	-	100	-	150	μA
ΔI _{CC}	additional supply current	pin \overline{OE} ; V ₁ = V _{CC} - 0.6 V; V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V	[2]	-	-	300	-	2000	μA
CI	input capacitance	pin \overline{OE} ; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V		-	0.9	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance	V_{CC} = 3.3 V; V_{I} = 0 V to 3.3 V		-	2.5	-	-	-	pF
C _{S(ON)}	ON-state capacitance	V_{CC} = 3.3 V; V_{I} = 0 V to 3.3 V		-	9.0	-	-	-	pF

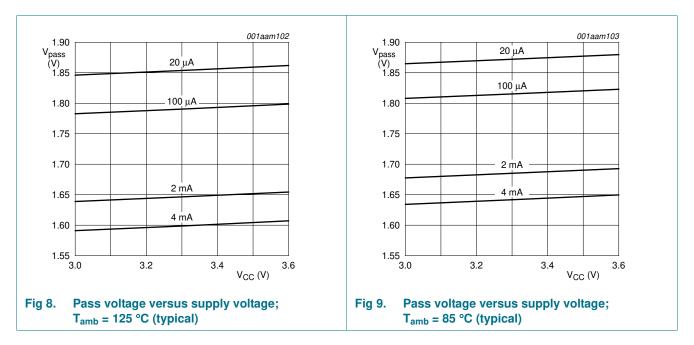
[1] All typical values are measured at $T_{amb} = 25$ °C.

[2] One input at 3 V, other inputs at V_{CC} or GND.

10-bit level-shifting bus switch with output enable

9.1 Test circuits





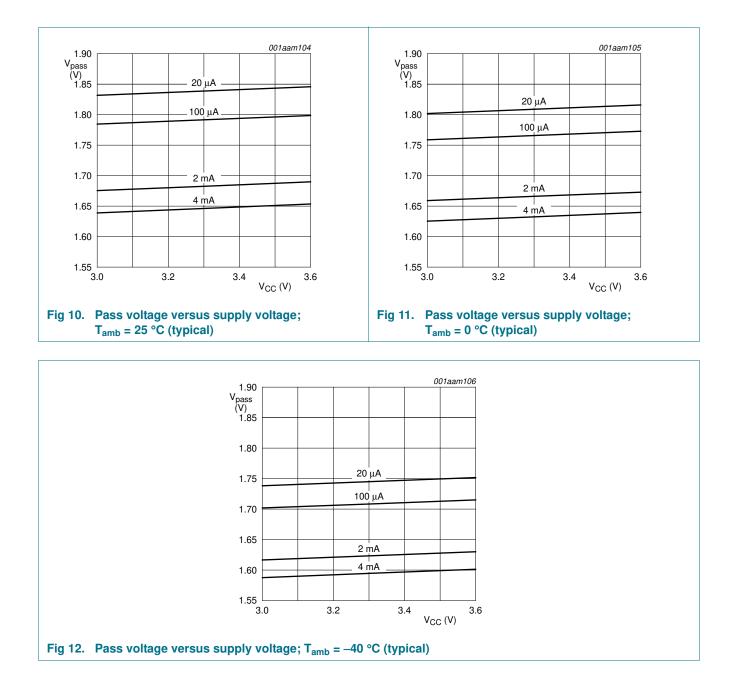
9.2 Typical pass voltage graphs

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9.3 ON resistance

Table 7. Resistance R_{ON}

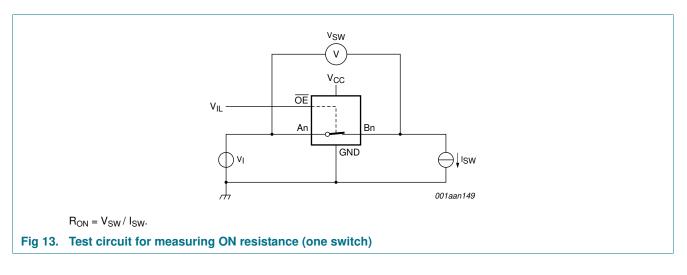
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 13.

Symbol	ymbol Parameter Conditions		T _{amb} =	–40 °C to	+85 °C	T _{amb} = -40 °	Unit	
			Min	Typ <mark>[1]</mark>	Max	Min	Max	
R _{ON}	ON resistance	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ [2]						
		$I_{SW} = 64 \text{ mA}; V_I = 0 \text{ V}$	-	3.7	7.0	-	10.0	Ω
		$I_{SW} = 24 \text{ mA}; V_I = 0 \text{ V}$	-	3.7	7.0	-	10.0	Ω
		$I_{SW} = 15 \text{ mA}; V_{I} = 1.2 \text{ V}$	-	4.7	10.0	-	12.0	Ω

[1] Typical values are measured at T_{amb} = 25 °C and nominal $V_{CC}.$

[2] Measured by the voltage drop between the An and Bn terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (An or Bn) terminals.

9.4 ON resistance test circuit



10-bit level-shifting bus switch with output enable

10. Dynamic characteristics

Dynamic characteristics Table 8.

GND = 0 V; for test circuit see Figure 16

Symbol	Parameter	Conditions	Conditions T		_{amb} = -40 °C to +85 °C		T_{amb} = -40 °	C to +125 °C	Unit
				Min	Typ <mark>[1]</mark>	Max	Min	Max	
t _{pd} propagation delay		An to Bn or Bn to An; see <u>Figure 14</u>	<u>[2][3]</u>						
		$V_{CC} = 3.0 \text{ V} \text{ to } 3.6 \text{ V}$		-	-	0.11	-	0.22	ns
t _{en}	enable time	OE to An or Bn; see <u>Figure 15</u>	<u>[4]</u>						
		$V_{CC} = 3.0 \text{ V} \text{ to } 3.6 \text{ V}$		1.5	2.9	5.0	1.5	6.0	ns
t _{dis} disable time		OE to An or Bn; see <u>Figure 15</u>	<u>[5]</u>						
		$V_{CC} = 3.0 \text{ V}$ to 3.6 V		0.8	3.3	7.0	0.8	8.0	ns

[1] All typical values are measured at T_{amb} = 25 °C and at nominal V_{CC}.

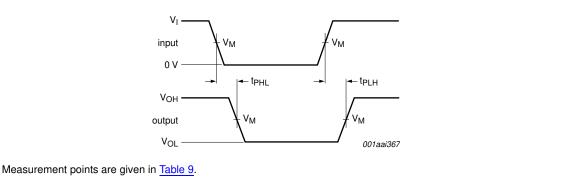
[2] The propagation delay is the calculated RC time constant of the on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).

 t_{pd} is the same as t_{PLH} and t_{PHL} . [3]

[4] t_{en} is the same as t_{PZH} and t_{PZL} .

[5] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

10.1 Waveforms



Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 14. The data input (An, Bn) to output (Bn, An) propagation delay times

Table 9. **Measurement points**

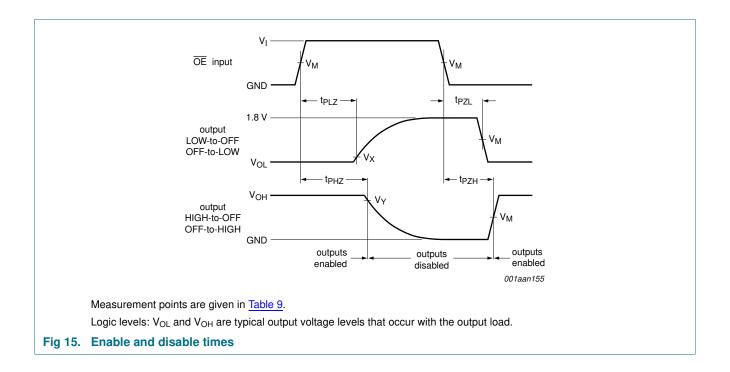
Supply voltage	Input C			Output		
V _{cc}	V _M	VI	$t_r = t_f$	V _M	V _X	V _Y
3.0 V to 3.6 V	0.5V _{CC}	V _{CC}	\leq 2.0 ns	0.9 V	V _{OL} + 0.15 V	V _{OH} – 0.15 V

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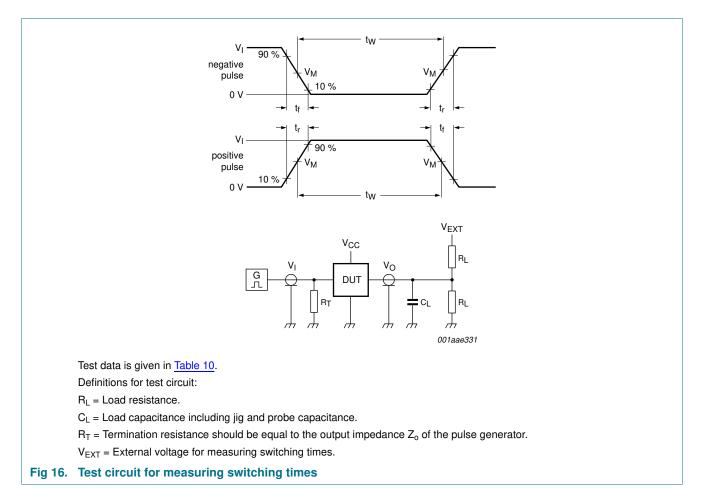


Table 10. Test data

Supply voltage	Load V		V _{EXT}		
V _{cc}	CL	RL	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
3.0 V to 3.6 V	30 pF	1 kΩ	open	GND	3.6 V

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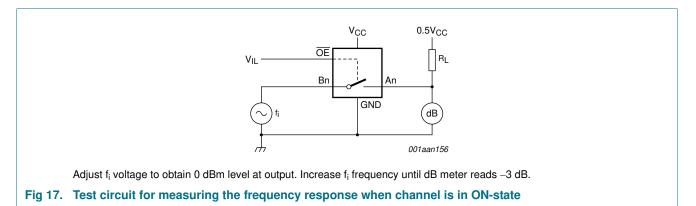
10.2 Additional dynamic characteristics

Table 11.Additional dynamic characteristicsGND = 0 V.

Symbol	Parameter	Conditions		T _{amb} = 25 °C			Unit
				Min	Тур	Max	
$f_{(-3dB)}$	-3 dB frequency response	V_{CC} = 3.3 V; R_L = 50 Ω ; see Figure 17	<u>[1]</u>	-	575	-	MHz

[1] f_i is biased at 0.5V_{CC}.

10.3 Test circuit

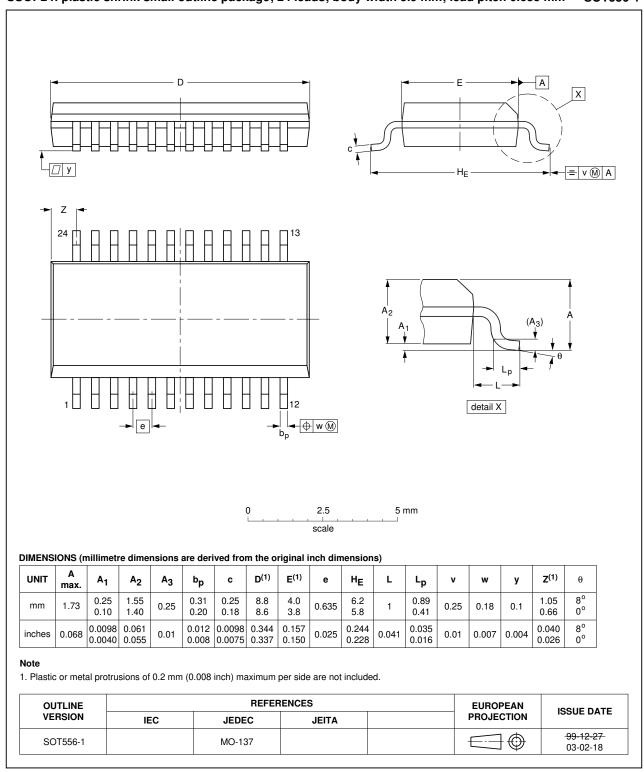


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11. Package outline



SSOP24: plastic shrink small outline package; 24 leads; body width 3.9 mm; lead pitch 0.635 mm SOT556-1

Fig 18. Package outline SOT556-1 (SSOP24)

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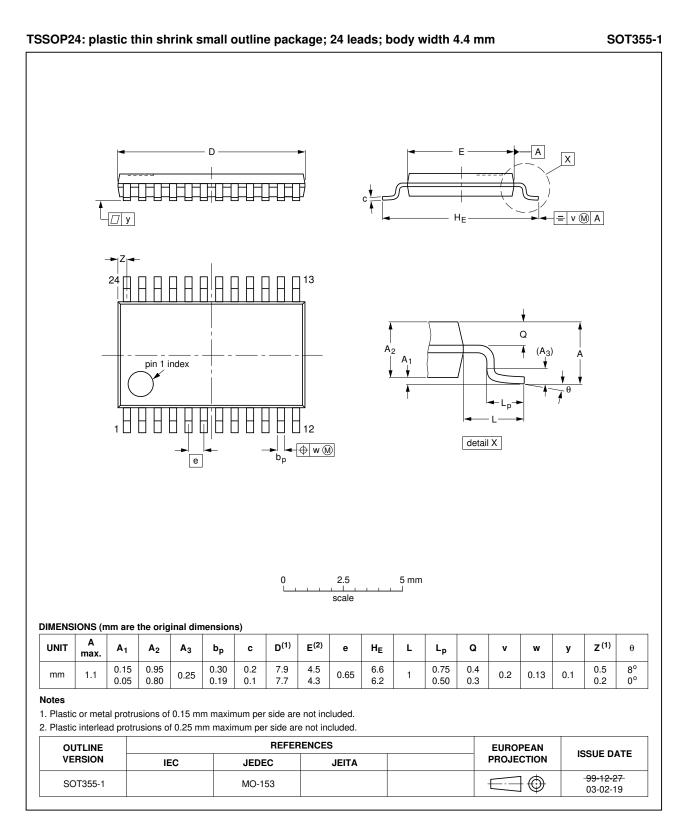
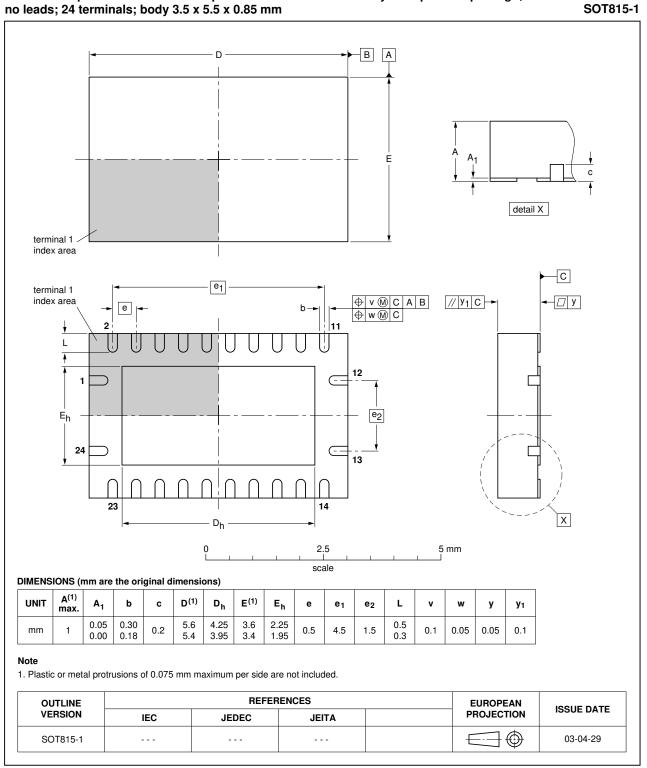


Fig 19. Package outline SOT355-1 (TSSOP24)

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DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm

Fig 20. Package outline SOT815-1 (DHVQFN24)

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12. Abbreviations

Table 12. Abb	reviations
Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

13. Revision history

Table 13.Revision history

Release date	Data sheet status	Change notice	Supersedes
20111214	Product data sheet	-	74CBTLVD3861 v.3
 Legal pages 	updated.		
20111020	Product data sheet	-	74CBTLVD3861 v.2
20110117	Product data sheet	-	74CBTLVD3861 v.1
20101206	Product data sheet	-	-
	20111214 • Legal pages 20111020 20110117	20111214Product data sheet• Legal pages updated.20111020Product data sheet20110117Product data sheet	20111214Product data sheet-• Legal pages updated20111020Product data sheet-20110117Product data sheet-

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14. Legal information

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Document status[1][2]	Product status ^[3]	Definition
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