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FAIRCHILD SEMICONDUCTOR®

January 2008

74F1071
18-Bit Undershoot/Overshoot Clamp and ESD Protection Device

Features

- 18-bit array structure in 20-pin package
- FAST® Bipolar voltage clamping action
- Dual center pin grounds for min inductance
- Robust design for ESD protection
- Low input capacitance
- Optimum voltage clamping for 5V CMOS/TTL applications

General Description

The 74F1071 is an 18-bit undershoot/overshoot clamp which is designed to limit bus voltages and also to protect more sensitive devices from electrical overstress due to electrostatic discharge (ESD). The inputs of the device aggressively clamp voltage excursions nominally at 0.5V below and 7V above ground.

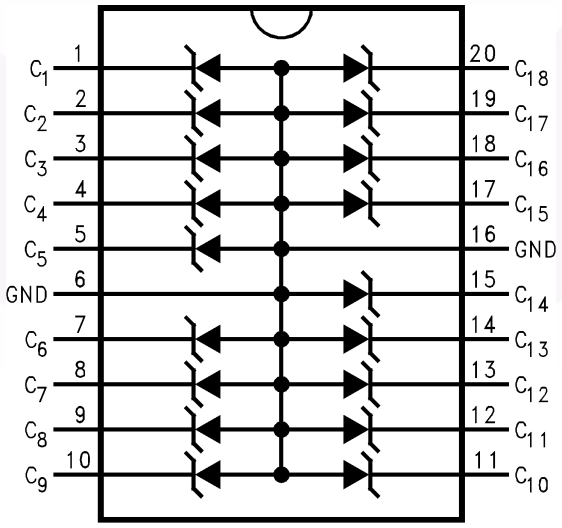
Ordering Information

Order Number	Package Number	Package Description
74F1071SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74F1071MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74F1071MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Note: Simplified Component Representation

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
T_{STG}	Storage Temperature	–65°C to +150°C
T_A	Ambient Temperature Under Bias	–65°C to +125°C
T_J	Junction Temperature Under Bias	–65°C to +150°C
V_I	Input Voltage(1)	–0.5V to +6V
I_I	Input Current(1)	–200mA to +50mA
	ESD(2)	
	Human Body Model (MIL-STD-883D method 3015.7)	±10kV
	IEC 801-2	±6kV
	Machine Model (EIAJIC-121-1981)	±2kV
	DC Latchup Source Current (JEDEC Method 17)	±500mA
	Package Power Dissipation @ +70°C SOIC Package	800mW

Notes:

1. Voltage ratings may be exceeded if current ratings and junction temperature and power consumption ratings are not exceeded.
2. ESD Rating for Direct contact discharge using ESD Simulation Tester. Higher rating may be realized in the actual application.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

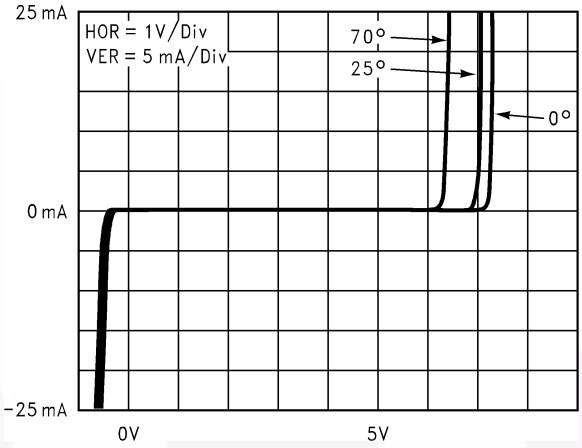
Symbol	Parameter	Rating
T_A	Free Air Ambient Temperature	0°C to +70°C
V_Z	Reverse Bias Voltage	0V to 5.25 V_{DC}
θ_{JA}	Thermal Resistance (in Free Air)	
	SOIC Package	100°C/W
	SSOP Package	110°C/W

DC Electrical Characteristics

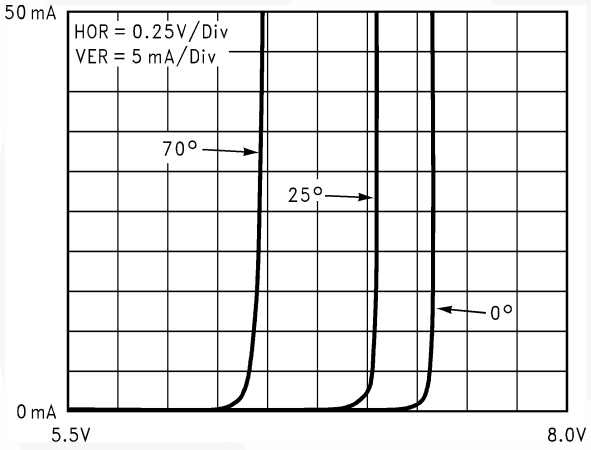
Symbol	Parameter	Conditions	T_A = +25°C			T_A = 0°C to +70°C		Units
			Min.	Typ.	Max.	Min.	Max.	
I_{IH}	Input HIGH Current	V_{IN} = 5.25V; Untested Input @ GND		1.5	10		50	µA
		V_{IN} = 5.5V; Untested Input @ GND		3	20		100	
V_Z	Reverse Voltage	I_Z = 1mA; Untested Inputs @ GND	6.6	6.9	7.2	5.9	7.7	V
		I_Z = 50mA; Untested Inputs @ GND		7.1	7.5		8.0	
V_F	Forward Voltage	I_F = –18mA; Untested Inputs @ 5V	–0.3	–0.6	–0.9	–0.3	–0.9	V
		I_F = –200mA; Untested Inputs @ 5V	–0.5	–1.1	–1.5	–0.5	–1.5	
I_{CT}	Adjacent Input Crosstalk				3			%
C_{IN}	Input Capacitance (small signal @ 1MHz)	V_{BIAS} = 0 V_{DC}		25				pF
		V_{BIAS} = 5 V_{DC}		13				

DC Electrical Characteristics

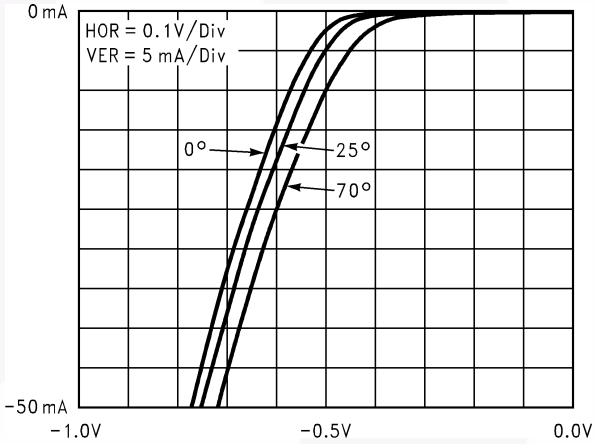
Typical Forward and Reverse V/I Characteristics

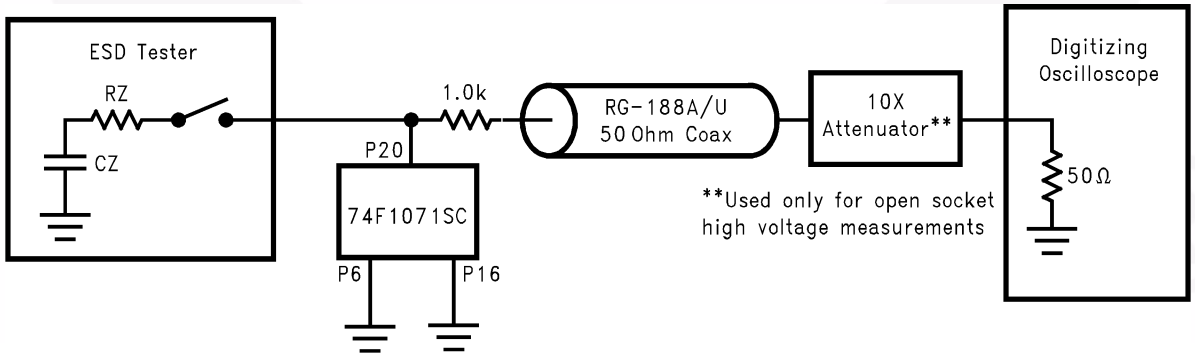


Typical Reverse Conduction Characteristics



Typical Forward Conduction Characteristics



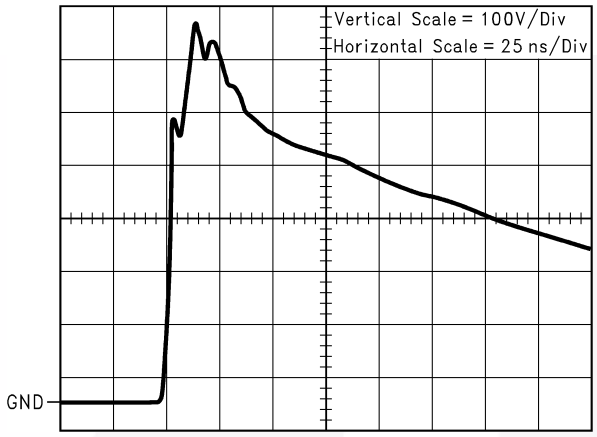


ESD Network	CZ	RZ
Human Body Model	100pF	1500Ω
IEC 801-2	150pF	330Ω

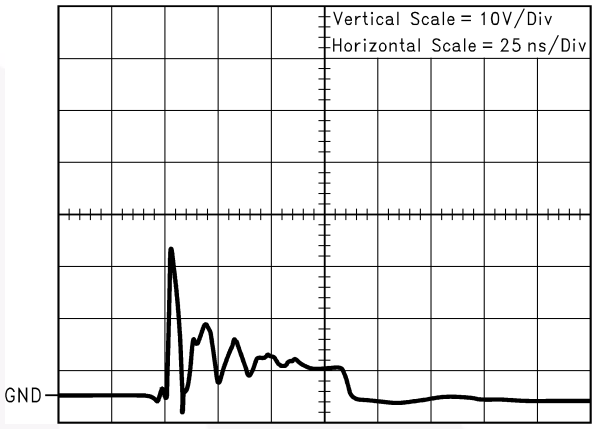
Simulated ESD Voltage Clamping Test Circuit

DC Electrical Characteristics (Continued)

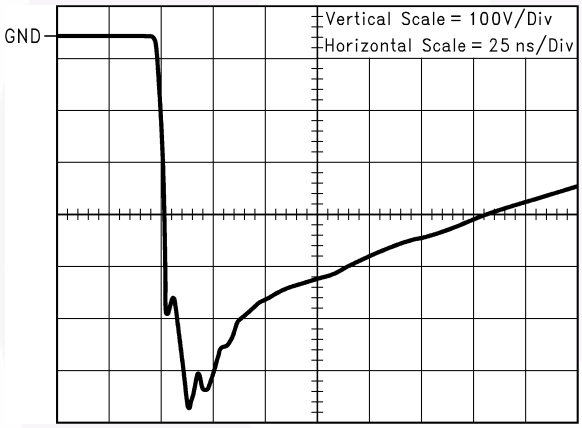
Unclamped +1kV ESD Voltage Waveform (IEC801-2 Network)



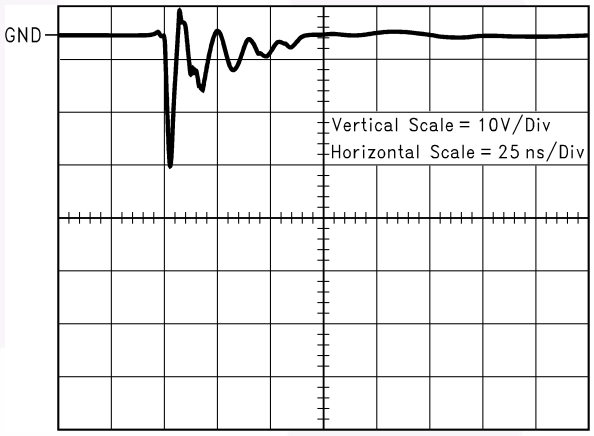
Clamped +1kV ESD Voltage Waveform (IEC801-2 Network)



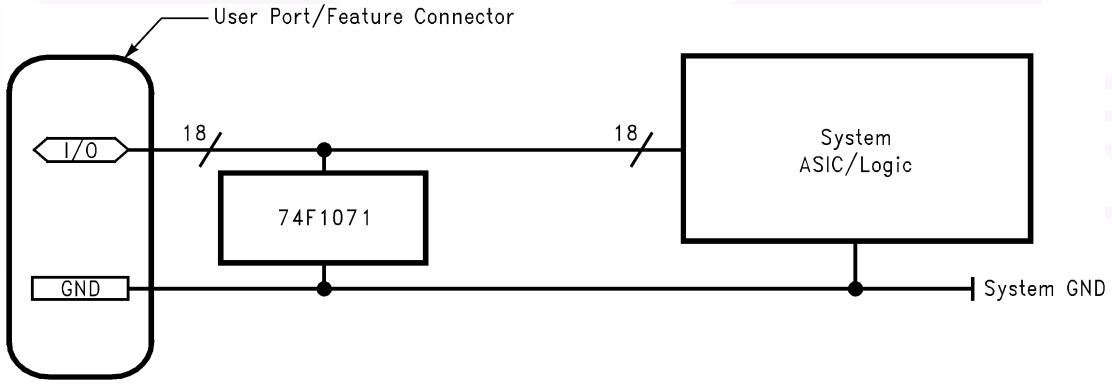
Unclamped -1kV ESD Voltage Waveform (IEC801-2 Network)



Clamped -1kV ESD Voltage Waveform (IEC801-2 Network)



Typical Application



74F1071 ESD Protection of ASIC on User Port

Physical Dimensions

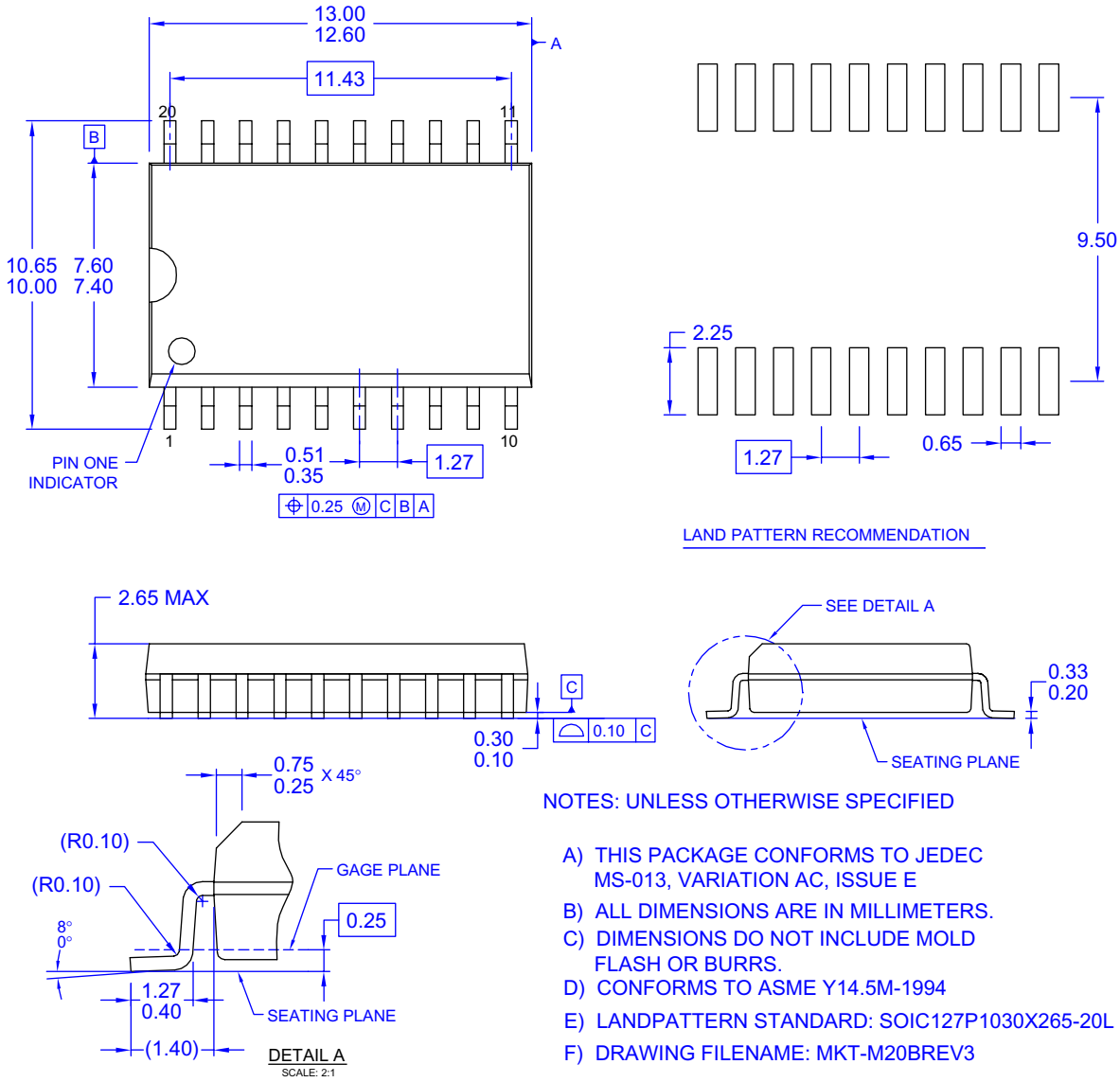


Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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Physical Dimensions (Continued)

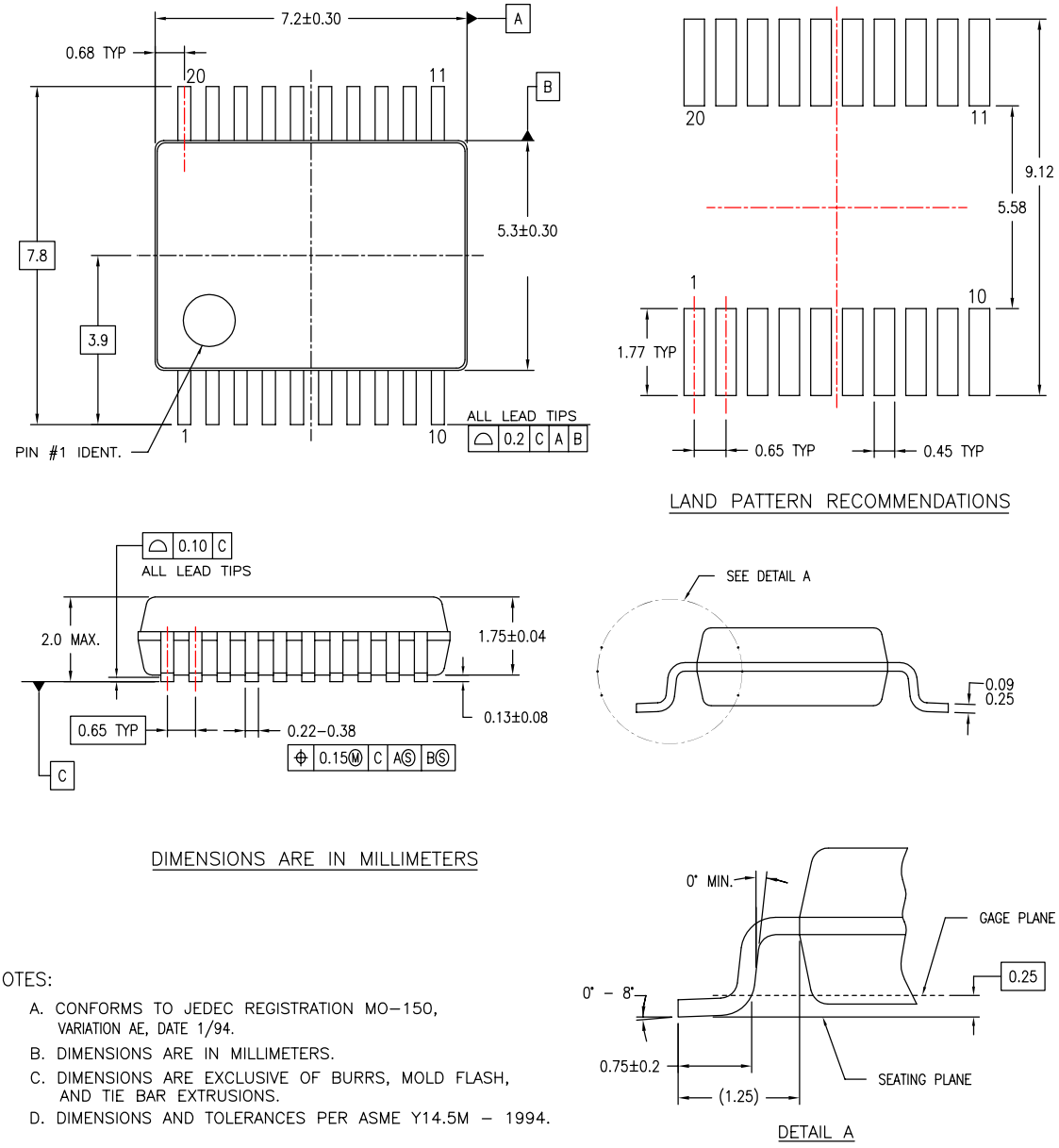

Figure 2. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

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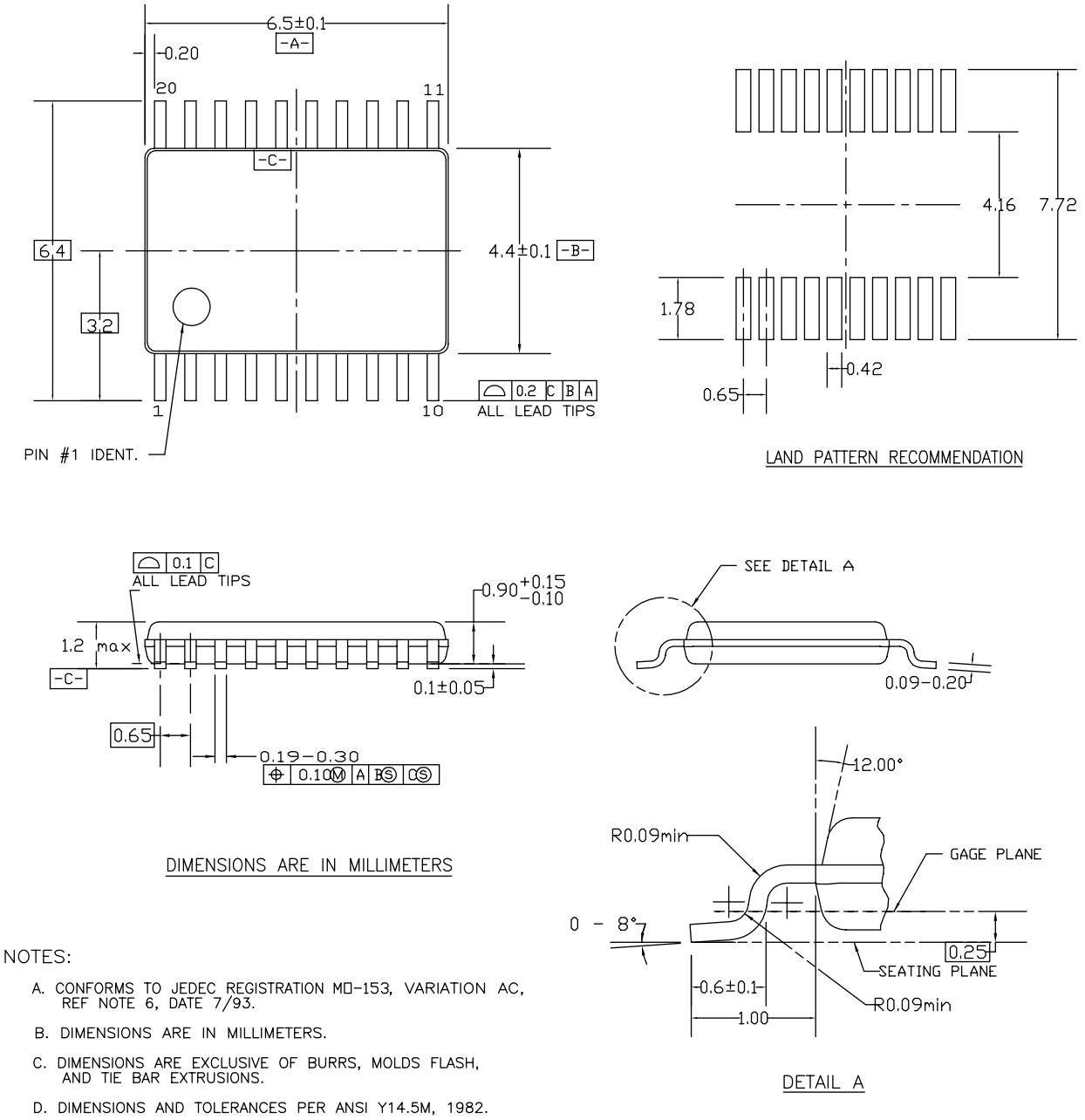
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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