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# 74F109

## Dual JK Positive Edge-Triggered Flip-Flop

### General Description

The F109 consists of two high-speed, completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D-type flip-flop (refer to F74 data sheet) by connecting the J and K inputs.

### Asynchronous Inputs:

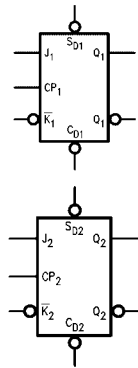
- LOW input to  $\bar{S}_D$  sets Q to HIGH level
- LOW input to  $\bar{C}_D$  sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

### Ordering Code:

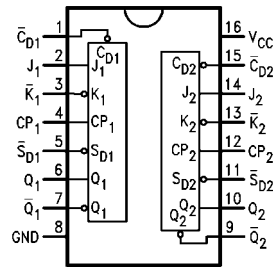
Order Number	Package Number	Package Description
74F109SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F109SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F109PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

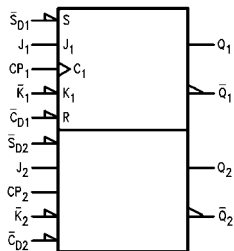
### Logic Symbols



### Connection Diagram



### IEEE/IEC



### Truth Table

Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	↗	l	l	L	H
H	H	↗	h	l	Toggle	Toggle
H	H	↗	l	h	Q	$\overline{Q}$
H	H	↗	h	h	H	L
H	H	L	X	X	Q	$\overline{Q}$

H (h) = HIGH Voltage Level  
 L (l) = LOW Voltage Level  
 ↗ = LOW-to-HIGH Transition  
 X = Immaterial

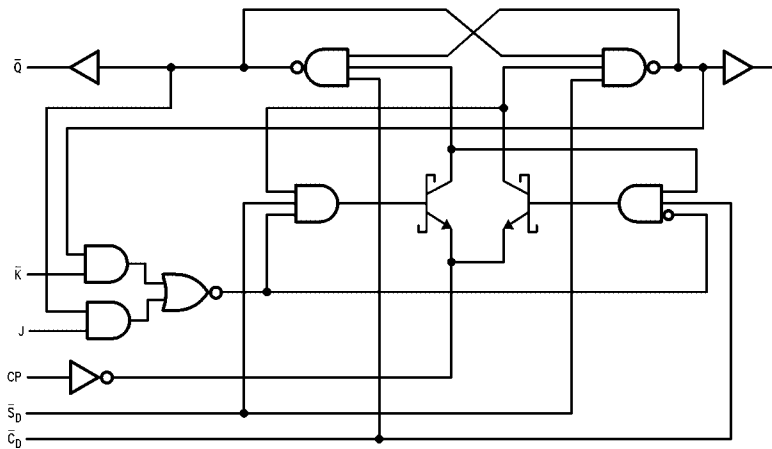
Q<sub>0</sub> ( $\overline{Q}_0$ ) = Before LOW-to-HIGH Transition of Clock

Lower case letters indicate the state of the referenced output one setup time prior to the LOW-to-HIGH clock transition.

### Unit Loading/Fan Out

Pin Names	Description	U.L.	
		HIGH/LOW	Input I <sub>IH</sub> /I <sub>IL</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
J <sub>1</sub> , J <sub>2</sub> , $\overline{K}_1$ , $\overline{K}_2$	Data Inputs	1.0/1.0	20 μA/-0.6 mA
CP <sub>1</sub> , CP <sub>2</sub>	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0	20 μA/-0.6 mA
$\overline{C}_D1$ , $\overline{C}_D2$	Direct Clear Inputs (Active LOW)	1.0/3.0	20 μA/-1.8 mA
$\overline{S}_D1$ , $\overline{S}_D2$	Direct Set Inputs (Active LOW)	1.0/3.0	20 μA/-1.8 mA
Q <sub>1</sub> , Q <sub>2</sub> , $\overline{Q}_1$ , $\overline{Q}_2$	Outputs	50/33.3	-1 mA/20 mA

### Block Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEx</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V (J <sub>n</sub> , $\overline{R}_n$ )
				-1.8	mA	Max	V <sub>IN</sub> = 0.5V ( $\overline{C}_{Dn}$ , $\overline{S}_{Dn}$ )
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		11.7	17.0	mA	Max	CP = 0V

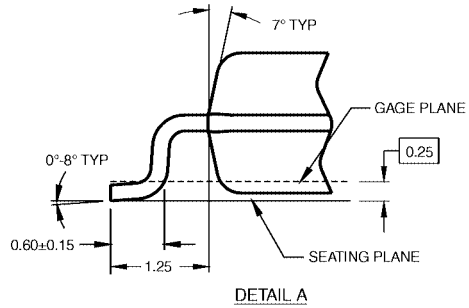
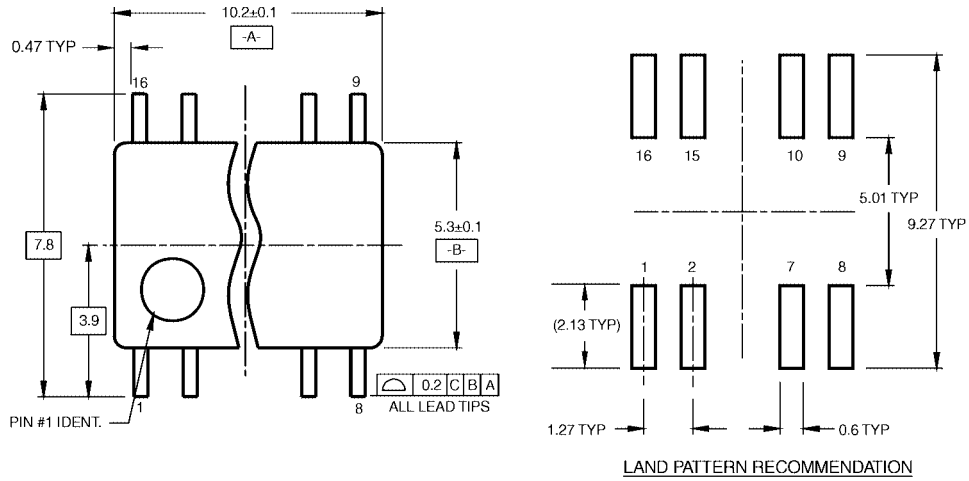
AC Electrical Characteristics							
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency	100	125		90		MHz
$t_{PLH}$	Propagation Delay	3.8	5.3	7.0	3.8	8.0	ns
$t_{PHL}$	$CP_n$ to $Q_n$ or $\bar{Q}_n$	4.4	6.2	8.0	4.4	9.2	
$t_{PLH}$	Propagation Delay	3.2	5.2	7.0	3.2	8.0	ns
$t_{PHL}$	$\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to $Q_n$ or $\bar{Q}_n$	3.5	7.0	9.0	3.5	10.5	ns
AC Operating Requirements							
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		Units	
		Min	Max	Min	Max		
$t_S(H)$	Setup Time, HIGH or LOW	3.0		3.0		ns	
$t_S(L)$	$J_n$ or $\bar{K}_n$ to $CP_n$	3.0		3.0			
$t_H(H)$	Hold Time, HIGH or LOW	1.0		1.0		ns	
$t_H(L)$	$J_n$ or $\bar{K}_n$ to $CP_n$	1.0		1.0			
$t_W(H)$	$CP_n$ Pulse Width	4.0		4.0		ns	
$t_W(L)$	HIGH or LOW	5.0		5.0			
$t_W(L)$	$\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ Pulse Width LOW	4.0		4.0		ns	
$t_{REC}$	Recovery Time $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to CP	2.0		2.0		ns	

**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

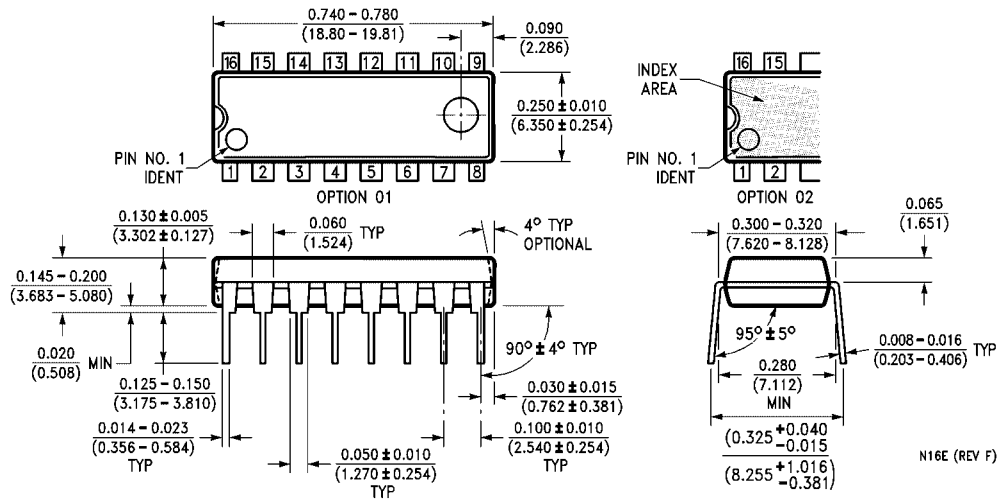


- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E**

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