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## 74F151A 8-Input Multiplexer

### General Description

The F151A is a high-speed 8-input digital multiplexer. It provides in one package the ability to select one line of data from up to eight sources. The F151A can be used as a

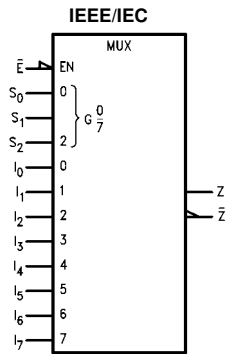
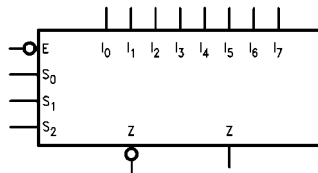
universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

### Ordering Code:

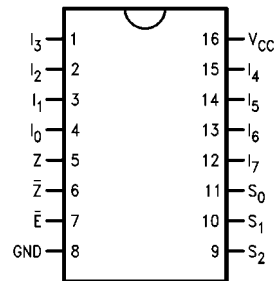
Order Number	Package Number	Package Description
74F151ASC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F151ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F151APC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



### Unit Loading/Fan Out

Pin Names	Description	U.L.	
		HIGH/LOW	Input $I_H/I_L$ Output $I_{OH}/I_{OL}$
$I_0$ - $I_7$	Data Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$S_0$ - $S_2$	Select Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$\bar{E}$	Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
Z	Data Output	50/33.3	-1 mA/20 mA
$\bar{Z}$	Inverted Data Output	50/33.3	-1 mA/20 mA

### Functional Description

The F151A is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs,  $S_0, S_1, S_2$ . Both assertion and negation outputs are provided. The Enable input ( $\bar{E}$ ) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \bar{E} \cdot (I_0 \bar{S}_2 \bar{S}_1 \bar{S}_0 + I_1 \bar{S}_2 \bar{S}_1 S_0 + I_2 \bar{S}_2 S_1 \bar{S}_0 + I_3 \bar{S}_2 S_1 S_0 + I_4 S_2 \bar{S}_1 \bar{S}_0 + I_5 S_2 \bar{S}_1 S_0 + I_6 S_2 S_1 \bar{S}_0 + I_7 S_2 S_1 S_0)$$

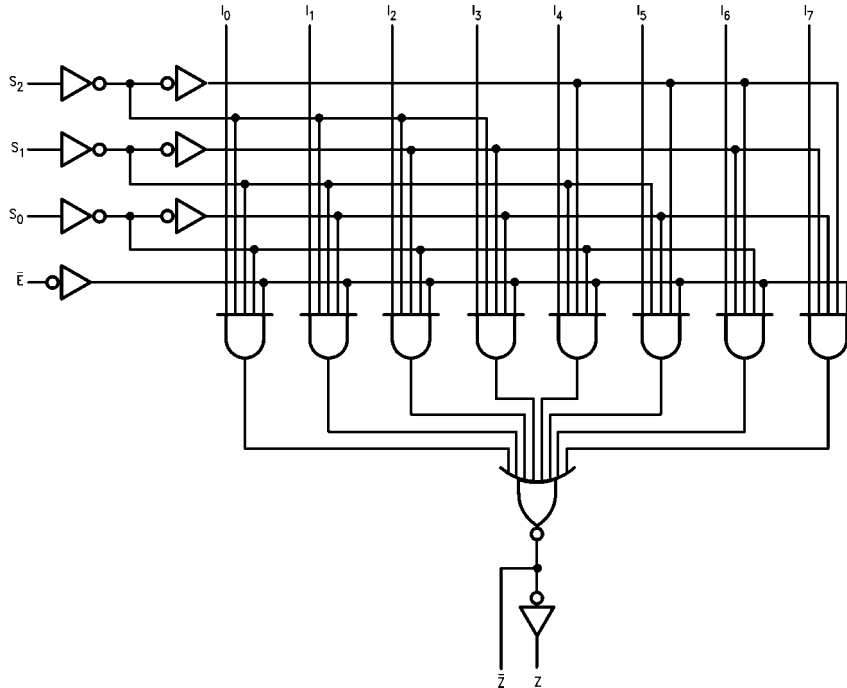
The F151A provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the F151A can provide any logic function of four variables and its negation.

### Truth Table

Inputs				Outputs	
$\bar{E}$	$S_2$	$S_1$	$S_0$	$\bar{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\bar{I}_0$	$I_0$
L	L	L	H	$\bar{I}_1$	$I_1$
L	L	H	L	$\bar{I}_2$	$I_2$
L	L	H	H	$\bar{I}_3$	$I_3$
L	H	L	L	$\bar{I}_4$	$I_4$
L	H	L	H	$\bar{I}_5$	$I_5$
L	H	H	L	$\bar{I}_6$	$I_6$
L	H	H	H	$\bar{I}_7$	$I_7$

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

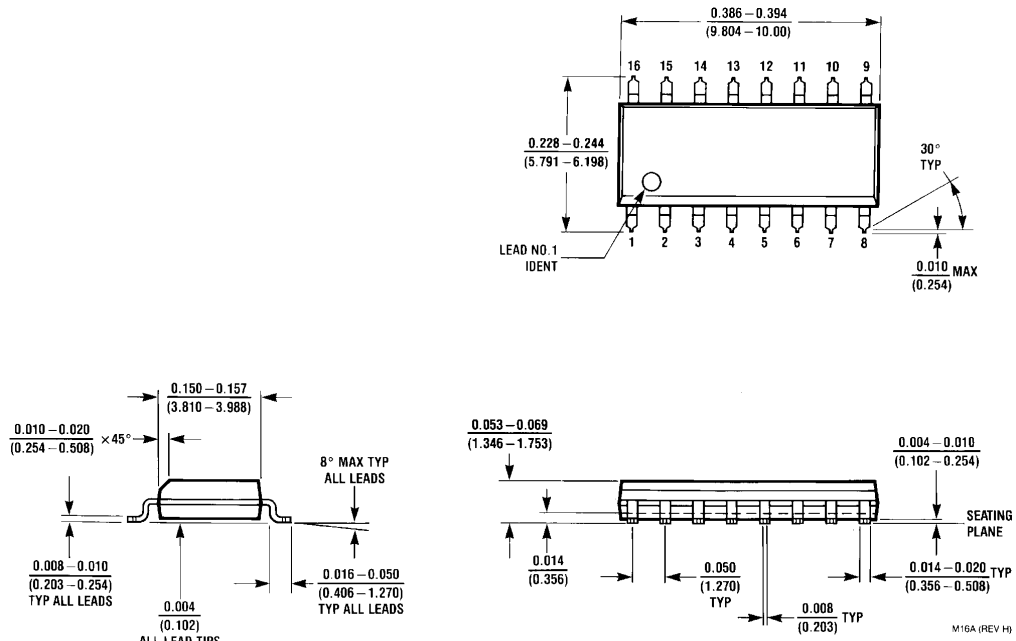
**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 5% V <sub>CC</sub>	2.5 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		13.5	21.0	mA	Max	V <sub>O</sub> = HIGH

## AC Electrical Characteristics

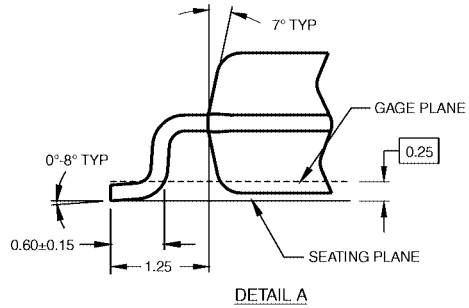
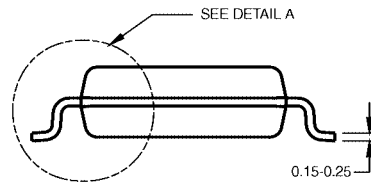
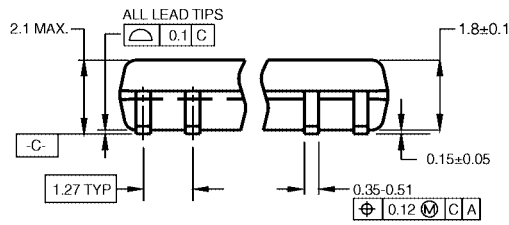
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = 0°C to +70°C C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>n</sub> to $\bar{Z}$	4.0	6.2	9.0	3.5	9.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>n</sub> to Z	4.5	7.5	10.5	4.5	12.0	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\bar{E}$ to $\bar{Z}$	3.0	4.7	6.1	3.0	7.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\bar{E}$ to Z	5.0	7.0	9.5	4.0	10.5	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to $\bar{Z}$	3.0	4.8	6.5	3.0	7.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Z	3.0	4.8	6.5	2.5	7.5	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Z	3.7	5.5	7.0	3.7	7.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Z	3.7	5.5	7.0	3.7	7.5	

**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

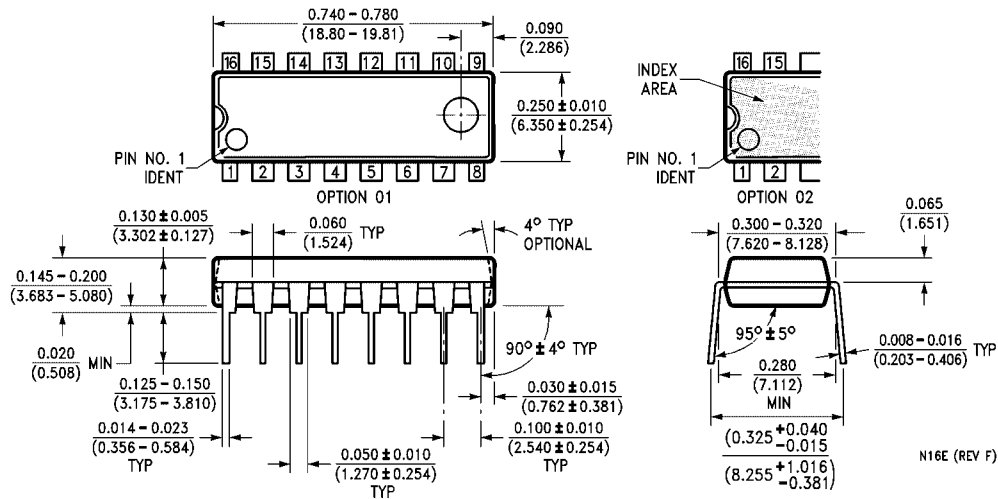


- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E**

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