



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# 74F299

## Octal Universal Shift/Storage Register with Common Parallel I/O Pins

### General Description

The 74F299 is an 8-bit universal shift/storage register with 3-STATE outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs,  $Q_0$ - $Q_7$ , are provided to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

### Features

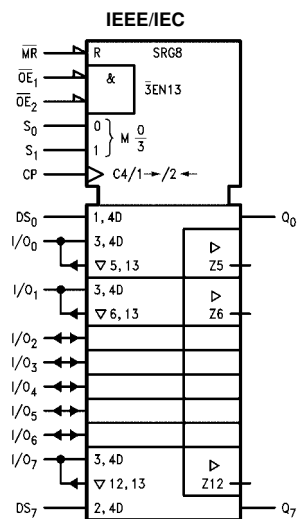
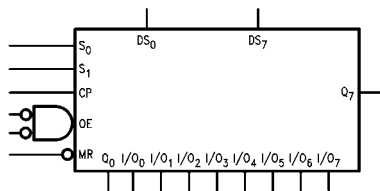
- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- 3-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

### Ordering Code:

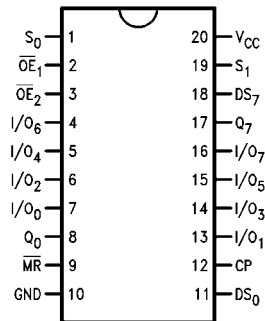
Order Number	Package Number	Package Description
74F299SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F299SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F299PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



### Unit Loading/Fan Out

Pin Names	Description	U.L.	
		HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/-0.6 mA
DS <sub>0</sub>	Serial Data Input for Right Shift	1.0/1.0	20 $\mu$ A/-0.6 mA
DS <sub>7</sub>	Serial Data Input for Left Shift	1.0/1.0	20 $\mu$ A/-0.6 mA
S <sub>0</sub> , S <sub>1</sub>	Mode Select Inputs	1.0/2.0	20 $\mu$ A/-1.2 mA
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
I/O <sub>0</sub> -I/O <sub>7</sub>	Parallel Data Inputs or 3-STATE Parallel Outputs	3.5/1.083 150/40(33.3)	70 $\mu$ A/-0.65 mA -3 mA/24 mA (20 mA)
Q <sub>0</sub> , Q <sub>7</sub>	Serial Outputs	50/33.3	-1 mA/20 mA

### Functional Description

The 74F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S<sub>0</sub> and S<sub>1</sub>, as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-STATE buffers that also serve as data inputs in the parallel load mode. Q<sub>0</sub> and Q<sub>7</sub> are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on  $\overline{MR}$  overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

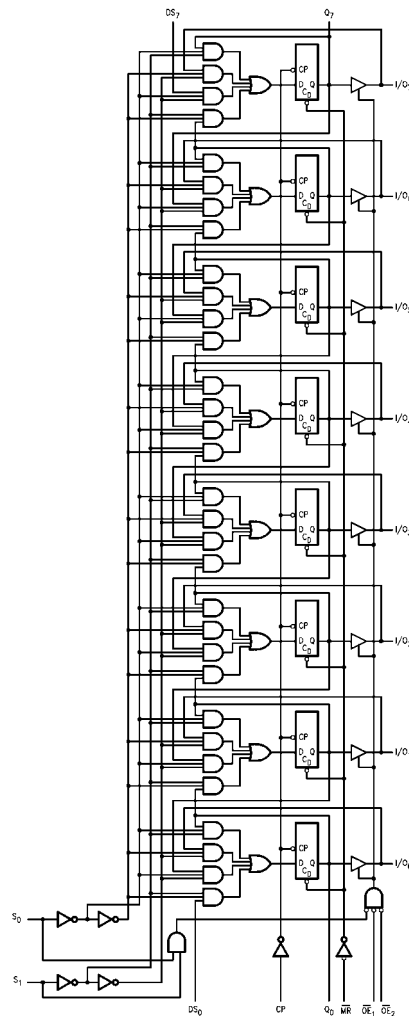
A HIGH signal on either  $\overline{OE}_1$  or  $\overline{OE}_2$  disables the 3-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-STATE outputs are also disabled by HIGH signals on both S<sub>0</sub> and S<sub>1</sub> in preparation for a parallel load operation.

### Mode Select Table

Inputs				Response
$\overline{MR}$	S <sub>1</sub>	S <sub>0</sub>	CP	
L	X	X	X	Asynchronous Reset; Q <sub>0</sub> -Q <sub>7</sub> = LOW
H	H	H	↗	Parallel Load; I/O <sub>n</sub> → Q <sub>n</sub>
H	L	H	↗	Shift Right; DS <sub>0</sub> → Q <sub>0</sub> , Q <sub>0</sub> → Q <sub>1</sub> , etc.
H	H	L	↗	Shift Left; DS <sub>7</sub> → Q <sub>7</sub> , Q <sub>7</sub> → Q <sub>6</sub> , etc.
H	L	L	X	Hold

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↗ = LOW-to-HIGH Clock Transition

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
ESD Last Passing Voltage (Min)	4000V
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	
Current Applied to Output in LOW State (Max)	-0.5V to +5.5V twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 10% V <sub>CC</sub> 5% V <sub>CC</sub> 5% V <sub>CC</sub>	2.5 2.4 2.7 2.7		V	Min	I <sub>OH</sub> = -1 mA (Q <sub>0</sub> , Q <sub>7</sub> , I/O <sub>n</sub> ) I <sub>OH</sub> = -3 mA (I/O <sub>n</sub> ) I <sub>OH</sub> = -1 mA (Q <sub>0</sub> , Q <sub>7</sub> , I/O <sub>n</sub> ) I <sub>OH</sub> = -3 mA (I/O <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub> 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA (Q <sub>0</sub> , Q <sub>7</sub> ) I <sub>OL</sub> = 24 mA (I/O <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V (CP, DS <sub>0</sub> , DS <sub>7</sub> , S <sub>0</sub> , S <sub>1</sub> , MR, OE <sub>1</sub> , OE <sub>2</sub> )
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V (CP, DS <sub>0</sub> , DS <sub>7</sub> , S <sub>0</sub> , S <sub>1</sub> , MR, OE <sub>1</sub> , OE <sub>2</sub> )
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)			0.5	mA	Max	V <sub>IN</sub> = 5.5V (I/O <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6 -1.2	mA	Max	V <sub>IN</sub> = 0.5V (CP, DS <sub>0</sub> , DS <sub>7</sub> , MR, OE <sub>1</sub> , OE <sub>2</sub> ) V <sub>IN</sub> = 0.5V (S <sub>0</sub> , S <sub>1</sub> )
I <sub>IH+</sub> I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>I/O</sub> = 2.7V (I/O <sub>n</sub> )
I <sub>IL+</sub> I <sub>OZL</sub>	Output Leakage Current			-650	μA	Max	V <sub>I/O</sub> = 0.5V (I/O <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		68	95	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		68	95	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		68	95	mA	Max	V <sub>O</sub> = HIGH Z

AC Electrical Characteristics									
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = 5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V C <sub>L</sub> = 50 pF		T <sub>A</sub> = 0 to +70°C V <sub>CC</sub> = 5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Input Frequency	70	100		85		70		MHz
t <sub>PLH</sub>	Propagation Delay	4.0	7.0	8.0	4.0	9.0	4.0	8.5	ns
t <sub>PHL</sub>	CP to Q <sub>0</sub> or Q <sub>7</sub>	4.5	6.5	8.0	4.5	9.5	4.5	8.5	
t <sub>PLH</sub>	Propagation Delay	3.5	7.0	9.0	3.5	10.0	3.5	10.0	ns
t <sub>PHL</sub>	CP to I/O <sub>n</sub>	4.0	8.5	9.0	4.0	11.0	4.0	10.0	
t <sub>PHL</sub>	Propagation Delay MR to Q <sub>0</sub> or Q <sub>7</sub>	5.5	7.5	9.5	5.5	12.5	5.5	10.5	ns
t <sub>PHL</sub>	Propagation Delay MR to I/O <sub>n</sub>	5.5	11.0	10.0	5.5	12.0	5.5	10.5	
t <sub>PZH</sub>	Output Enable Time	3.5	6.0	8.0	3.0	9.5	3.5	9.0	ns
t <sub>PZL</sub>	OE to I/O <sub>n</sub>	4.0	7.0	10.0	4.0	13.0	4.0	11.0	
t <sub>PHZ</sub>	Output Disable Time	2.0	4.5	6.0	1.5	7.0	2.0	7.0	ns
t <sub>PLZ</sub>	OE to I/O <sub>n</sub>	1.0	4.0	5.5	1.0	6.5	1.0	6.5	
t <sub>PZH</sub>	Output Enable Time	3.5		9.0	3.0	10.5	3.5	10.0	ns
t <sub>PZL</sub>	S <sub>n</sub> to I/O <sub>n</sub>	4.0		10.0	4.0	13.0	4.0	11.0	
t <sub>PHZ</sub>	Output Disable Time	2.5		6.0	1.5	7.0	2.5	7.0	ns
t <sub>PLZ</sub>	S <sub>n</sub> to I/O <sub>n</sub>	1.5		5.5	1.0	6.5	1.5	6.5	

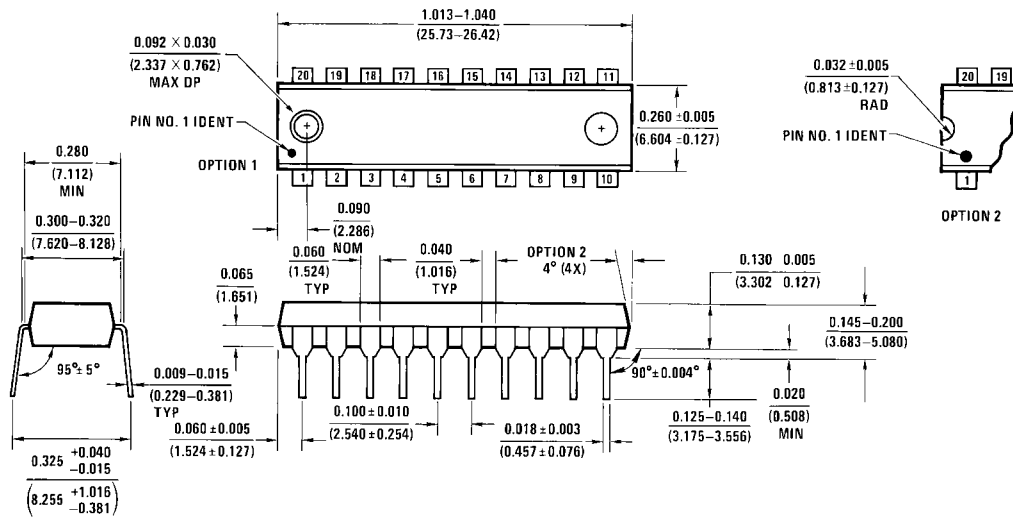
  

AC Operating Requirements								
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = 5.0V		T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V		T <sub>A</sub> = 0 to +70°C V <sub>CC</sub> = 5.0V		Units
		Min	Max	Min	Max	Min	Max	
t <sub>S(H)</sub>	Setup Time, HIGH or LOW	8.5		10.0		8.5		ns
t <sub>S(L)</sub>	S <sub>0</sub> or S <sub>1</sub> to CP	8.5		7.5		8.5		
t <sub>H(H)</sub>	Hold Time, HIGH or LOW	0		0		0		ns
t <sub>H(L)</sub>	S <sub>0</sub> or S <sub>1</sub> to CP	0		0		0		
t <sub>S(H)</sub>	Setup Time, HIGH or LOW	5.0		5.0		5.0		ns
t <sub>S(L)</sub>	I/O <sub>n</sub> , DS <sub>0</sub> or DS <sub>7</sub> to CP	5.0		5.0		5.0		
t <sub>H(H)</sub>	Hold Time, HIGH or LOW	2.0		2.0		2.0		ns
t <sub>H(L)</sub>	I/O <sub>n</sub> , DS <sub>0</sub> or DS <sub>7</sub> to CP	2.0		2.0		2.0		
t <sub>W(H)</sub>	CP Pulse Width	5.0		5.0		5.0		ns
t <sub>W(L)</sub>	HIGH or LOW	5.0		5.0		5.0		
t <sub>W(L)</sub>	MR Pulse Width, LOW	5.0		6.0		5.0		ns
t <sub>REC</sub>	Recovery Time, MR to CP	7.0		12.0		7.0		ns





**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N20A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)