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FAIRCHILD SEMICONDUCTOR TM

April 1988
Revised April 1999

74F322
Octal Serial/Parallel Register with Sign Extend

General Description

The 74F322 is an 8-bit shift register with provision for either serial or parallel loading and with 3-STATE parallel outputs plus a bi-state serial output. Parallel data inputs and parallel outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend and parallel load. An asynchronous Master Reset ($\overline{MR}$) input overrides clocked operation and clears the register.

Features

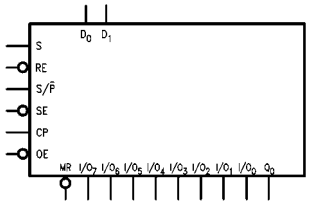
- Multiplexed parallel I/O ports
- Separate serial input and output
- Sign extend function
- 3-STATE outputs for bus applications

Ordering Code:

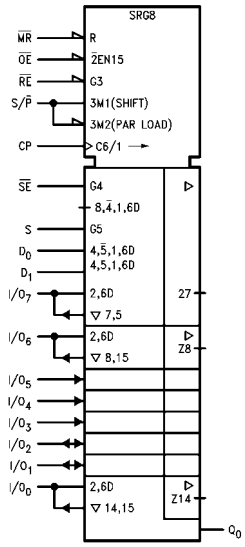
Order Number	Package Number	Package Description
74F322PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

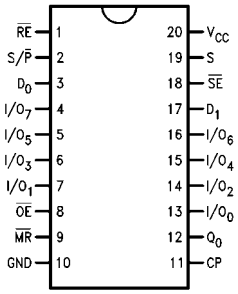
Logic Symbols



IEEE/IEC



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{RE}$	Register Enable Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
$S/\overline{P}$	Serial (HIGH) or Parallel (LOW) Mode Control Input	1.0/1.0	20 µA/–0.6 mA
$\overline{SE}$	Sign Extend Input (Active LOW)	1.0/3.0	20 µA/–1.8 mA
S	Serial Data Select Input	1.0/2.0	20 µA/–1.2 mA
D_0, D_1	Serial Data Inputs	1.0/1.0	20 µA/–0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 µA/–0.6 mA
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
$\overline{OE}$	3-STATE Output Enable Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
Q_0	Bi-State Serial Output	50/33.3	–1 mA/–20 mA
I/O_0–I/O_7	Multiplexed Parallel Data Inputs or	3.5/1.083	70 µA/–0.65 mA
	3-STATE Parallel Data Outputs	150/40 (33.3)	–3 mA/24 mA (20 mA)

Functional Description

The 74F322 contains eight D-type edge triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A LOW signal on $\overline{RE}$ enables shifting or parallel loading, while a HIGH signal enables the hold mode. A HIGH signal on $S/\overline{P}$ enables shift right, while a LOW signal disables the 3-STATE output buffers and enables parallel loading. In the shift right mode a HIGH signal on $\overline{SE}$ enables serial entry from either D_0 or D_1, as determined by the S input. A LOW signal on $\overline{SE}$ enables shift right but Q_7 reloads its contents, thus performing the sign extend function required for the 74F384 Twos Complement Multiplier. A HIGH signal on $\overline{OE}$ disables the 3-STATE output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

Mode Select Table

Mode	Inputs							Outputs								Q_0
	$\overline{MR}$	$\overline{RE}$	$S/\overline{P}$	$\overline{SE}$	S	$\overline{OE}$ (Note 1)	CP	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	
Clear	L	X	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X	↗	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	I_0
Shift Right	H	L	H	H	L	L	↗	D_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
	H	L	H	H	H	L	↗	D_1	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
Sign Extend	H	L	H	L	X	L	↗	O_7	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
Hold	H	H	X	X	X	L	↗	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance Output State
↗ = LOW-to-HIGH Transition
NC = No Change

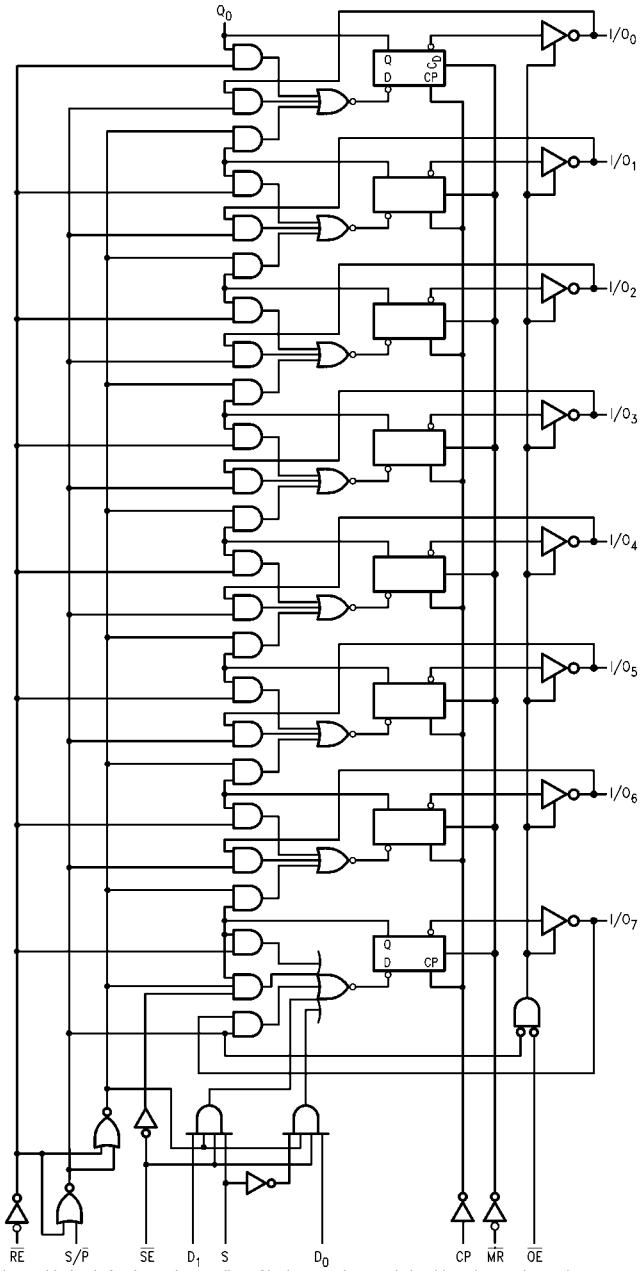
Note: I_7–I_0 = The level of the steady-state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q_0) are isolated from the I/O terminal.

Note: D_0, D_1 = The level of the steady-state inputs to the serial multiplexer input.

Note: O_7–O_0 = The level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.

Note 1: When the $\overline{OE}$ input is HIGH all I/O_n terminals are at the high impedance state; sequential operation or clearing of the register is not affected.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA (Q_0, I/O_n)
		10% V_{CC}	2.4					I_{OH} = −3 mA (I/O_n)
		5% V_{CC}	2.7					I_{OH} = −1 mA (Q_0, I/O_n)
		5% V_{CC}	2.7					I_{OH} = −3 mA (I/O_n)
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA (Q_0)
		10% V_{CC}			0.5			I_{OL} = 24 mA (I/O_n)
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V (Non-I/O Inputs)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				0.5	mA	Max	V_{IN} = 5.5V (I/O_n)
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V ($\overline{RE}$, S/$\overline{P}$, D_n, CP, $\overline{MR}$, $\overline{OE}$)
					−1.2	mA	Max	V_{IN}= 0.5V (S)
					−1.8	mA	Max	V_{IN}= 0.5V ($\overline{SE}$)
I_{IH} + I_{OZH}	Output Leakage Current				70	µA	Max	$V_{I/O}$ = 2.7V (I/O_n)
I_{IL} + I_{OZL}	Output Leakage Current				−650	µA	Max	$V_{I/O}$ = 0.5V (I/O_n)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	µA	0.0V	V_{OUT} = 5.25V
I_{CC}	Power Supply Current			60	90	mA	Max	

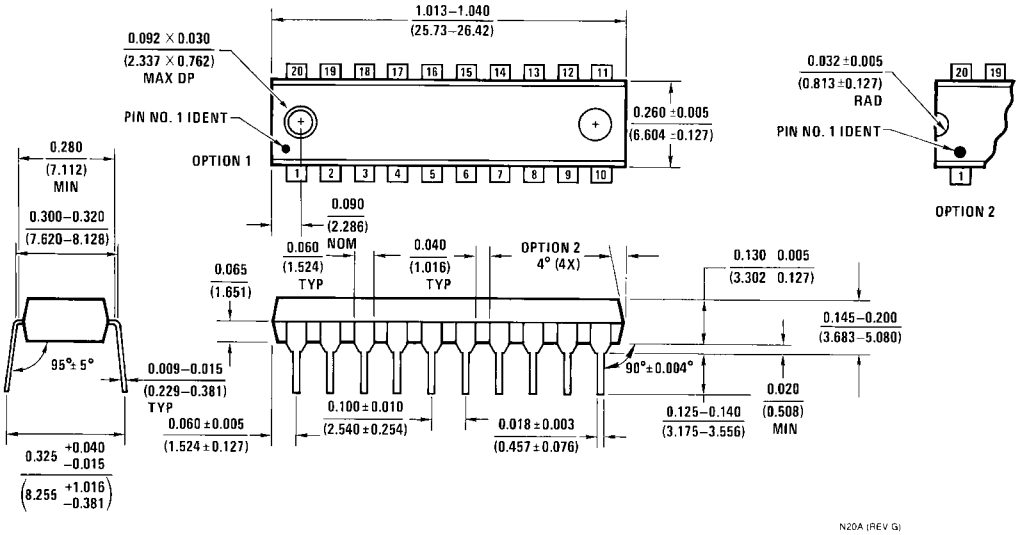
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		$T_A = 0°C$ to $+75°C$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	70	90		50		70		MHz
t_{PLH}	Propagation Delay	3.5	7.0	7.5	3.5	9.5	3.5	8.5	ns
t_{PHL}	CP to I/O_n	5.0	8.5	11.0	3.5	10.0	5.0	12.0	
t_{PLH}	Propagation Delay	3.5	7.0	9.0	3.5	11.0	3.5	10.0	
t_{PHL}	CP to Q_0	3.5	7.0	8.0	3.5	10.0	3.5	9.0	
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	6.0	10.0	13.0	6.0	15.0	6.0	14.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0	5.5	7.5	12.0	5.5	14.0	5.5	13.0	ns
t_{PZH}	Output Enable Time	3.0	6.5	9.0	3.0	12.5	3.0	10.0	ns
t_{PZL}	$\overline{OE}$ to I/O_n	4.0	8.5	11.0	4.0	14.5	4.0	12.0	
t_{PHZ}	Output Disable Time	2.0	4.5	6.0	2.0	8.0	2.0	7.0	
t_{PLZ}	$\overline{OE}$ to I/O_n	2.0	5.0	7.0	2.0	10.0	2.0	8.0	
t_{PZH}	Output Enable Time	4.5	8.0	10.5	4.5	13.5	4.5	11.5	ns
t_{PZL}	$S/\overline{P}$ to I/O_n	5.5	10.0	14.0	5.5	17.0	5.5	15.0	
t_{PHZ}	Output Disable Time	5.0	9.0	11.5	5.0	16.5	5.0	12.5	
t_{PLZ}	$S/\overline{P}$ to I/O_n	6.0	12.0	15.5	6.0	19.5	6.0	16.5	

AC Operating Requirements

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$		$T_A = -55°C$ to $+125°C$		$T_A = 0C$ to $+75°C$		Units
		Min	Max	Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	6.0		14.0		7.0		ns
$t_S(L)$	$\overline{RE}$ to CP	14.0		18.0		16.0		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		0		ns
$t_H(L)$	$\overline{RE}$ to CP	0		0		0		
$t_S(H)$	Setup Time, HIGH or LOW	6.5		8.5		7.5		ns
$t_S(L)$	D_0, D_1 or I/O_n to CP	6.5		8.5		7.5		
$t_H(H)$	Hold Time, HIGH or LOW	2.0		3.0		3.0		ns
$t_H(L)$	D_0, D_1 or I/O_n to CP	2.0		3.0		3.0		
$t_SH)$	Setup Time, HIGH or LOW	7.0		9.0		8.0		ns
$t_S(L)$	$\overline{SE}$ to CP	2.5		11.0		3.5		
$t_H(H)$	Hold Time, HIGH or LOW	2.0		2.0		2.0		ns
$t_H(L)$	$\overline{SE}$ to CP	0.0		1.0		0.0		
$t_S(H)$	Setup Time, HIGH or LOW	11.0		13.0		12.0		ns
$t_S(L)$	$S/\overline{P}$ to CP	13.5		21.0		15.5		
$t_S(H)$	Setup Time, HIGH or LOW	6.5		8.5		7.5		ns
$t_S(L)$	S to CP	9.0		11.0		10.0		
$t_H(H)$	Hold Time, HIGH or LOW	0		1.0		0		ns
$t_H(L)$	S or $S/\overline{P}$ to CP	0		0		0		
$t_W(H)$	CP Pulse Width, HIGH or LOW	7.0		8.0		7.0		ns
$t_W(L)$								
$t_W(L)$	$\overline{MR}$ Pulse Width, LOW	5.5		7.5		6.5		
t_{REC}	Recovery Time $\overline{MR}$ to CP	8.0		12.0		8.0		ns

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A