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DATA SHEET

For a complete data sheet, please also download:

• The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
• The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
• The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT139

Dual 2-to-4 line decoder/demultiplexer

Product specification

File under Integrated Circuits, IC06

September 1993

Philips Semiconductors

PHILIPS

Dual 2-to-4 line decoder/demultiplexer   74HC/HCT139

FEATURES

- Demultiplexing capability

- Two independent 2-to-4 decoders

- Multifunction capability

- Active LOW mutually exclusive outputs

- Output capability: standard

- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT139 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT139 are high-speed, dual 2-to-4 line decoder/multiplexers. This device has two independent decoders, each accepting two binary weighted inputs (nA_0 and nA_1) and providing four mutually exclusive active LOW outputs ($n\overline{Y}_0$ to $n\overline{Y}3$). Each decoder has an active LOW enable input ($n\overline{E}$).
When $n\overline{E}$ is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.
The "139" is identical to the HEF4556 of the HE4000B family.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	nA_n to $n\overline{Y}_n$		11	13	ns
	$n\overline{E}_3$ to $n\overline{Y}_n$		10	13	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	42	44	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

    $$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

    f_i = input frequency in MHz

    f_o = output frequency in MHz

    $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

    C_L = output load capacitance in pF

    V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
    For HCT the condition is V_I = GND to V_{CC} − 1.5 V

APPLICATIONS

- Memory decoding or data-routing

- Code conversion

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

Dual 2-to-4 line decoder/demultiplexer

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{E}$, $2\overline{E}$	enable inputs (active LOW)
2, 3	$1A_0$, $1A_1$	address inputs
4, 5, 6, 7	$1\overline{Y}_0$ to $1\overline{Y}_3$	outputs (active LOW)
8	GND	ground (0 V)
12, 11, 10, 9	$2\overline{Y}_0$ to $2\overline{Y}_3$	outputs (active LOW)
14, 13	$2A_0$, $2A_1$	address inputs
16	V_{CC}	positive supply voltage

Fig.1 Pin configuration.

Fig.2 Logic symbol.

(a)

(b)

Fig.3 IEC logic symbol.
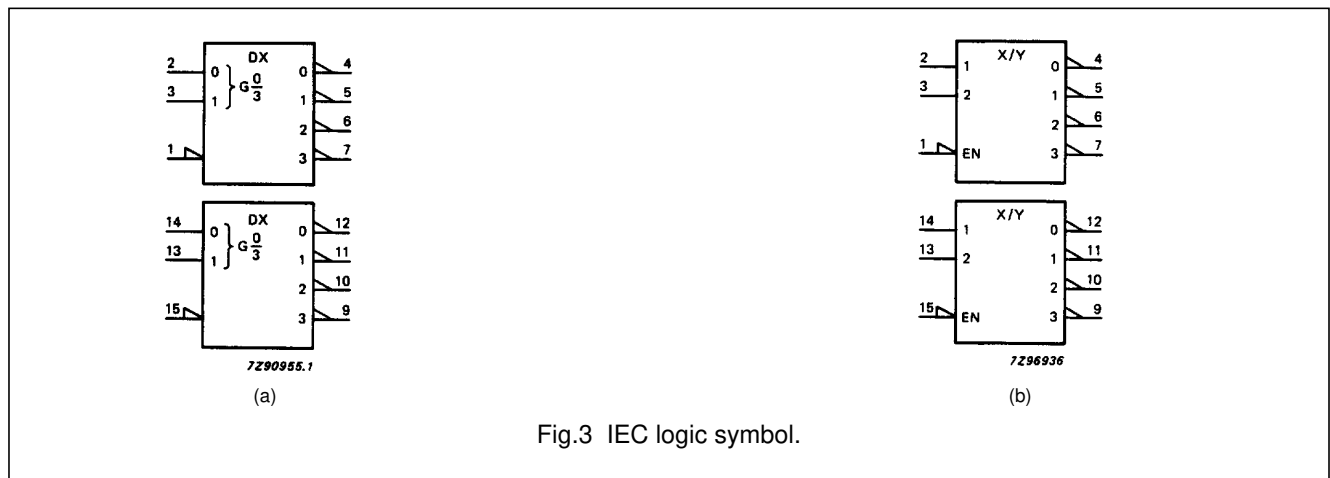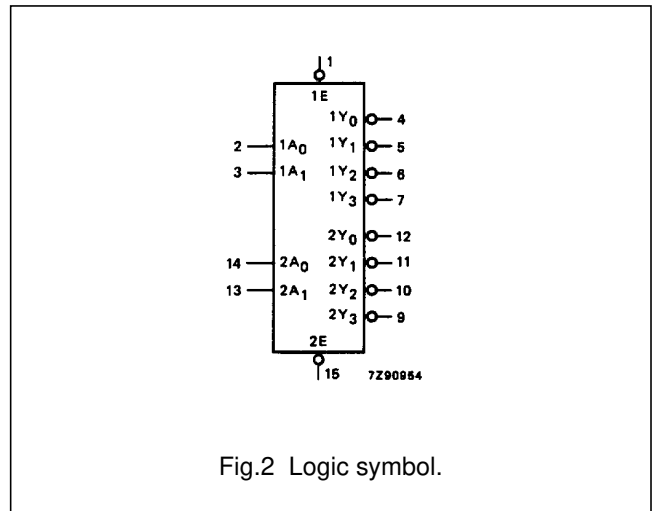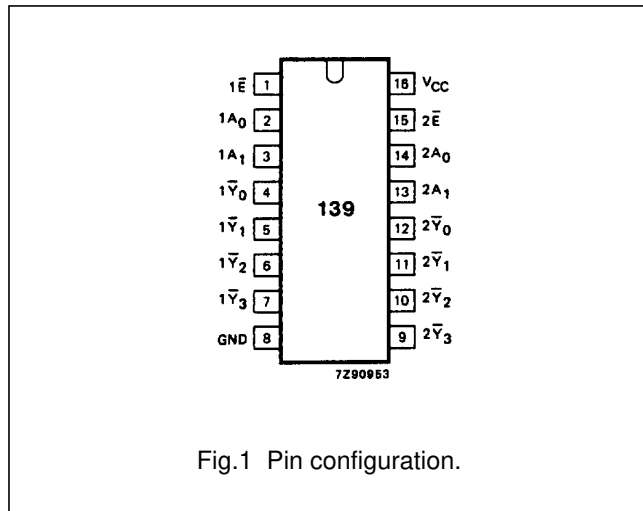
Dual 2-to-4 line decoder/demultiplexer

74HC/HCT139
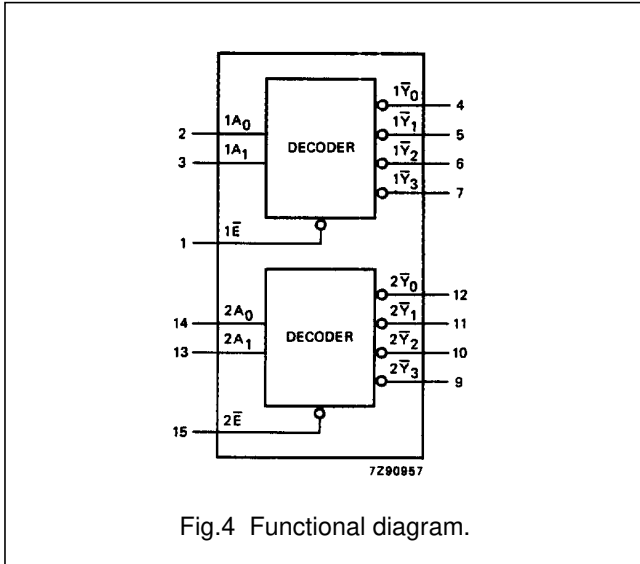
Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUTS			
$n\overline{E}$	nA_0	nA_1	$n\overline{Y}_0$	$n\overline{Y}_1$	$n\overline{Y}_2$	$n\overline{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

Notes

1. H = HIGH voltage level
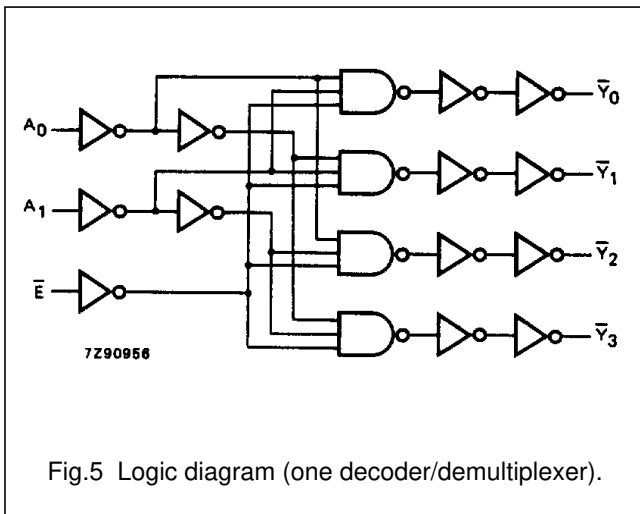   L = LOW voltage level
   X = don't care

Fig.5 Logic diagram (one decoder/demultiplexer).

Dual 2-to-4 line decoder/demultiplexer

74HC/HCT139

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS	
		74HC							V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125			
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA_n to $\overline{Y}_n$		39 14 11	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{E}$ to $n\overline{Y}_n$		33 12 10	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

Dual 2-to-4 line decoder/demultiplexer   74HC/HCT139

DC CHARACTERISTICS FOR HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$1A_n$	0.70
$2A_n$	0.70
$n\overline{E}$	1.35

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_f = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HCT						UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125		V_{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		
t_{PHL}/ t_{PLH}	propagation delay nA_n to $\overline{Y}_n$		16	34		43		51	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{E}$ to $n\overline{Y}_n$		16	34		43		51	ns	4.5	Fig.7
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

Dual 2-to-4 line decoder/demultiplexer

74HC/HCT139

AC WAVEFORMS

(1) HC   : V_M = 50%; V_I = GND to V_{CC}.
    HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6   Waveforms showing the address input (nA_n) to output ($n\overline{Y}_n$) propagation delays and the output transition times.

(1) HC   : V_M = 50%; V_I = GND to V_{CC}.
    HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7   Waveforms showing the enable input ($n\overline{E}$) to output ($n\overline{Y}_n$) propagation delays and the output transition times.
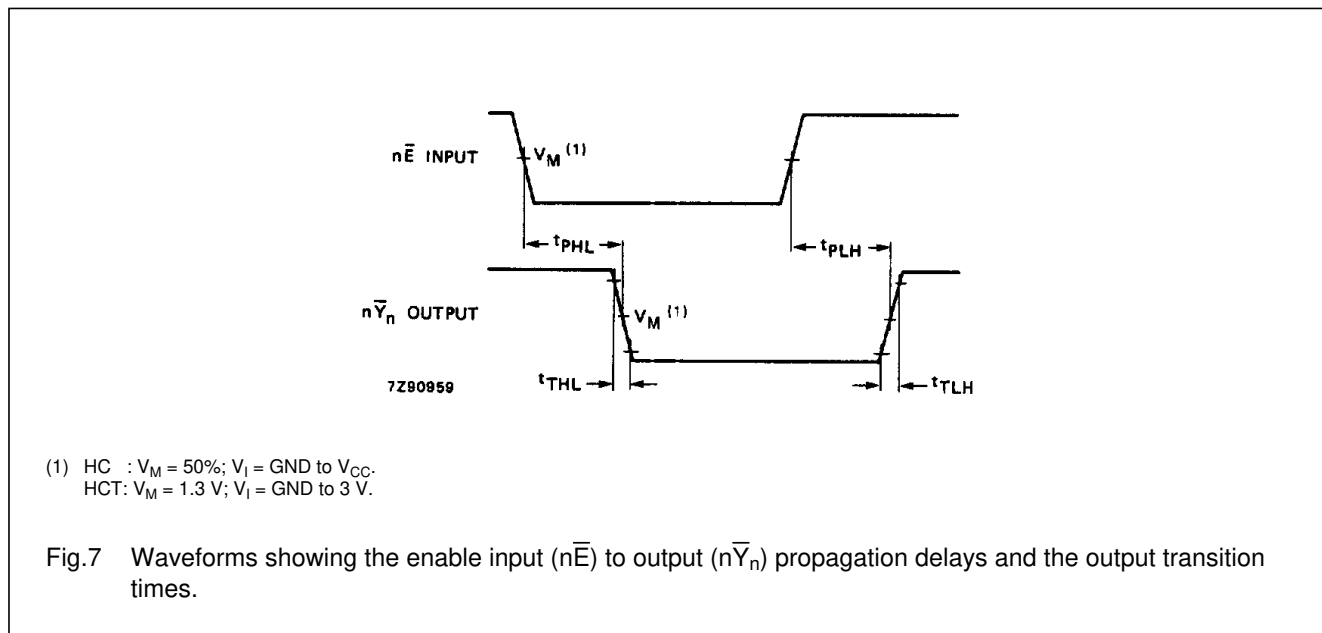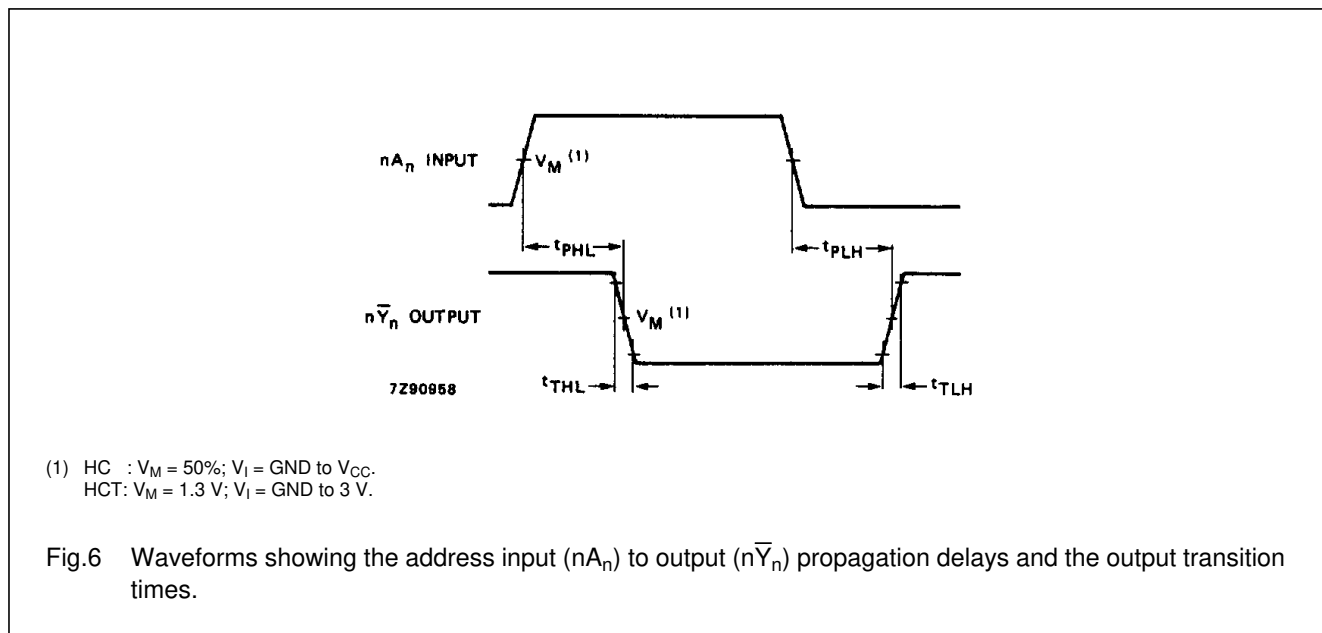
PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.