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Kind regards,

Team Nexperia

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

**74HC/HCT160**

Presettable synchronous BCD decade counter; asynchronous reset

Product specification

File under Integrated Circuits, IC06

December 1990

**Philips Semiconductors**

**PHILIPS**

# Presettable synchronous BCD decade counter; asynchronous reset

# 74HC/HCT160

## FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Asynchronous reset
- Output capability: standard
- $I_{CC}$ category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT160 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT160 are synchronous presettable decade counters which feature an internal look-ahead carry and can be used for high-speed counting.
Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).
The outputs ($Q_0$ to $Q_3$) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs ($D_0$ to $D_3$) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops ($Q_0$ to $Q_3$) to LOW level regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of $Q_0$. This pulse can be used to enable the next cascaded stage.

The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{t_{P(max)}\ (CP\ to\ TC)\ +\ t_{SU}\ (CEP\ to\ CP)}$$

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25 °C; $t_r$ = $t_f$ = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|--------|-----------|------------|------|-----|------|
| | | | HC | HCT | |
| $t_{PHL}$ | propagation delay<br>CP to $Q_n$<br>CP to TC<br>$\overline{MR}$ to $Q_n$<br>$\overline{MR}$ to TC<br>CET to TC | $C_L$ = 15 pF;<br>$V_{CC}$ = 5 V | 19<br>21<br>21<br>21<br>14 | 21<br>24<br>23<br>26<br>14 | ns<br>ns<br>ns<br>ns<br>ns |
| $t_{PLH}$ | propagation delay<br>CP to $Q_n$<br>CP to TC<br>CET to TC | | 19<br>21<br>14 | 21<br>20<br>7 | ns<br>ns<br>ns |
| $f_{max}$ | maximum clock frequency | | 61 | 31 | MHz |
| $C_I$ | input capacitance | | 3.5 | 3.5 | pF |
| $C_{PD}$ | power dissipation capacitance per package | notes 1 and 2 | 39 | 34 | pF |

**Notes**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$

   where:

   $f_i$ = input frequency in MHz
   $f_o$ = output frequency in MHz
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   $C_L$ = output load capacitance in pF
   $V_{CC}$ = supply voltage in V

2. For HC the condition is
   $V_I$ = GND to $V_{CC}$
   For HCT the condition is
   $V_I$ = GND to $V_{CC}$ − 1.5 V

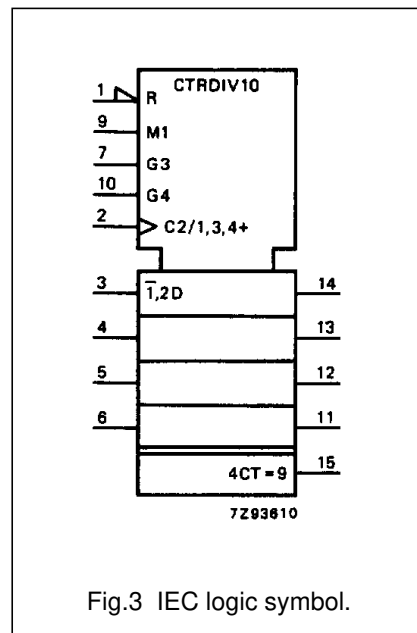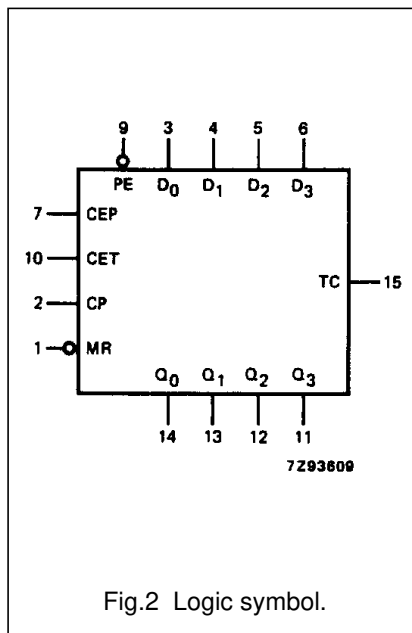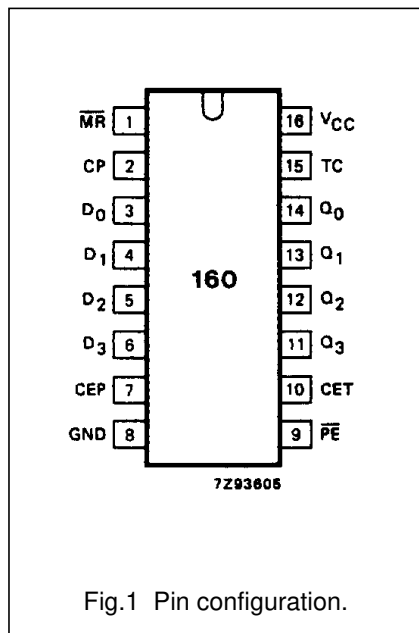## Presettable synchronous BCD decade counter; asynchronous reset

## 74HC/HCT160

### ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

### PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1 | $\overline{MR}$ | asynchronous master reset (active LOW) |
| 2 | CP | clock input (LOW-to-HIGH, edge-triggered) |
| 3, 4, 5, 6 | $D_0$ to $D_3$ | data inputs |
| 7 | CEP | count enable input |
| 8 | GND | ground (0 V) |
| 9 | $\overline{PE}$ | parallel enable input (active LOW) |
| 10 | CET | count enable carry input |
| 14, 13, 12, 11 | $Q_0$ to $Q_3$ | flip-flop outputs |
| 15 | TC | terminal count output |
| 16 | $V_{CC}$ | positive supply voltage |



Fig.1  Pin configuration.



Fig.2  Logic symbol.



Fig.3  IEC logic symbol.

Presettable synchronous BCD decade
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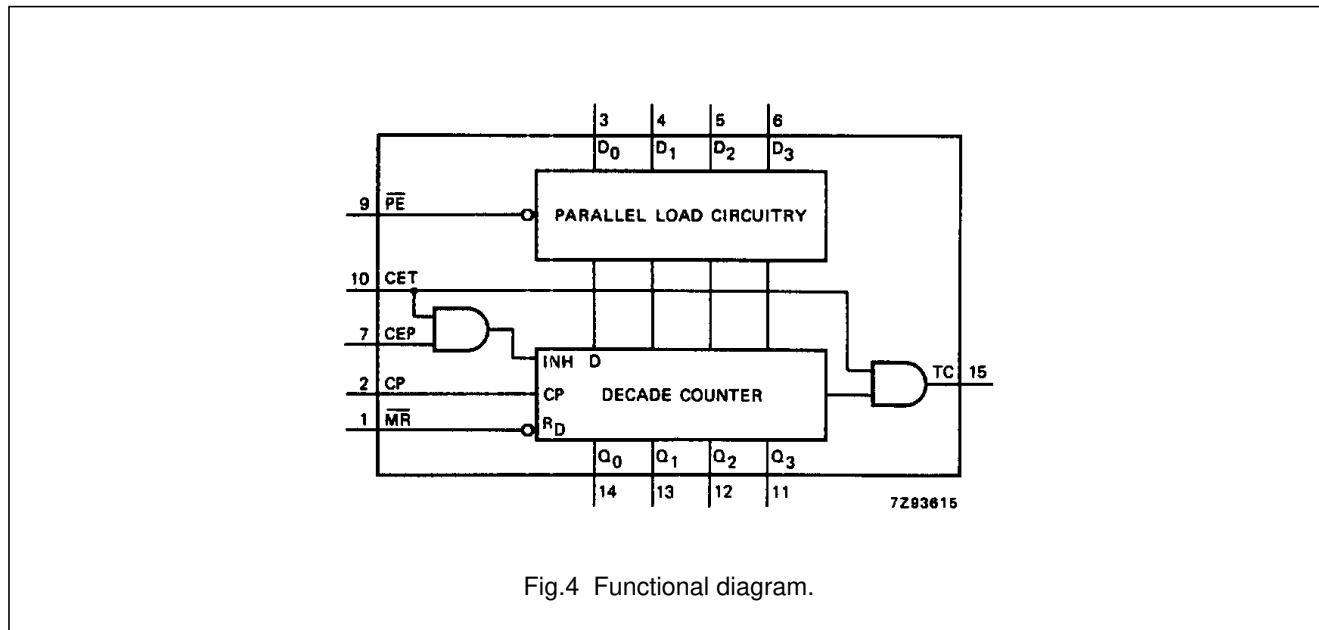


Fig.4  Functional diagram.

**FUNCTION TABLE**

| OPERATING MODE | INPUTS | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|
| | $\overline{MR}$ | CP | CEP | CET | $\overline{PE}$ | $D_n$ | $Q_n$ | TC |
| reset (clear) | L | X | X | X | X | X | L | L |
| parallel load | H | ↑ | X | X | l | l | L | L |
| | H | ↑ | X | X | l | h | H | [1] |
| count | H | ↑ | h | h | h | X | count | [1] |
| hold | H | X | l | X | h | X | $q_n$ | [1] |
| (do nothing) | H | X | X | l | h | X | $q_n$ | L |

**Notes**

1. The TC output is HIGH when CET is HIGH and the counter is at terminal count (HLLH).
    H = HIGH voltage level
    h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
    L = LOW voltage level
    l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
    q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
    X = don't care
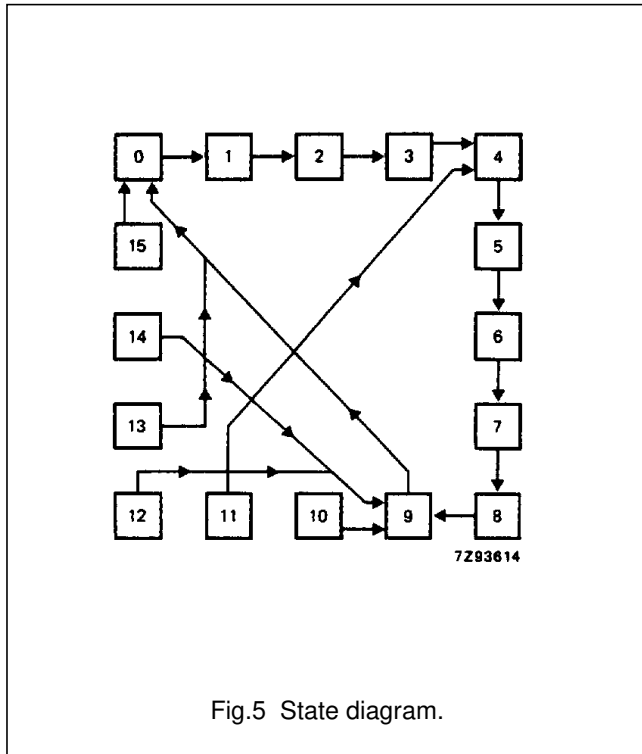    ↑ = LOW-to-HIGH CP transition
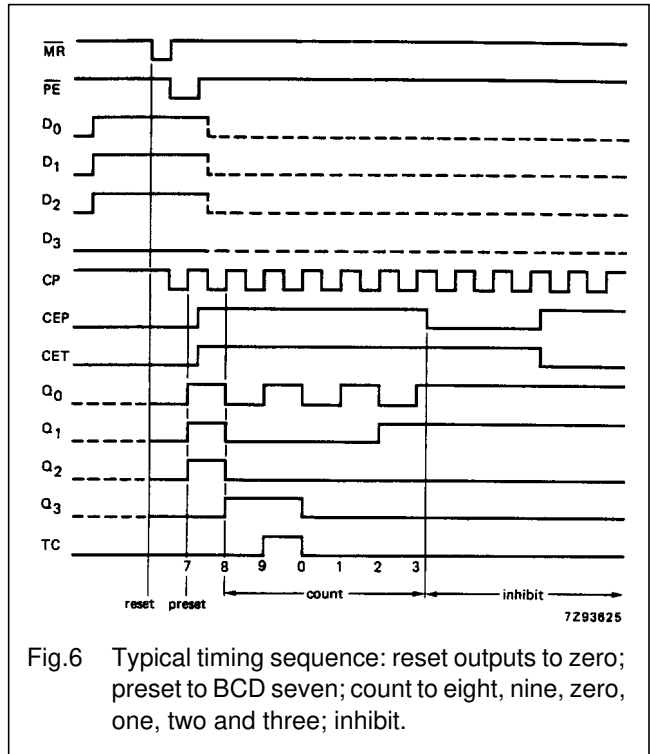
Fig.5  State diagram.



Fig.6  Typical timing sequence: reset outputs to zero;
preset to BCD seven; count to eight, nine, zero,
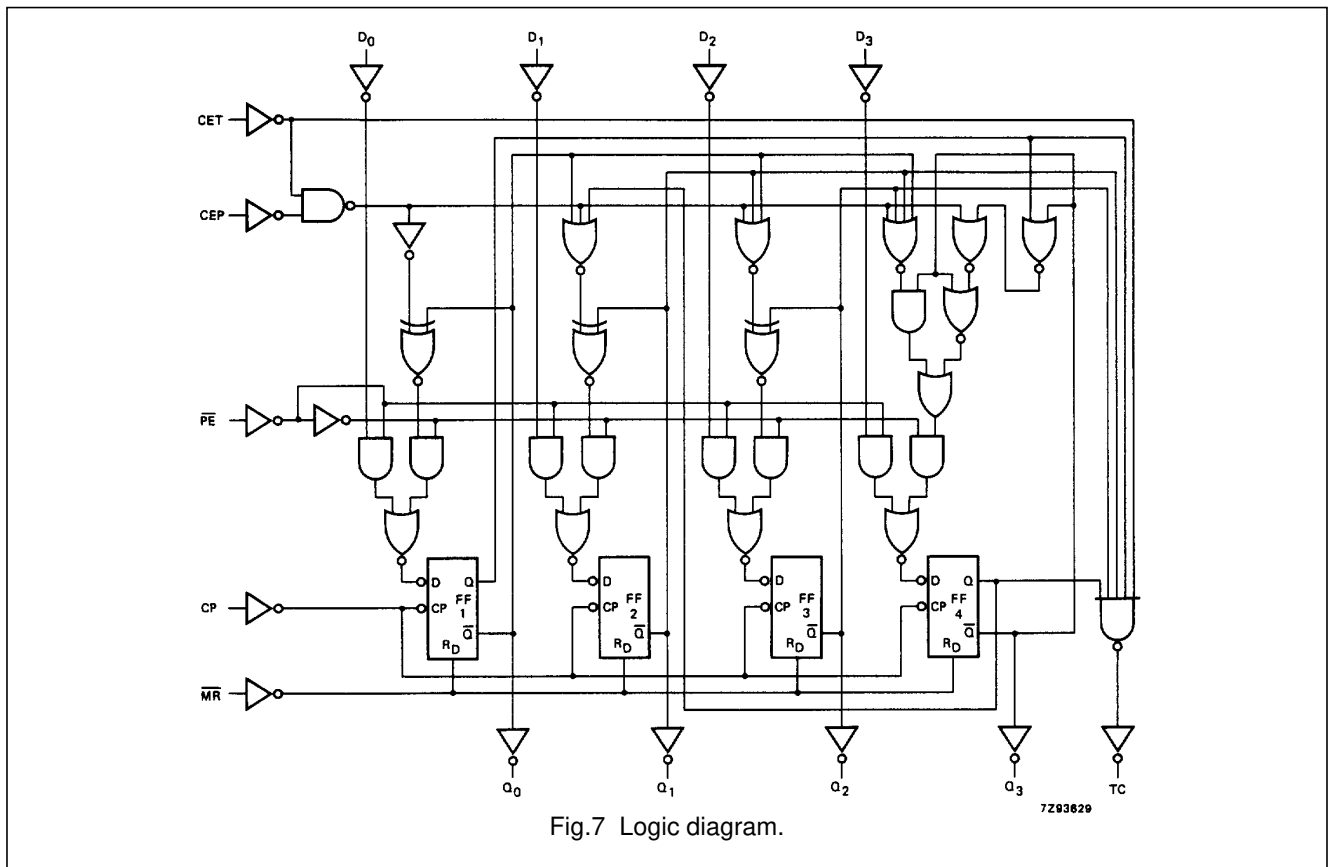one, two and three; inhibit.



Fig.7  Logic diagram.

# Presettable synchronous BCD decade counter; asynchronous reset

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
$I_{CC}$ category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | **74HC** | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay CP to $Q_n$ | | 61 22 18 | 185 37 31 | | 230 46 39 | | 280 56 48 | ns | 2.0 4.5 6.0 | Fig. 8 |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay CP to TC | | 69 25 20 | 215 43 31 | | 270 54 46 | | 325 65 55 | ns | 2.0 4.5 6.0 | Fig. 8 |
| $t_{PHL}$ | propagation delay $\overline{MR}$ to $Q_n$ | | 69 25 20 | 210 42 36 | | 265 53 45 | | 315 63 54 | ns | 2.0 4.5 6.0 | Fig. 9 |
| $t_{PHL}$ | propagation delay $\overline{MR}$ to TC | | 69 25 20 | 220 44 37 | | 275 55 47 | | 330 66 56 | ns | 2.0 4.5 6.0 | Fig. 9 |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay CET to TC | | 47 17 14 | 150 30 26 | | 190 38 33 | | 225 45 38 | ns | 2.0 4.5 6.0 | Fig. 10 |
| $t_{THL}$/ $t_{TLH}$ | output transition time | | 19 7 6 | 75 15 13 | | 95 19 16 | | 110 22 19 | ns | 2.0 4.5 6.0 | Figs 8 and 10 |
| $t_W$ | clock pulse width HIGH or LOW | 80 16 14 | 22 8 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig. 8 |
| $t_W$ | master reset pulse width LOW | 80 16 14 | 28 10 8 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig. 9 |
| $t_{rem}$ | removal time $\overline{MR}$ to CP | 100 20 17 | 30 11 9 | | 125 25 21 | | 150 30 26 | | ns | 2.0 4.5 6.0 | Fig. 9 |
| $t_{su}$ | set-up time $D_n$ to CP | 80 16 14 | 22 8 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig. 11 |
| $t_{su}$ | set-up time $\overline{PE}$ to CP | 135 27 23 | 41 15 12 | | 170 34 29 | | 205 41 35 | | ns | 2.0 4.5 6.0 | Fig. 11 |

Presettable synchronous BCD decade
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74HC/HCT160

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{su}$ | set-up time CEP, CET to CP | 200 40 34 | 63 23 18 | | 250 50 43 | | 300 60 51 | | ns | 2.0 4.5 6.0 | Fig. 12 |
| $t_h$ | hold time $D_n$ to CP | 0 0 0 | −17 −6 −5 | | 0 0 0 | | 0 0 0 | | ns | 2.0 4.5 6.0 | Figs 11 and 12 |
| $t_h$ | hold time $\overline{PE}$ to CP | 0 0 0 | −41 −15 −12 | | 0 0 0 | | 0 0 0 | | ns | 2.0 4.5 6.0 | Figs 11 and 12 |
| $t_h$ | hold time CEP, CET to CP | 0 0 0 | −58 −21 −17 | | 0 0 0 | | 0 0 0 | | ns | 2.0 4.5 6.0 | Figs 11 and 12 |
| $f_{max}$ | maximum clock pulse frequency | 6.0 30 35 | 18 55 66 | | 4.8 24 28 | | 4.0 20 24 | | MHz | 2.0 4.5 6.0 | Fig. 8 |

Presettable synchronous BCD decade
counter; asynchronous reset

74HC/HCT160

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
$I_{CC}$ category: MSI

**Note to HCT types**

The value of additional quiescent supply current ($\Delta I_{CC}$) for unit load of 1 is given in the family specifications.
To determine $\Delta I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD   COEFFICIENT |
|-------|--------------------------|
| $\overline{MR}$ | 0.95 |
| CP | 0.80 |
| CEP | 0.25 |
| $D_n$ | 0.25 |
| CET | 1.05 |
| $\overline{PT}$ | 0.30 |

## Presettable synchronous BCD decade counter; asynchronous reset

**74HC/HCT160**

### AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) 74HCT +25 min. | typ. | max. | −40 to +85 min. | max. | −40 to +125 min. | max. | UNIT | $V_{CC}$ (V) | WAVEFORMS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | propagation delay CP to $Q_n$ | | 25 | 43 | | 54 | | 65 | ns | 4.5 | Fig. 8 |
| $t_{PHL}$ | propagation delay CP to TC | | 28 | 48 | | 60 | | 72 | ns | 4.5 | Fig. 8 |
| $t_{PLH}$ | propagation delay CP to TC | | 23 | 39 | | 49 | | 59 | ns | 4.5 | Fig. 8 |
| $t_{PHL}$ | propagation delay $\overline{MR}$ to $Q_n$ | | 27 | 50 | | 63 | | 75 | ns | 4.5 | Fig. 9 |
| $t_{PHL}$ | propagation delay $\overline{MR}$ to TC | | 30 | 50 | | 63 | | 75 | ns | 4.5 | Fig. 9 |
| $t_{PHL}$ | propagation delay CET to TC | | 17 | 35 | | 44 | | 53 | ns | 4.5 | Fig. 10 |
| $t_{PLH}$ | propagation delay CET to TC | | 9 | 17 | | 21 | | 26 | ns | 4.5 | Fig. 10 |
| $t_{THL}/t_{TLH}$ | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Figs 8 and 10 |
| $t_W$ | clock pulse width HIGH or LOW | 16 | 8 | | 20 | | 24 | | ns | 4.5 | Fig. 8 |
| $t_W$ | master reset pulse width LOW | 20 | 11 | | 25 | | 30 | | ns | 4.5 | Fig. 9 |
| $t_{rem}$ | removal time $\overline{MR}$ to CP | 20 | 9 | | 25 | | 30 | | ns | 4.5 | Fig. 9 |
| $t_{su}$ | set-up time $D_n$ to CP | 18 | 10 | | 25 | | 30 | | ns | 4.5 | Fig. 11 |
| $t_{su}$ | set-up time $\overline{PE}$ to CP | 30 | 18 | | 44 | | 53 | | ns | 4.5 | Fig. 11 |
| $t_{su}$ | set-up time CEP, CET to CP | 50 | 30 | | 63 | | 75 | | ns | 4.5 | Fig. 12 |
| $t_h$ | hold time $D_n$ to CP | 0 | −8 | | 0 | | 0 | | ns | 4.5 | Figs 11 and 12 |
| $t_h$ | hold time $\overline{PE}$ to CP | 0 | −13 | | 0 | | 0 | | ns | 4.5 | Figs 11 and 12 |
| $t_h$ | hold time CEP, CET to CP | 0 | −21 | | 0 | | 0 | | ns | 4.5 | Figs 11 and 12 |
| $f_{max}$ | maximum clock pulse frequency | 16 | 28 | | 13 | | 11 | | MHz | 4.5 | Fig. 8 |

### PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.