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CMOS Digital Integrated Circuits Silicon Monolithic

74HC164D

1. Functional Description

• 8-Bit Shift Register (S-IN, P-OUT)

2. General

The 74HC164D is a high speed CMOS 8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER fabricated with silicon gate C2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of a serial-in, parallel-out 8-bit shift register with a CK input and an overriding $\overline{\text{CLR}}$ input.

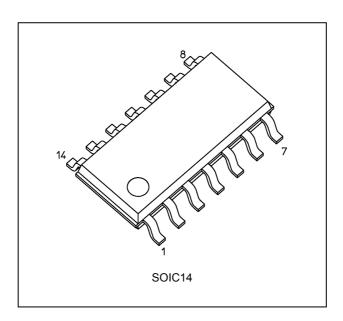
Two serial data inputs (A, B) are provided so that one may be used as a data enable.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

3. Features

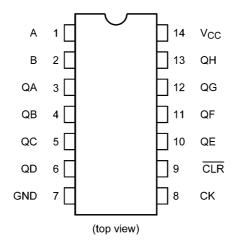
- (1) High speed: $f_{MAX} = 58 \text{ MHz}$ (typ.) at $V_{CC} = 5 \text{ V}$
- (2) Low power dissipation: $I_{CC} = 4.0 \mu A \text{ (max)}$ at $T_a = 25 \text{ °C}$
- (3) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- (4) Wide operating voltage range: $V_{CC(opr)} = 2.0$ to 6.0 V

4. Packaging

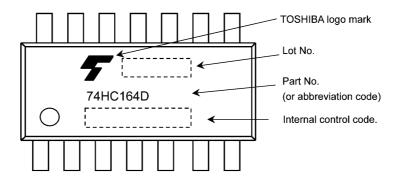




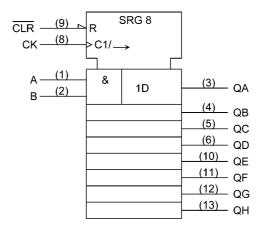
5. Pin Assignment



6. Marking



7. IEC Logic Symbol





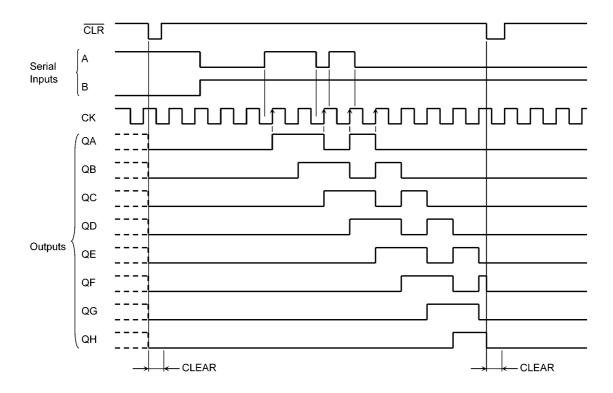
8. Truth Table

	Inputs				Out	puts	
CLR	СК	Seri	al IN	QA	QB		QH
CLK	5	A	В	QA	Qb		QII
L	Х	Х	Х	L	L		L
Н		Х	Х		No CI	nange	
Н		L	Х	L	QAn		QGn
Н		Х	L	L QAn QC			QGn
Н	<u></u>	Ι	Н	Н	QAn		QGn

X: Don't care

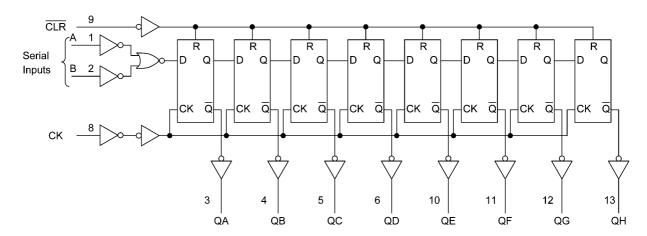
QAn to QGn: The level of QA to QG, respectively, before the most recent positive edge of the CK.

9. Timing Diagrams





10. System Diagram



11. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V _{CC}		-0.5 to 7.0	V
Input voltage	V _{IN}		-0.5 to V _{CC} + 0.5	V
Output voltage	V _{OUT}		-0.5 to V _{CC} + 0.5	V
Input diode current	I _{IK}		±20	mA
Output diode current	I _{OK}		±20	mA
Output current	I _{OUT}		±25	mA
V _{CC} /ground current	I _{CC}		±50	mA
Power dissipation	P _D	(Note 1)	500	mW
Storage temperature	T _{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: P_D derates linearly with -8 mW/°C above 85 °C

12. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V _{CC}		2.0 to 6.0	V
Input voltage	V _{IN}		0 to V _{CC}	V
Output voltage	V _{OUT}		0 to V _{CC}	٧
Operating temperature	T _{opr}	_	-40 to 125	ç
Input rise and fall times	t _r ,t _f		0 to 50	μS

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.



13. Electrical Characteristics

13.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	١	V _{CC} (V)	Min	Тур.	Max	Unit
High-level input voltage	V _{IH}	_		2.0	1.50	_	_	V
				4.5	3.15	_	_	
				6.0	4.20	_	_	
Low-level input voltage	V _{IL}	_		2.0		_	0.50	V
				4.5		_	1.35	
				6.0		_	1.80	
High-level output voltage	V _{OH}	$V_{IN} = V_{IH}$ or V_{IL}	I _{OH} = -20 μA	2.0	1.9	2.0	_	V
				4.5	4.4	4.5	_	
				6.0	5.9	6.0	_	
			I _{OH} = -4 mA	4.5	4.18	4.31	_	
			I _{OH} = -5.2 mA	6.0	5.68	5.80	_	
Low-level output voltage	V _{OL}	$V_{IN} = V_{IH}$ or V_{IL}	I _{OL} = 20 μA	2.0	_	0.0	0.1	V
				4.5	_	0.0	0.1	
				6.0	_	0.0	0.1	
			I _{OL} = 4 mA	4.5	_	0.17	0.26	
			I _{OL} = 5.2 mA	6.0	_	0.18	0.26	
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND		6.0	_	_	±0.1	μА
Quiescent supply current	I _{CC}	$V_{IN} = V_{CC}$ or GND		6.0	_	_	4.0	μА

13.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V _{CC} (V)	Min	Max	Unit
High-level input voltage	V _{IH}	_		2.0	1.50	_	V
				4.5	3.15	_]
				6.0	4.20	_	
Low-level input voltage	V _{IL}	_		2.0	_	0.50	V
				4.5	_	1.35	
				6.0	_	1.80	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 μA	2.0	1.9	_	V
				4.5	4.4	_]
				6.0	5.9	_	
			I _{OH} = -4 mA	4.5	4.13	_	
			I _{OH} = -5.2 mA	6.0	5.63	_	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	2.0	_	0.1	V
				4.5	_	0.1	
				6.0	_	0.1	
			I _{OL} = 4 mA	4.5	_	0.33	
			I _{OL} = 5.2 mA	6.0	_	0.33]
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND		6.0	_	±1.0	μА
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		6.0	_	40.0	μА



13.3. DC Characteristics (Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Symbol	Test Condition	1	V _{CC} (V)	Min	Max	Unit
High-level input voltage	V _{IH}	_		2.0	1.50	_	V
				4.5	3.15	_	
				6.0	4.20	_]
Low-level input voltage	V _{IL}	_		2.0	_	0.50	V
				4.5	_	1.35	
				6.0	_	1.80	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 μA	2.0	1.9	_	V
				4.5	4.4	_	
				6.5	5.9	_	
			I _{OH} = -4 mA	4.5	3.7	_	
			I _{OH} = -5.2 mA	6.0	5.2	_	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	2.0	_	0.1	V
				4.5	_	0.1	
				6.0	_	0.1	
			I _{OL} = 4 mA	4.5	_	0.4]
			I _{OL} = 5.2 mA	6.0	_	0.4	
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND		6.0	_	±1.0	μА
Quiescent supply current	I _{CC}	$V_{IN} = V_{CC}$ or GND		6.0	_	160	μА

13.4. Timing Requirements (Unless otherwise specified, T_a = 25 °C, Input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	_	2.0	75	ns
			4.5	15	
			6.0	13	
Minimum pulse width (CLR)	t _{w(L)}	_	2.0	80	ns
			4.5	16	
			6.0	14	
Minimum setup time (A, B)	t _S	_	2.0	50	ns
			4.5	10	
			6.0	9	
Minimum hold time (A, B)	t _h	_	2.0	5	ns
			4.5	5	
			6.0	5	
Minimum removal time (CLR)	t _{rem}	_	2.0	5	ns
			4.5	5	
			6.0	5	
Clock frequency	f	_	2.0	6	MHz
			4.5	31	
			6.0	36	



13.5. Timing Requirements (Unless otherwise specified, T_a = -40 to 85 °C, Input: t_f = t_f = 6 ns)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	_	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum pulse width (CLR)	t _{w(L)}	_	2.0	100	ns
			4.5	20	
			6.0	17	
Minimum setup time (A, B)	t _S	_	2.0	65	ns
			4.5	13	
			6.0	11	
Minimum hold time (A, B)	t _h	_	2.0	5	ns
			4.5	5	
			6.0	5	
Minimum removal time (CLR)	t _{rem}	_	2.0	5	ns
			4.5	5	
			6.0	5	
Clock frequency	f	_	2.0	5	MHz
			4.5	25	
			6.0	29	

13.6. Timing Requirements (Unless otherwise specified, T_a = -40 to 125 °C, Input: t_f = t_f = 6 ns)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	_	2.0	120	ns
			4.5	24	
			6.0	20]
Minimum pulse width (CLR)	t _{w(L)}	_	2.0	120	ns
			4.5	24	
			6.0	20	
Minimum setup time (A, B)	t _S	_	2.0	90	ns
			4.5	18	
			6.0	15	1
Minimum hold time (A, B)	t _h	_	2.0	5	ns
			4.5	5	
			6.0	5	1
Minimum removal time (CLR)	t _{rem}	_	2.0	5	ns
			4.5	5	
			6.0	5	1
Clock frequency	f	_	2.0	4	MHz
			4.5	20]
			6.0	24	



13.7. AC Characteristics (Unless otherwise specified, C_L = 15 pF, V_{CC} = 5 V, T_a = 25 °C, Input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Output transition time	t_{TLH}, t_{THL}	_	_	4	8	ns
Propagation delay time (CK-Qn)	t _{PLH} ,t _{PHL}	_	_	15	27	
Propagation delay time (CLR-Qn)	t _{PHL}	_	_	16	30	
Maximum clock frequency	f _{MAX}	_	33	58	_	MHz

13.8. AC Characteristics (Unless otherwise specified, $C_L = 50$ pF, $T_a = 25$ °C, Input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Note	V _{CC} (V)	Min	Тур.	Max	Unit
Output transition time	t_{TLH}, t_{THL}		2.0	_	25	75	ns
			4.5	_	7	15	
			6.0	_	6	13	
Propagation delay time (CK-Qn)	t _{PLH} ,t _{PHL}		2.0	_	57	160	ns
			4.5	_	19	32	
			6.0	_	16	27	
Propagation delay time (CLR-Qn)	t _{PHL}		2.0	_	60	175	ns
			4.5	_	20	35	
			6.0	_	17	30	
Maximum clock frequency	f _{MAX}		2.0	6	18	_	MHz
			4.5	31	53	_	
			6.0	36	62	_	
Input capacitance	C _{IN}				3		pF
Power dissipation capacitance	C _{PD}	(Note 1)	_	_	30	_	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

13.9. AC Characteristics

(Unless otherwise specified, $C_L = 50$ pF, $T_a = -40$ to 85 °C, Input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	V _{CC} (V)	Min	Max	Unit
Output transition time	t _{TLH} ,t _{THL}	2.0	_	95	ns
		4.5	_	19	
		6.0		16	
Propagation delay time (CK-Qn)	t _{PLH} ,t _{PHL}	2.0	_	200	ns
		4.5	_	40	
		6.0	_	34	
Propagation delay time (CLR-Qn)	t _{PHL}	2.0	_	220	ns
		4.5	_	44	
		6.0	_	37	
Maximum clock frequency	f _{MAX}	2.0	5	_	MHz
		4.5	25		
		6.0	29		



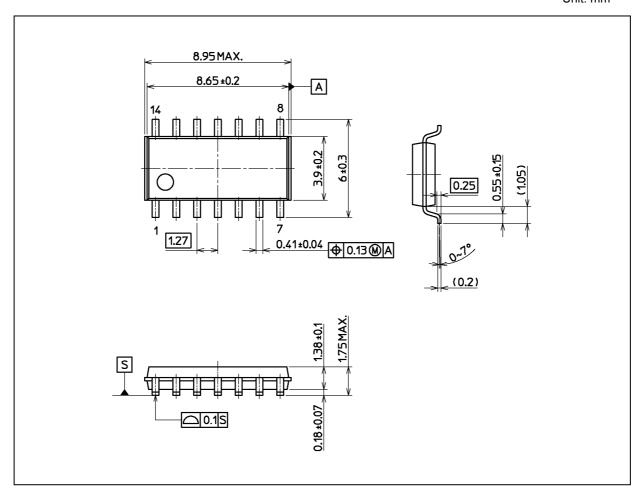
13.10. AC Characteristics (Unless otherwise specified, C_L = 50 pF, T_a = -40 to 125 °C, Input: t_r = t_f = 6 ns)

Characteristics	Symbol	V _{CC} (V)	Min	Max	Unit
Output transition time	t _{TLH} ,t _{THL}	2.0	_	110	ns
		4.5	_	22	
		6.0	_	19	
Propagation delay time (CK-Qn)	t _{PLH} ,t _{PHL}	2.0	_	240	ns
		4.5	_	48	
		6.0	_	41	
Propagation delay time (CLR-Qn)	t _{PHL}	2.0	_	265	ns
		4.5	_	53	
		6.0	_	45	
Maximum clock frequency	f _{MAX}	2.0	4	_	MHz
		4.5	20	_	
		6.0	24	_	



Package Dimensions

Unit: mm



Weight: 0.13 g (typ.)

	Package Name(s)
Nickname: SOIC14	



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