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CMOS Digital Integrated Circuits Silicon Monolithic

74HC374D

1. Functional Description

Octal D-Type Flip Flop with 3-State Outputs

2. General

The 74HC374D is a high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{\text{OE}}$).

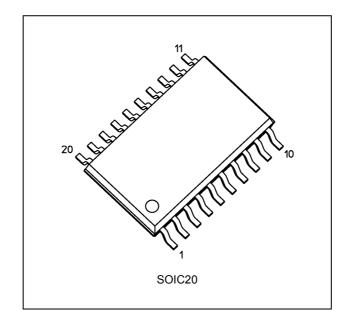
When the input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

3. Features

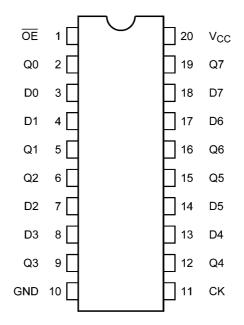
- (1) High speed: f_{MAX} = 90 MHz (typ.) at V_{CC} = 6.0 V
- (2) Low power dissipation: I_{CC} = 4.0 μ A (max) at T_a = 25 °C
- (3) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- (4) Wide operating voltage range: $V_{CC(opr)} = 2.0 \text{ V}$ to 6.0 V

4. Packaging

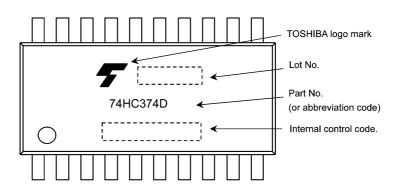


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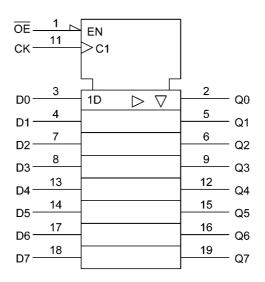
5. Pin Assignment



6. Marking



7. IEC Logic Symbol



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8. Truth Table

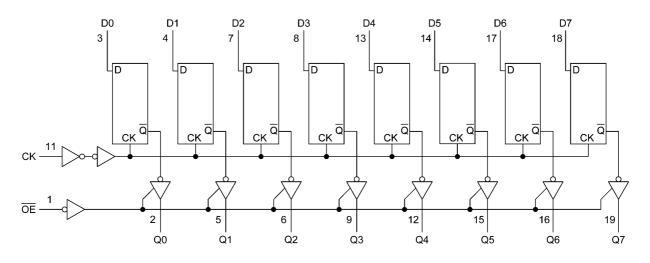
	Inputs		Output
ŌĒ	СК	D	Output
н	Х	Х	Z
L		Х	Qn
L		L	L
L		н	н

X: Don't care

Z: High impedance

Qn: No change

9. System Diagram



10. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V _{CC}		-0.5 to 7.0	V
Input voltage	V _{IN}		-0.5 to V _{CC} + 0.5	V
Output voltage	V _{OUT}		-0.5 to V _{CC} + 0.5	V
Input diode current	I _{IK}		±20	mA
Output diode current	I _{ОК}		±20	mA
Output current	I _{OUT}		±35	mA
V _{CC} /ground current	I _{CC}		±75	mA
Power dissipation	PD	(Note 1)	500	mW
Storage temperature	T _{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: PD derates linearly with -8 mW/°C above 85 °C

11. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V _{CC}	—	2.0 to 6.0	V
Input voltage	V _{IN}	_	0 to V_{CC}	V
Output voltage	V _{OUT}	_	0 to V _{CC}	V
Operating temperature	T _{opr}	—	-40 to 125	°C
Input rise and fall times	t _r ,t _f		0 to 50	μS

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

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12. Electrical Characteristics

12.1. DC Characteristics (Unless otherwise specified, $T_a = 25$ °C)

Characteristics	Symbol	Test Condition	1	V _{CC} (V)	Min	Тур.	Max	Unit
High-level input voltage	V _{IH}	—		2.0	1.50	_	_	V
				4.5	3.15	_	_	
				6.0	4.20	_	_	
Low-level input voltage	VIL	—		2.0	_	_	0.50	V
				4.5		—	1.35	
				6.0		_	1.80	
High-level output voltage	V _{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	I _{OH} = -20 μA	2.0	1.9	2.0		V
				4.5	4.4	4.5		
				6.0	5.9	6.0		
			I _{OH} = -6 mA	4.5	4.18	4.31		
			I _{OH} = -7.8 mA	6.0	5.68	5.80		
Low-level output voltage	V _{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	I_{OL} = 20 μ A	2.0		0.0	0.1	V
				4.5		0.0	0.1	
				6.0		0.0	0.1	
			I _{OL} = 6 mA	4.5		0.17	0.26	
			I _{OL} = 7.8 mA	6.0		0.18	0.26	
3-state output OFF-state leakage current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		6.0	_	_	±0.5	μA
Input leakage current	I _{IN}	$V_{IN} = V_{CC}$ or GND		6.0	_	—	±0.1	μA
Quiescent supply current	I _{CC}	$V_{IN} = V_{CC} \text{ or } GND$ $I_O = 0 \text{ A}$		6.0	—	_	4.0	μA

12.2. DC Characteristics (Unless otherwise specified, $T_a = -40$ to 85 °C)

Characteristics	Symbol	Test Condition	1	V _{CC} (V)	Min	Max	Unit
High-level input voltage	V _{IH}	—		2.0	1.50	—	V
				4.5	3.15	_]
				6.0	4.20	_	
Low-level input voltage	VIL	—		2.0	_	0.50	V
				4.5	_	1.35]
				6.0	_	1.80	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 μA	2.0	1.9	—	V
				4.5	4.4	_	
				6.0	5.9	_	
			I _{OH} = -6 mA	4.5	4.13	_	
			I _{OH} = -7.8 mA	6.0	5.63	_	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	2.0	_	0.1	V
				4.5	_	0.1	
				6.0	_	0.1	
			I _{OL} = 6 mA	4.5	_	0.33	
			I _{OL} = 7.8 mA	6.0	_	0.33	
3-state output OFF-state leakage current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		6.0	_	±5.0	μΑ
Input leakage current	I _{IN}	$V_{IN} = V_{CC}$ or GND		6.0		±1.0	μA
Quiescent supply current	I _{CC}	$V_{IN} = V_{CC}$ or GND $I_{O} = 0$ A		6.0	_	40.0	μΑ

12.3. DC Characteristics (Unless otherwise specified, $T_a = -40$ to 125 °C)

Characteristics	Symbol	Test Condition	I	V _{CC} (V)	Min	Max	Unit
High-level input voltage	V _{IH}	—		2.0	1.50	_	V
				4.5	3.15	_	
				6.0	4.20	_]
Low-level input voltage	V _{IL}	—		2.0	_	0.50	V
				4.5	_	1.35	
				6.0	_	1.80	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 μA	2.0	1.9	_	V
				4.5	4.4	_	
				6.0	5.9	—]
			I _{OH} = -6 mA	4.5	3.7	—	
			I _{OH} = -7.8 mA	6.0	5.2	—	
Low-level output voltage	V _{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	I _{OL} = 20 μA	2.0	_	0.1	V
				4.5	_	0.1	
				6.0	_	0.1	
			I _{OL} = 6 mA	4.5	_	0.4]
			I _{OL} = 7.8 mA	6.0	_	0.4]
3-state output OFF-state leakage current	I _{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or } GND$		6.0		±10.0	μA
Input leakage current	I _{IN}	$V_{IN} = V_{CC}$ or GND		6.0	_	±1.0	μA
Quiescent supply current	I _{CC}	$V_{IN} = V_{CC}$ or GND $I_{O} = 0$ A		6.0	_	160.0	μA

12.4. Timing Requirements (Unless otherwise specified, $T_a = 25$ °C, Input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Limit	Unit
Minimum pulse width	$t_{w(L)}, t_{w(H)}$	_	2.0	_	75	ns
(CK)			4.5	—	15	
			6.0	_	13	
Minimum setup time (Dn)	ts	_	2.0	_	75	ns
			4.5	—	15	
			6.0	_	13	
Minimum hold time	t _h	_	2.0	_	0	ns
(Dn)			4.5	—	0	
			6.0	_	0	
Clock frequency	f	—	2.0	—	6	MHz
			4.5	_	31	
			6.0	_	36	

12.5. Timing Requirements

(Unless otherwise specified, $T_a = -40$ to 85 °C, Input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Limit	Unit
Minimum pulse width	t _{w(L)} ,t _{w(H)}	—	2.0	95	ns
(CK)			4.5	19	
			6.0	16	
Minimum setup time	ts		2.0	95	ns
(Dn)			4.5	19	
			6.0	16	
Minimum hold time	t _h		2.0	0	ns
(Dn)			4.5	0	
			6.0	0	
Clock frequency	f		2.0	5	MHz
			4.5	25	
			6.0	29	

12.6. Timing Requirements (Unless otherwise specified, T_a = -40 to 125 °C, Input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Limit	Unit
Minimum pulse width	t _{w(L)} ,t _{w(H)}	_	2.0	120	ns
(CK)			4.5	24	
			6.0	20	
Minimum setup time (Dn)	ts	_	2.0	120	ns
			4.5	24	
			6.0	20	
Minimum hold time	t _h	_	2.0	0	ns
(Dn)			4.5	0	
			6.0	0	
Clock frequency	f	_	2.0	4	MHz
			4.5	20]
			6.0	24	

12.7. AC Characteristics (Unless otherwise specified, $T_a = 25$ °C, Input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Note	Test Condition	C _L (pF)	V _{CC} (V)	Min	Тур.	Max	Unit
Output transition time	t _{TLH} ,t _{THL}		_	50	2.0	_	20	60	ns
					4.5	_	6	12	
					6.0		5	10	
Propagation delay time	t _{PLH} ,t _{PHL}		—	50	2.0	_	45	140	ns
(CK-Q)					4.5	_	15	28	
					6.0	_	13	24	
				150	2.0	_	60	190	
					4.5	_	20	38	
					6.0	_	17	32	
Output enable time	t _{PZL} ,t _{PZH}		$R_L = 1 k\Omega$	50	2.0	_	39	135	ns
					4.5	_	13	27	
					6.0		11	23	
				150	2.0		54	185	
					4.5		18	37	
					6.0	_	15	31	
Output disable time	t _{PLZ} ,t _{PHZ}		$R_L = 1 k\Omega$	50	2.0	_	30	135	ns
					4.5	_	13	27	
					6.0	_	12	23	
Maximum clock frequency	f _{MAX}		_	50	2.0	6	18	_	MHz
					4.5	31	75	_	
					6.0	36	90	_	
Input capacitance	C _{IN}		_				3	_	pF
Output capacitance	C _{OUT}					_	4	_	pF
Power dissipation capacitance	C _{PD}	(Note 1)	_				11	_	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

 $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per latch)

And the total C_{PD} when n pcs of latch operate can be gained by the following equation.

 C_{PD} (total) = 22 + 16 \times n

12.8. AC Characteristics (Unless otherwise specified, $T_a = -40$ to 85 °C, Input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	C _L (pF)	V _{CC} (V)	Min	Max	Unit			
Output transition time	t _{TLH} ,t _{THL}		50	2.0	_	75	ns			
				4.5	_	15	1			
				6.0	_	13	1			
Propagation delay time	t _{PLH} ,t _{PHL}	_	50	2.0	_	175	ns			
(CK-Q)				4.5	_	35				
				6.0	_	30]			
			150	2.0	_	240				
				4.5	_	48				
				6.0	_	41				
Output enable time	t _{PZL} ,t _{PZH}	R _L = 1 kΩ	50	2.0	_	170	ns			
				4.5	_	34	-			
				6.0	_	29				
			150	2.0	_	230				
				4.5	_	46]			
				6.0	_	39]			
Output disable time	t _{PLZ} ,t _{PHZ}	R _L = 1 kΩ	50	2.0	_	170	ns			
				4.5	_	34]			
				6.0	_	29				
Maximum clock frequency	f _{MAX}	_	50	2.0	5	_	MHz			
							4.5	25	_]
				6.0	29	_]			

12.9. AC Characteristics (Unless otherwise specified, T_a = -40 to 125 °C, Input: t_r = t_f = 6 ns)

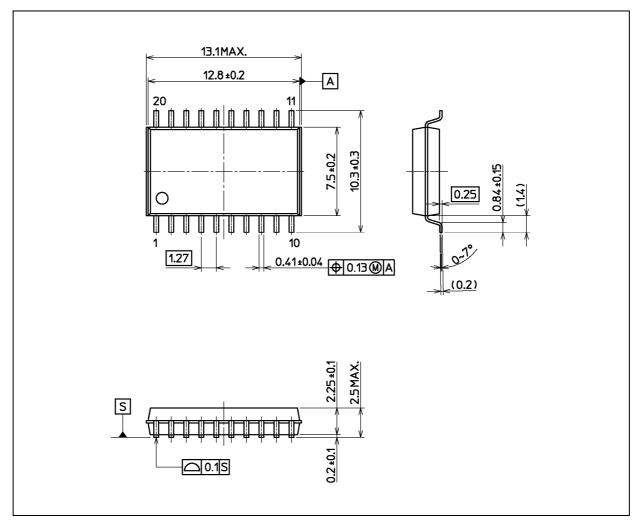
Characteristics	Symbol	Test Condition	C _L (pF)	V _{CC} (V)	Min	Max	Unit
Output transition time	t _{TLH} ,t _{THL}	—	50	2.0	_	90	ns
				4.5	_	18]
				6.0	_	15	
Propagation delay time	t _{PLH} ,t _{PHL}	_	50	2.0	_	250	ns
(CK-Q)				4.5	_	50	
				6.0	_	43]
			150	2.0	_	285]
				4.5	_	57	
				6.0	_	48	
Output enable time	t _{PZL} ,t _{PZH}	$R_L = 1 k\Omega$	50	2.0	_	205	ns
				4.5	_	41]
				6.0	_	35	
			150	2.0	_	280	
				4.5	_	56	
				6.0	_	48]
Output disable time	t _{PLZ} ,t _{PHZ}	R _L = 1 kΩ	50	2.0	_	205	ns
				4.5	_	41]
				6.0	_	35	1
Maximum clock frequency	f _{MAX}	_	50	2.0	4	_	MHz
				4.5	20	_	
				6.0	24		



Package Dimensions

74HC374D

Unit: mm



Weight: 0.51 g (typ.)

Package Name(s)

Nickname: SOIC20

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