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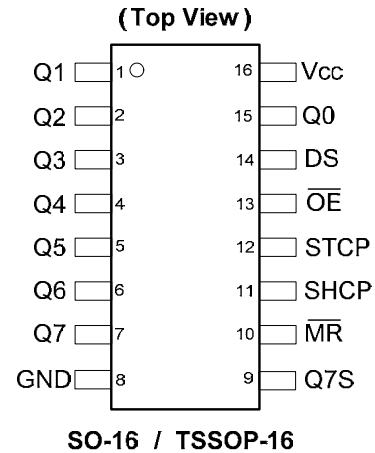Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

74HC595

8-BIT SHIFT REGISTER WITH 8-BIT OUTPUT REGISTER

Description

The 74HC595 is an high speed CMOS device.

An eight bit shift register accpets data from the serial input (DS) on each positive transition of the shift register clock (STCP). When asserted low the reset function ($\overline{MR}$) sets all shift register values to zero and is indepent of all clocks.

Data from the input serial shift register is placed in the output register with a rising pulse on the storages resister clock (SHCP). With the output enable ($\overline{OE}$) asserted low the 3-state outputs Q0-Q7 become active and present th

All registers capture data on rising edge and change output on the falling edge. If both clocks are connected together the input shift register is always one clock cycle ahead of the output register.

Pin Assignments

(Top View)

Q1	1	16	Vcc
Q2	2	15	Q0
Q3	3	14	DS
Q4	4	13	$\overline{OE}$
Q5	5	12	STCP
Q6	6	11	SHCP
Q7	7	10	$\overline{MR}$
GND	8	9	Q7S

SO-16 / TSSOP-16

Features

- Wide Supply Voltage Range from 2.0V to 6.0V
- Sinks or sources 8mA at V_{CC} = 4.5V
- CMOS low power consumption
- Schmitt Trigger Action at All Inputs
- Inputs accept up to 6.0V
- ESD Protection Tested per JESD 22
  - Exceeds 200-V Machine Model (A115-A)
  - Exceeds 2000-V Human Body Model (A114-A)
  - Exceeds 1000-V Charged Device Model (C101C)
- Latch-Up Exceeds 250mA per JESD 78, Class II
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

- General Purpose Logic
- Serial to Parallel Data conversion
- Capture and hold data for extended periods of time.
- Allow simple serial bit streams from a microcontroller to control as many peripheral lines as needed.
- Wide array of products such as:
  - Computer peripherals
  - Appliances
  - Industrial control

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

74HC595
Document number: DS35492 Rev. 3 - 2

1 of 11
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June 2013
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Pin Descriptions

Pin Number	Pin Name	Function
1	Q1	Parallel Data Output 1
2	Q2	Parallel Data Output 2
3	Q3	Parallel Data Output 3
4	Q4	Parallel Data Output 4
5	Q5	Parallel Data Output 5
6	Q6	Parallel Data Output 6
7	Q7	Parallel Data Output 7
8	GND	Ground
9	Q7S	Serial Data Output
10	$\overline{MR}$	Master Reset Input
11	SHCP	Shift Register Clock Input
12	STCP	Storage Register Clock Input
13	$\overline{OE}$	Output Enable Input
14	DS	Serial Data Input
15	Q0	Parallel Data Output 0
16	Vcc	Supply Voltage

Functional Diagram
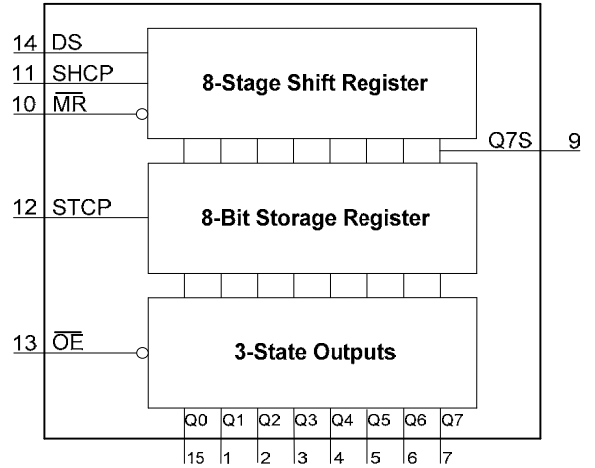
Logic Diagram
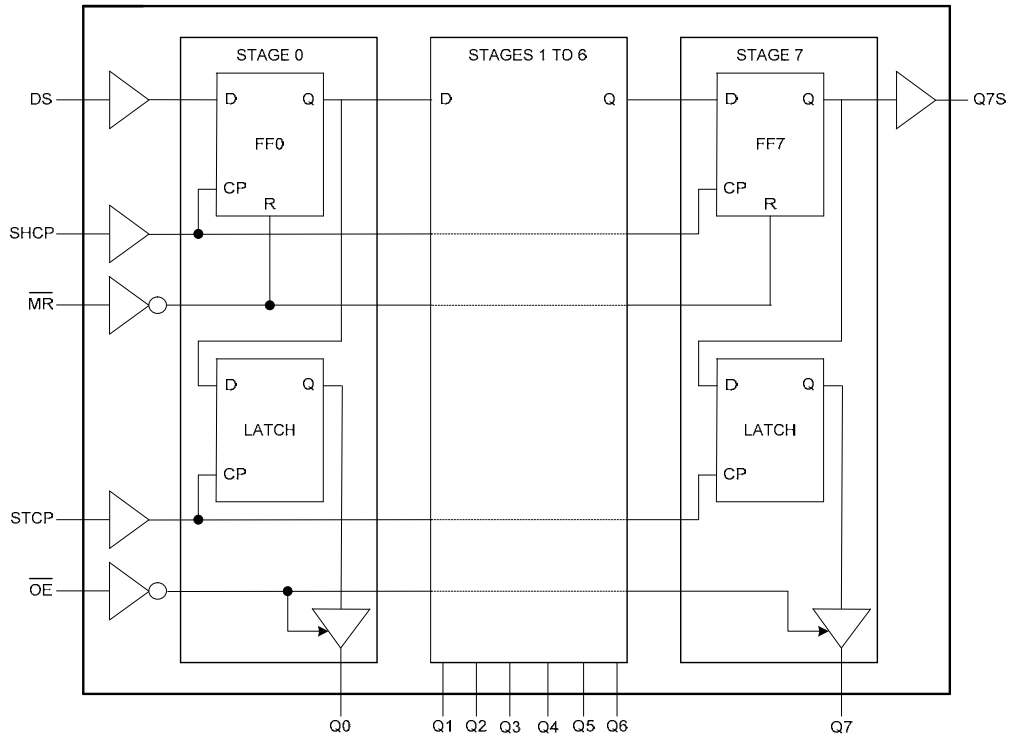
Functional Description and Timing Diagram

Control				Input	Output		Function
SHCP	STCP	$\overline{OE}$	$\overline{MR}$	DS	Q7S	Qn	
X	X	L	L	–	L	NC	Low-level asserted on MR clears shift register. Storage register is unchanged
X	↑	L	L	–	L	L	Empty shift register transferred to storage register
X	X	H	L	–	L	Z	Shift register remains clear;: All Q ouputs in Z state.
↑	X	L	H	–	Q6S	NC	HIGH is shifted into first stage of Shift Register Contents of each register shifted to next register The content of Q6S has been shifted to Q7S and now appears on device pin Q7S
X	↑	L	H	–	NC	QnS	Contents of shift register copied to storage register. With output now in active state the storage resister contents appear on Q outputs.
↑	↑	L	H	–	Q6S	QnS	Contents of shift register copied to output register then shift register shifted.

H=HIGH voltage state
L=LOW voltage state
↑=LOW to HIGH transition
X= don't care – high or low (not floating)
NC= No change
Z= high-impedance state

74HC595
Document number: DS35492 Rev. 3 - 2

June 2013
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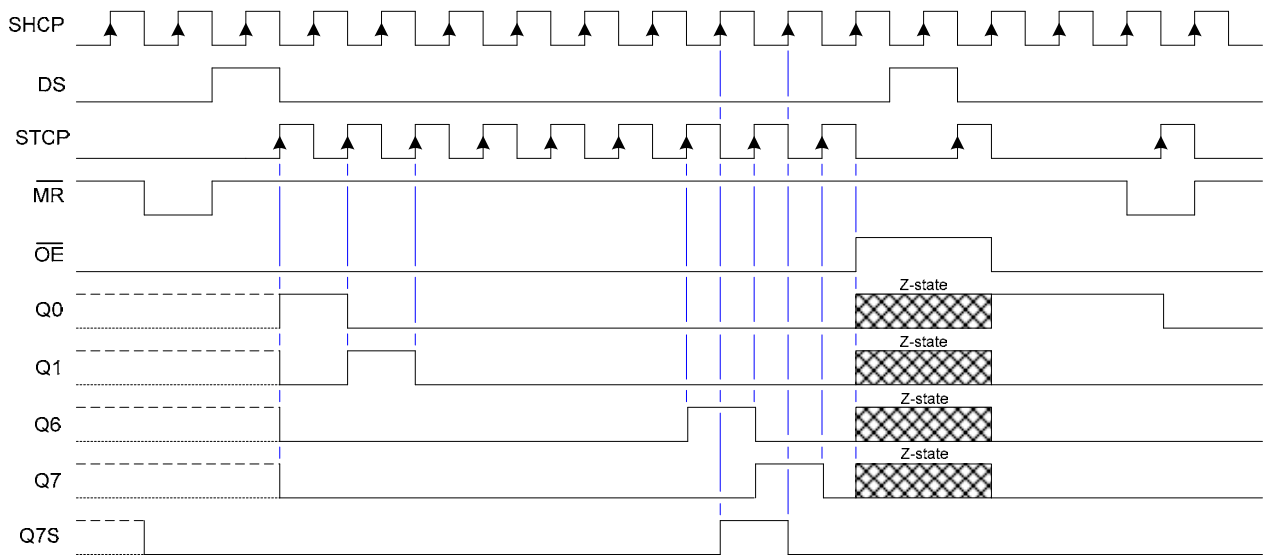
Absolute Maximum Ratings (Note 4) (@T$_A$ = +25°C, unless otherwise specified.)

Symbol	Description		Rating	Unit
ESD HBM	Human Body Model ESD Protection		2	kV
ESD CDM	Charged Device Model ESD Protection		1	kV
ESD MM	Machine Model ESD Protection		200	V
V$_{CC}$	Supply Voltage Range		-0.5 to +7.0	V
V$_I$	Input Voltage Range		-0.5 to +7.0	V
V$_o$	Voltage applied to output in high or low state		-0.3 to V$_{CC}$ +0.5	V
I$_{IK}$	Input Clamp Current V$_I$ < -0.5V		-20	mA
I$_{IK}$	Input Clamp Current VI > Vcc +0.5V		20	mA
I$_{OK}$	Output Clamp Current V$_O$ <-0.5V		-20	mA
I$_{OK}$	Output Clamp Current V$_O$ > V$_{CC}$ +0.5V		20	mA
I$_O$	Continuous output current	Q7 standard output	±25	mA
		Qn bus driver outputs	±35	mA
I$_{CC}$	Continuous current through Vdd or GND		70	mA
I$_{GND}$	Continuous current through Vdd or GND		-70	mA
T$_J$	Operating Junction Temperature		-40 to +150	°C
T$_{STG}$	Storage Temperature		-65 to +150	°C
P$_{TOT}$	Total Power Dissipation		500	mW

Note: 4. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.

Recommended Operating Conditions (Note 5) (@T$_A$ = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Max	Unit
V$_{CC}$	Supply Voltage	–	2.0	6.0	V
V$_I$	Input Voltage	–	0	V$_{CC}$	V
V$_O$	Output Voltage	Active Mode	0	V$_{CC}$	V
Δt/ΔV	Input transition rise or fall rate	V$_{CC}$ = 2.0V	–	1000	ns/V
		V$_{CC}$ = 4.5V	–	500	
		V$_{CC}$ = 6.0V	–	400	–
T$_A$	Operating free-air temperature	–	-40	+125	°C

Note: 5. Unused inputs should be held at V$_{CC}$ or Ground.

74HC595
Document number: DS35492 Rev. 3 - 2

4 of 11
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June 2013
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Electrical Characteristics (@T$_A$ = +25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	V$_{CC}$	T$_A$ = +25°C			T$_A$ = -40°C to +85°C		T$_A$ = -40°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V$_{IH}$	High-Level Input Voltage	–	2.0V	1.5	1.2	–	1.5	–	1.5	–	V
		–	4.5V	3.15	2.4	–	3.15	–	3.15	–	
		–	6.0V	4.2	3.2	–	4.2	–	4.2	–	
V$_{IL}$	Low-Level Input Voltage	–	2.0V	–	0.8	0.5	–	0.5	–	0.5	V
		–	4.5V	–	2.1	1.35	–	1.35	–	1.35	
		–	6.0V	–	2.8	1.8	–	1.8	–	1.8	
V$_{OH}$	High-Level Output Voltage	I$_{OH}$ = -20µA All outputs	2.0V	1.9	2.0	–	1.9	–	1.9	–	V
			4.5V	4.4	4.5	–	4.4	–	4.4	–	
			6.0V	5.9	6.0	–	5.9	–	5.9	–	
	Q7 output	I$_{OH}$ = -4.0mA	4.5V	3.84	4.32	–	4.32	–	3.7	–	
		I$_{OH}$ = -5.2mA	6.0V	5.34	5.81	–	5.81	–	5.2	–	
	Qn Bus Outputs	I$_{OH}$ = -6.0mA	4.5V	3.84	4.32	–	4.32	–	3.7	–	
		I$_{OH}$ = -7.8mA	6.0V	5.34	5.81	–	5.81	–	5.2	–	
V$_{OL}$	Low-Level Output Voltage	I$_{OL}$ = 20µA All outputs	2.0V	–	0	0.1	–	0.1	–	0.1	V
			4.5V	–	0	0.1	–	0.1	–	0.1	
			6.0V	–	0	0.1	–	0.1	–	0.1	
	Q7 output	I$_{OL}$ = 4.0mA	4.5V	–	.15	0.33	–	0.33	–	0.4	
		I$_{OL}$ = 5.2mA	6.0V	–	.16	0.33	–	0.33	–	0.4	
	Qn Bus Outputs	I$_{OL}$ = 6.0mA	4.5V	–	.15	0.33	–	0.33	–	0.4	
		I$_{OL}$ = 7.8mA	6.0V	–	.16	0.33	–	0.33	–	0.4	
I$_I$	Input Current	V$_I$ =GND to 5.5V	6.0V	–	–	±0.1	–	± 1	–	± 1	µA
I$_{OZ}$	OFF-state output current	Qn internal high or low Vo = Vcc or Gnd	6.0V	–	–	± 5	–	± 5	–	± 10	µA
I$_{CC}$	Supply Current	V$_I$ = GND or V$_{CC}$ I$_O$ = 0	6.0V	–	–	8.0	–	80	–	160	µA
C$_i$	Input Capacitance	V$_i$ = V$_{CC}$ or GND	6.0V	–	4	10	–	10	–	10	pF

Operating Characteristics (@T$_A$ = +25°C, unless otherwise specified.)

Parameter		Test Conditions	V$_{CC}$ = 5V Typ	Unit
C$_{pd}$	Power dissipation capacitance	f = 1 MHz all outputs switching-no load	43	pF

74HC595
Document number: DS35492 Rev. 3 - 2

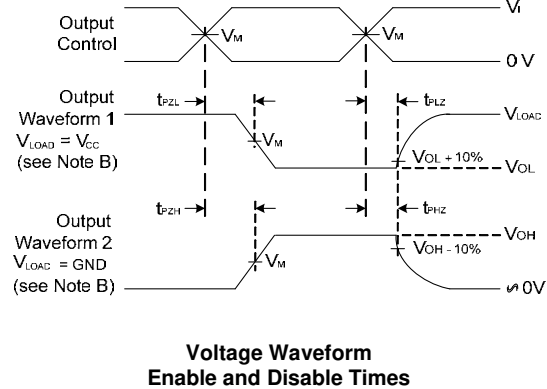5 of 11
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June 2013
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Switching Characteristics

Symbol / Parameter	Pins	Test Conditions	V_CC	T_A = +25°C			-40°C to +85°C		-40°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
f_{MAX} Maximum Frequency	SHCP or STCP	Figure 1	2.0V	9	30	–	4.8	–	4	–	MHz
			4.5V	30	91	–	24	–	20	–	
			6.0V	35	108	–	28	–	24	–	
t_W Pulse Width	SHCP HIGH or LOW	Figure 1	2.0V	75	17	–	95	–	110	–	ns
			4.5V	15	6	–	19	–	22	–	
			6.0V	13	5	–	16	–	19	–	
	STCP HIGH or LOW	Figure 1	2.0V	75	11	–	95	–	110	–	
			4.5V	15	4	–	19	–	22	–	
			6.0V	13	3	–	16	–	19	–	
	$\overline{MR}$ LOW	Figure 1	2.0V	75	17	–	95	–	110	–	
			4.5V	15	6	–	19	–	22	–	
			6.0V	13	5	–	16	–	19	–	
t_{SU} Set-up Time	DS to SHCP	Figure 1	2.0V	50	11	–	65	–	75	–	ns
			4.5V	10	4	–	13	–	15	–	
			6.0V	9	3	–	11	–	13	–	
	SHCP tp STCP	Figure 1	2.0V	75	22	–	95	–	110	–	ns
			4.5V	15	8	–	19	–	22	–	
			6.0V	13	7	–	16	–	19	–	
t_H Hold Time	DS to SHCP	Figure 1	2.0V	3	-6	–	3	–	3	–	ns
			4.5V	3	-2	–	3	–	3	–	
			6.0V	3	-2	–	3	–	3	–	
t_{REC} Recovery Time	$\overline{MR}$ to SHCP	Figure 1	2.0V	50	-19	–	65	–	75	–	ns
			4.5V	10	-7	–	13	–	15	–	
			6.0V	9	-6	–	11	–	13	–	
t_{PD} Propagation Delay	SHCP to Q7S	Figure 1 C_L=50pF	2.0V	–	52	160	–	200	–	240	ns
			4.5V	–	19	32	–	40	–	48	
			6.0V	–	15	27	–	34	–	41	
	STCP to Qn	Figure 1 C_L=50pF	2.0V	–	55	175	–	220	–	265	ns
			4.5V	–	20	35	–	44	–	53	
			6.0V	–	16	30	–	37	–	45	
t_{PHL} Propagation Delay	$\overline{MR}$ to Q7S	Figure 1 C_L=50pF	2.0V	–	47	175	–	220	–	265	ns
			4.5V	–	17	35	–	44	–	53	
			6.0V	–	14	30	–	37	–	45	
t_{EN} Enable Time	$\overline{OE}$ to Qn	Figure 1 C_L=50pF	2.0V	–	47	150	–	190	–	225	ns
			4.5V	–	17	30	–	38	–	45	
			6.0V	–	14	26	–	33	–	38	
t_{DIS} Disable Time	$\overline{OE}$ to Qn	Figure 1 C_L=50pF	2.0V	–	41	150	–	190	–	225	ns
			4.5V	–	15	30	–	38	–	45	
			6.0V	–	12	26	–	33	–	38	

74HC595

Document number: DS35492 Rev. 3 - 2

6 of 11

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June 2013

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Parameter Measurement Information
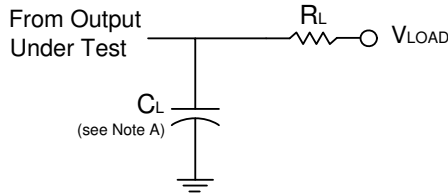
TEST	Vload
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	Vcc
t_{PHZ}/t_{PZH}	GND

V_{CC}	Inputs		V_M	C_L
	V_I	t_r/t_f		
2.0V	V_{CC}	6ns	$V_{CC}/2$	50pF
4.5V	V_{CC}	6ns	$V_{CC}/2$	50pF
6.0V	V_{CC}	6ns	$V_{CC}/2$	50pF

Voltage Waveform
Pulse Duration and Recovery Time

Voltage Waveform
Set-up and Hold Times

Voltage Waveform
Propagation Delay Times
Inverting and Non Inverting Outputs

Voltage Waveform
Enable and Disable Times
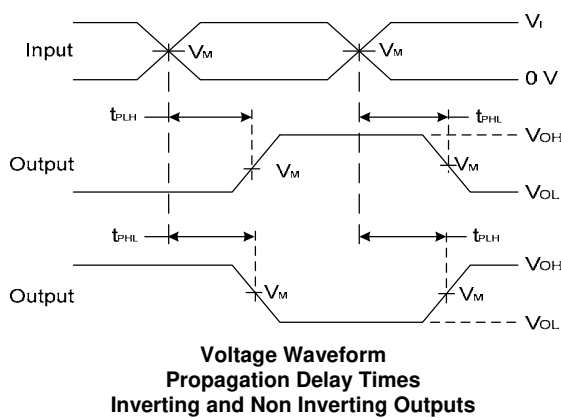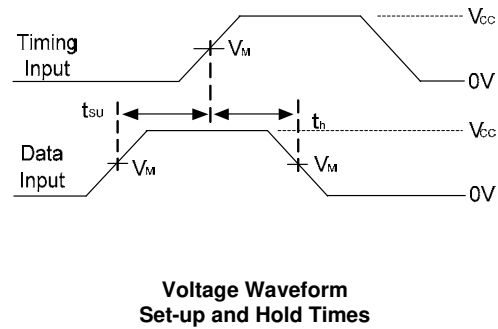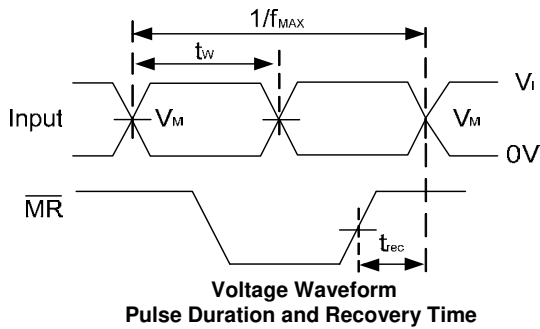
Notes: A. Includes test lead and test apparatus capacitance.
B. Output Waveform 1 depends on the internal Q_N node being low and behaves in this manner based on OE pin.
 Output Waveform 2 depends on the internal Q_N node being high and behaves in this manner based on OE pin.
C. All pulses are supplied at pulse repetition rate ≤ 10MHz
D. Inputs are measured separately one transition per measurement
E. t_{PLH} and t_{PHL} are the same as t_{PD}

Figure 1. Load Circuit and Voltage Waveforms

74HC595
Document number: DS35492 Rev. 3 - 2

7 of 11
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June 2013
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Ordering Information

74 HC 595 XXX - 13

Logic Device	Function	Package	Packing
74 : Logic Prefix HC : 2.0V to 6.0V Family	595 : 8-BIT SHIFT REGISTER WITH 8-BIT OUTPUT REGISTER	S16 : SO-16 T16 : TSSOP-16	-13 : 13" Tape & Reel
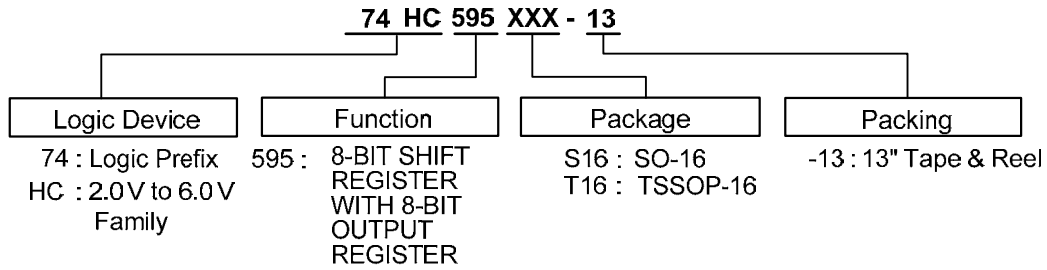
Part Number	Package Code	Packaging	7" Tape and Reel (Note 6)	
			Quantity	Part Number Suffix
74HC595S16-13	S16	SO-16	2500/Tape & Reel	-13
74HC595T16-13	T16	TSSOP-16	2500/Tape & Reel	-13

Note: 6. The taping orientation is located on our website at http://www.diodes.com/datasheets/ap02007.pdf

Marking Information

(1) SO-16, TSSOP16

(Top View)

Logo ◄

Part Number ◄

74HC595
YY WW X X

YY : Year : 08, 09,10~

WW : Week : 01~52; 52 represents 52 and 53 week

XX : Internal Codes
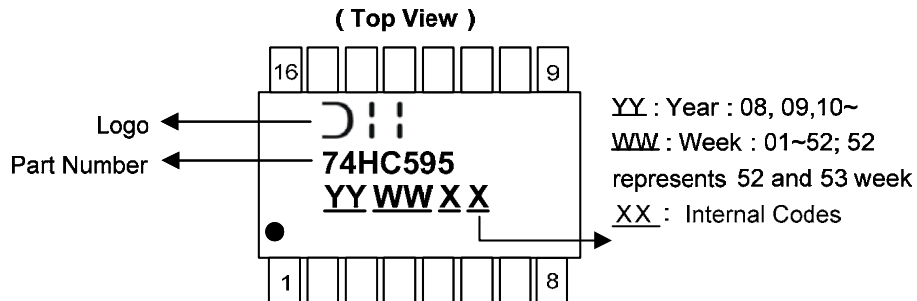
Part Number	Package
74HC595S16	SO-16
74HC595T16	TSSOP-16

Package Outline Dimensions (All dimensions in mm.)

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.

Package Type: SO-16
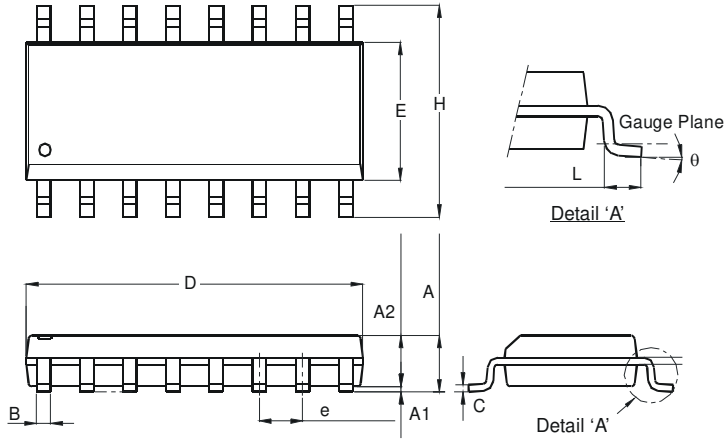
SO-16		
Dim	Min	Max
A	1.40	1.75
A1	0.10	0.25
A2	1.30	1.50
B	0.33	0.51
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
e	1.27 Typ	
H	5.80	6.20
L	0.38	1.27
θ	0°	8°
All Dimensions in mm		

Package Type: TSSOP-16
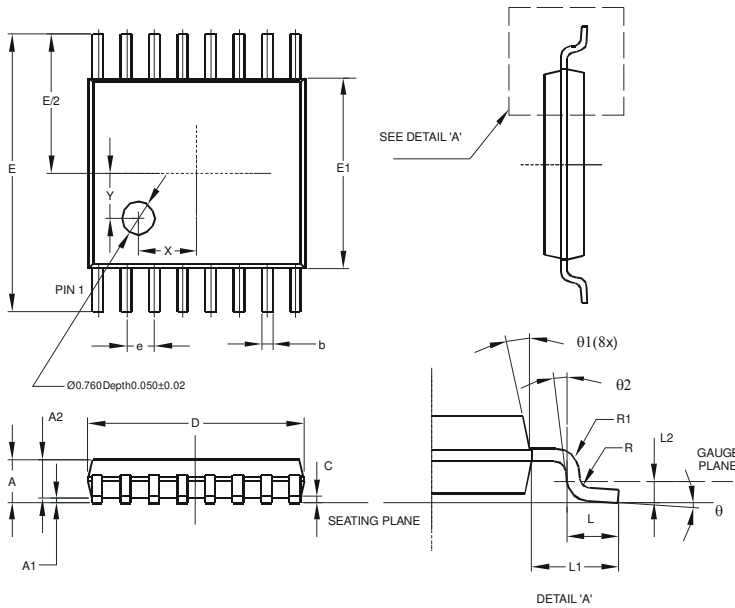
TSSOP-16			
Dim	Min	Max	Typ
A	-	1.08	-
A1	0.05	0.15	-
A2	0.80	0.93	-
b	0.19	0.30	-
c	0.09	0.20	-
D	4.90	5.10	-
E	6.40 BSC		
E1	4.30	4.50	-
e	0.65 BSC		
L	0.45	0.75	-
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
R1	0.09	-	-
X	-	-	1.350
Y	-	-	1.050
θ	0°	8°	-
θ1	5°	15°	-
θ2	0°	-	-
All Dimensions in mm			

74HC595
Document number: DS35492 Rev. 3 - 2

9 of 11
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Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

Package Type: SO-16
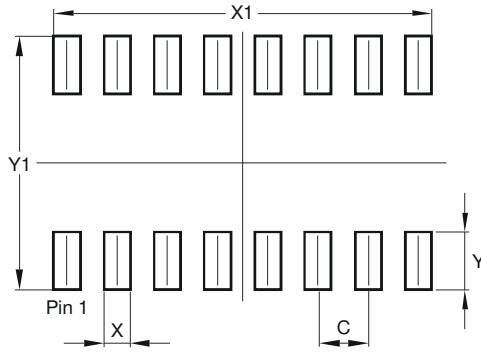
Dimensions	Value (in mm)
C	1.270
X	0.670
X1	9.560
Y	1.450
Y1	6.400

Package Type: TSSOP-16
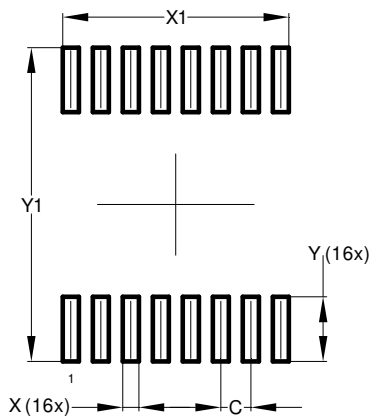
Dimensions	Value (in mm)
C	0.650
X	0.350
X1	4.900
Y	1.400
Y1	6.800

74HC595

Document number: DS35492 Rev. 3 - 2

10 of 11

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74HC595
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11 of 11
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