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DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC7266
Quad 2-input EXCLUSIVE-NOR gate

Product specification
File under Integrated Circuits, IC06

December 1990

Philips
Semiconductors

PHILIPS

Quad 2-input EXCLUSIVE-NOR gate 74HC7266

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC7266 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC7266 provide the EXCLUSIVE-NOR function with active push-pull output.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	11	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	note 1	17	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

Quad 2-input EXCLUSIVE-NOR gate 74HC7266

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 5, 8, 12	1A to 4A	data inputs
2, 6, 9, 13	1B to 4B	data inputs
3, 4, 10, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

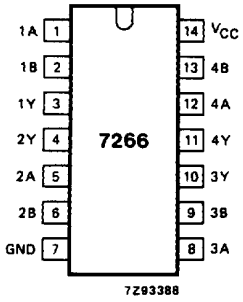


Fig.1 Pin configuration.

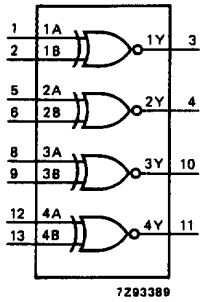


Fig.2 Logic symbol.

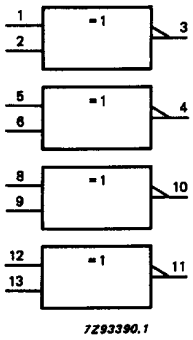


Fig.3 IEC logic symbol.

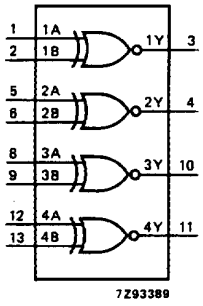


Fig.4 Functional diagram.

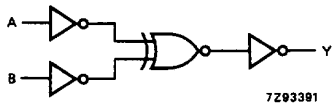


Fig.5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	H

Notes

1. H = HIGH voltage level
   L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

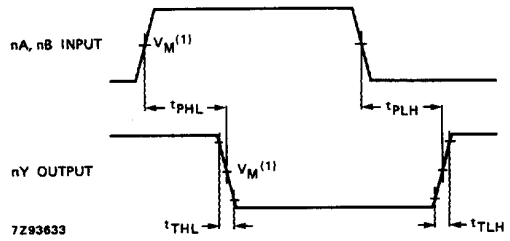
Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		39 14 11	115 23 20		145 29 25		175 35 30	ns	2.0 4.5 6.0	Fig.6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.

Fig.6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.