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DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT9114

Nine wide Schmitt trigger buffer; open drain outputs; inverting

Product specification
Supersedes data of March 1988
File under Integrated Circuits, IC06

December 1990

Philips Semiconductors

PHILIPS

Nine wide Schmitt trigger buffer; open drain outputs; inverting

74HC/HCT9114

FEATURES

- Schmitt trigger action on all data inputs
- Output capability: standard (open drain)
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT9114 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT9114 are nine wide Schmitt trigger inverting buffer with open drain outputs and Schmitt trigger inputs.

The Schmitt trigger action in the data inputs transform slowly changing input signals into sharply defined jitter-free output signals.

The 74HC/HCT9114 have open-drain N-transistor outputs, which are not clamped by a diode connected to V_{CC}. In the OFF-state, i.e. when one input is LOW, the output may be pulled to any voltage between GND and V_{Omax}. This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

The “9114” is identical to the “9115” but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLZ}	propagation delay A_n to $\overline{Y}_n$	C_L = 15 pF; V_{CC} = 5 V	12	13	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	5	5	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_8	data inputs
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12, 11	$\overline{Y}_0$ to $\overline{Y}_8$	data outputs
20	V_{CC}	positive supply voltage

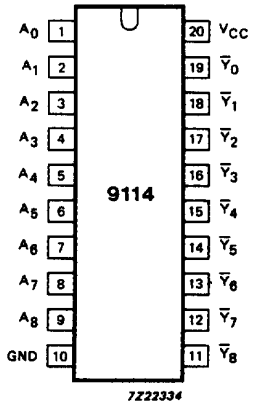


Fig.1 Pin configuration.

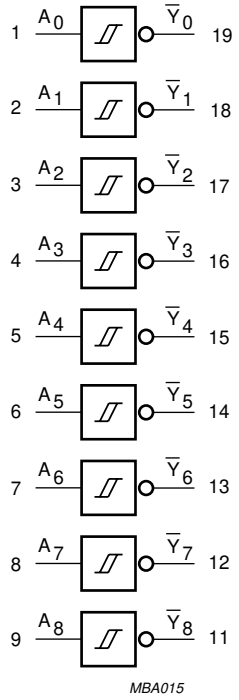


Fig.2 Logic diagram.

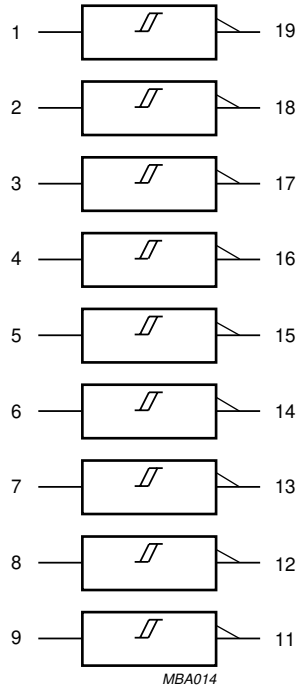


Fig.3 IEC logic diagram.

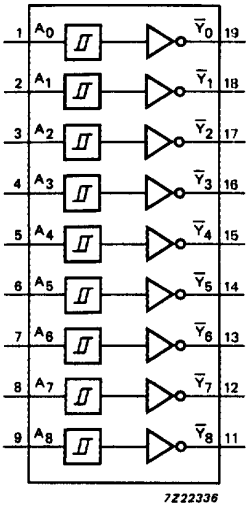


Fig.4 Functional diagram.

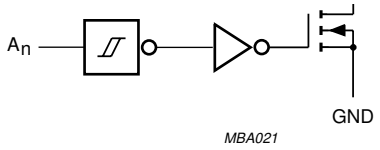


Fig.5 Logic diagram (one Schmitt trigger).

FUNCTION TABLE

INPUTS	OUTPUTS
A_n	$\overline{Y}_n$
L	Z
H	L

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.
Transfer characteristics are given below.

Output capability: standard
I_{CC} category: MSI

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are referred to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	0.70 1.75 2.30	1.13 2.37 3.11	1.50 3.15 4.20	0.70 1.75 2.30	1.50 3.15 4.20	0.70 1.75 2.30	1.50 3.15 4.20	V	2.0 4.5 6.0	Fig.6
V_{T-}	negative-going threshold	0.30 1.35 1.80	0.70 1.80 2.43	1.10 2.40 3.30	0.30 1.35 1.80	1.10 2.40 3.30	0.30 1.35 1.80	1.10 2.40 3.30	V	2.0 4.5 6.0	Fig.6
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.4 0.5	0.43 0.57 0.68	0.80 1.00 1.10	0.18 0.40 0.50	0.80 1.00 1.10	0.15 0.40 0.50	0.80 1.00 1.10	V	2.0 4.5 6.0	Fig.6

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLZ}	propagation delay A_n to $\overline{Y}n$		36 13 10	110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig.7
t_{THL}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.
Transfer characteristics are given below.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	0.3

TRANSFER CHARACTERISTICS FOR 74HCT

Voltages are referred to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	0.9 1.2	1.50 1.70	2.0 2.1	0.9 1.2	2.0 2.1	0.9 1.2	2.0 2.1	V	4.5 5.5	Fig.6
V_{T-}	negative-going threshold	0.7 0.8	1.06 1.27	1.4 1.7	0.7 0.8	1.4 1.7	0.7 0.8	1.4 2.7	V	4.5 5.5	Fig.6
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.2	0.44 0.44	0.8 0.8	0.2 0.2	0.8 0.8	0.2 0.2	0.8 0.8	V	4.5 5.5	Fig.6

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLZ}	propagation delay A_n to $\overline{Y}_n$		17	31		39		47	ns	4.5	Fig.7
t_{THL}	output transition time		7	15		19		22	ns	4.5	Fig.7

TRANSFER CHARACTERISTIC WAVEFORMS

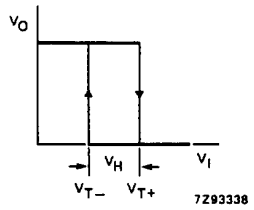
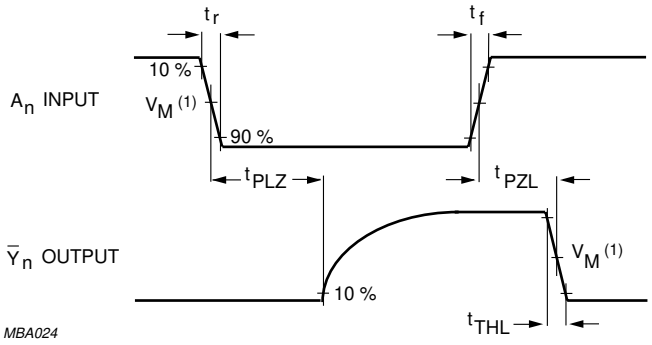


Fig.6 Transfer characteristic.

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the input (A_n) to output ($\overline{Y}_n$) propagation delays and the output transition times.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.