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74HC193; 74HCT193

Presettable synchronous 4-bit binary up/down counter

Rev. 4 — 24 June 2013 **Product data sheet**

1. General description

The 74HC193; 74HCT193 is a 4-bit synchronous binary up/down counter. Separate up/down clocks, CPU and CPD respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CPU clock is pulsed while CPD is held HIGH, the device will count up. If the CPD clock is pulsed while CPU is held HIGH, the device will count down. Only one clock input can be held HIGH at any time to guarantee predictable behaviour. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input ($\overline{PL}$). The terminal count up ($\overline{TCU}$) and terminal count down ($\overline{TCD}$) outputs are normally HIGH. When the circuit has reached the maximum count state of 15, the next HIGH-to-LOW transition of CPU will cause $\overline{TCU}$ to go LOW. $\overline{TCU}$ will stay LOW until CPU goes HIGH again, duplicating the count up clock. Likewise, the $\overline{TCD}$ output will go LOW when the circuit is in the zero state and the CPD goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added. The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D0 to D3) is loaded into the counter and appears on the outputs (Q0 to Q3) regardless of the conditions of the clock inputs when the parallel load ($\overline{PL}$) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q0 to Q3) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Input levels:
  - For 74HC193: CMOS level
  - For 74HCT193: TTL level
- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V.

- Multiple package options
- Specified from −40 °C to +85 °C and −40 °C to +125 °C.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC193D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC193DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC193N	−40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HC193PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT193D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT193DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT193N	−40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT193PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

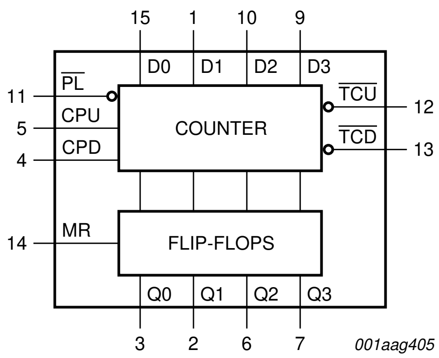


Fig 1. Functional diagram

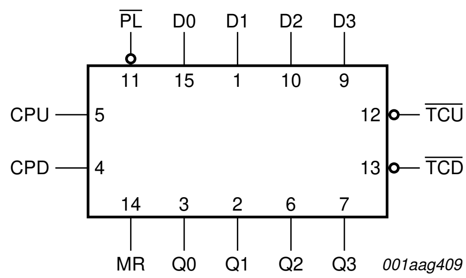


Fig 2. Logic symbol

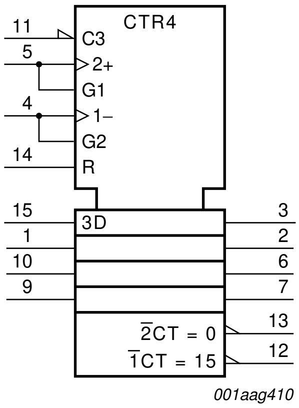


Fig 3. IEC logic symbol

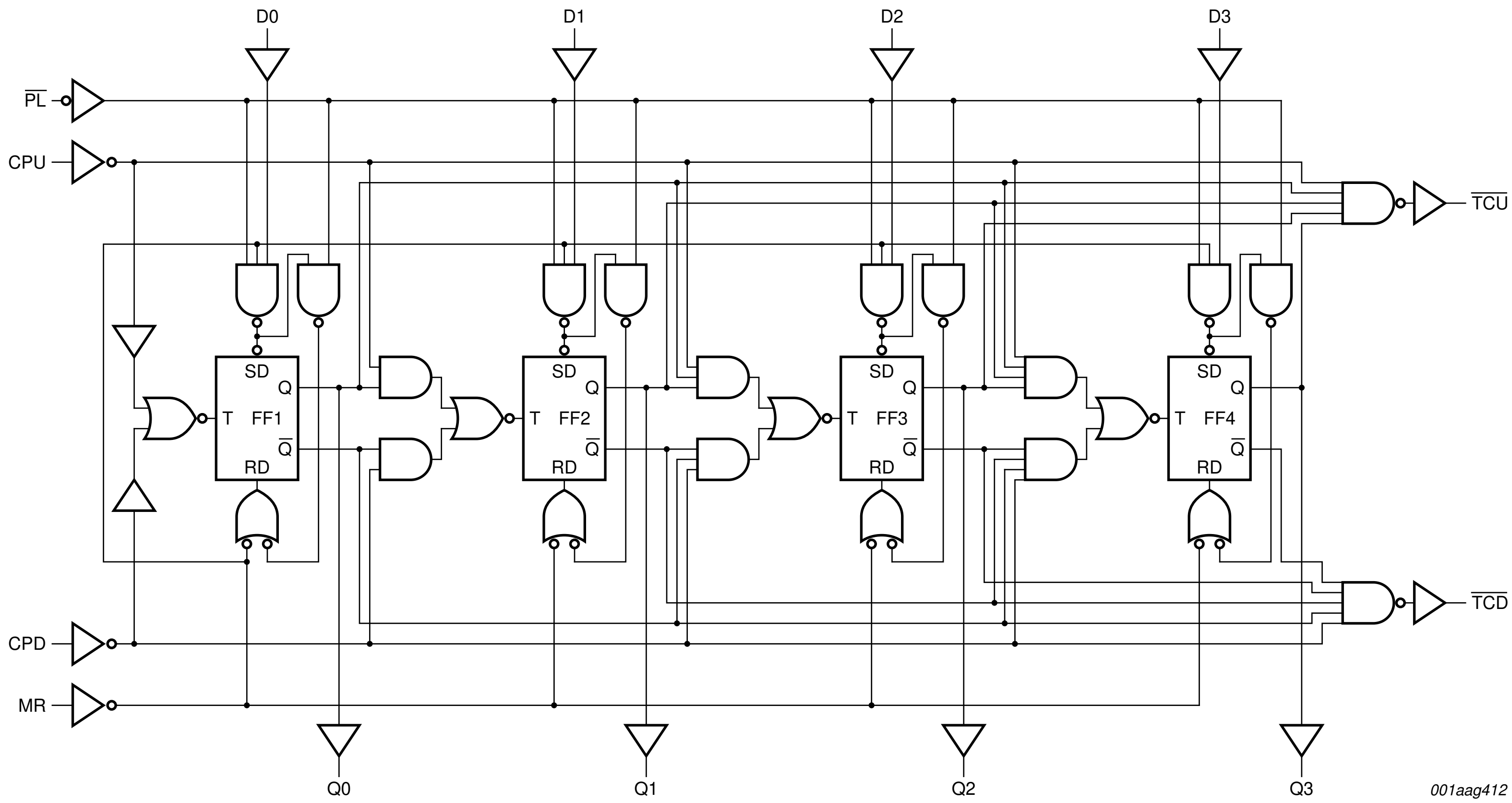


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

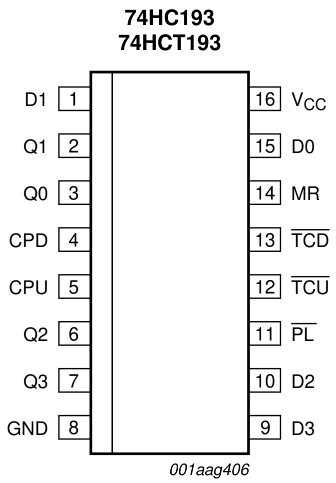


Fig 5. Pin configuration SO16

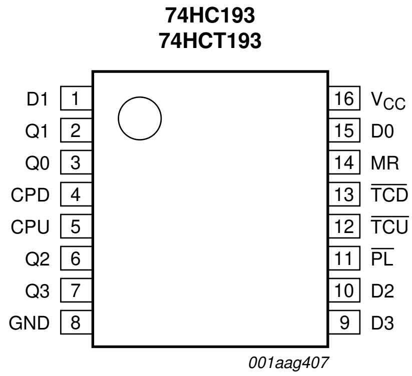


Fig 6. Pin configuration TSSOP16 and SSOP16

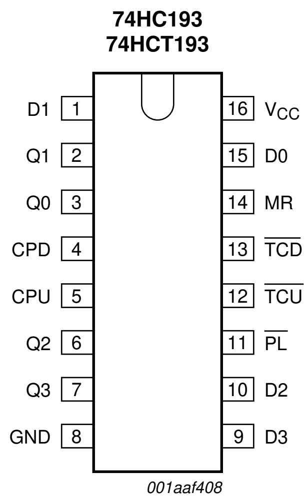


Fig 7. Pin configuration DIP16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
D0	15	data input 0
D1	1	data input 1
D2	10	data input 2
D3	9	data input 3
Q0	3	flip-flop output 0
Q1	2	flip-flop output 1
Q2	6	flip-flop output 2
Q3	7	flip-flop output 3
CPD	4	count down clock input[1]
CPU	5	count up clock input[1]
GND	8	ground (0 V)
$\overline{PL}$	11	asynchronous parallel load input (active LOW)
$\overline{TCU}$	12	terminal count up (carry) output (active LOW)
$\overline{TCD}$	13	terminal count down (borrow) output (active LOW)
MR	14	asynchronous master reset input (active HIGH)
V_{CC}	16	supply voltage

[1] LOW-to-HIGH, edge triggered.

6. Functional description

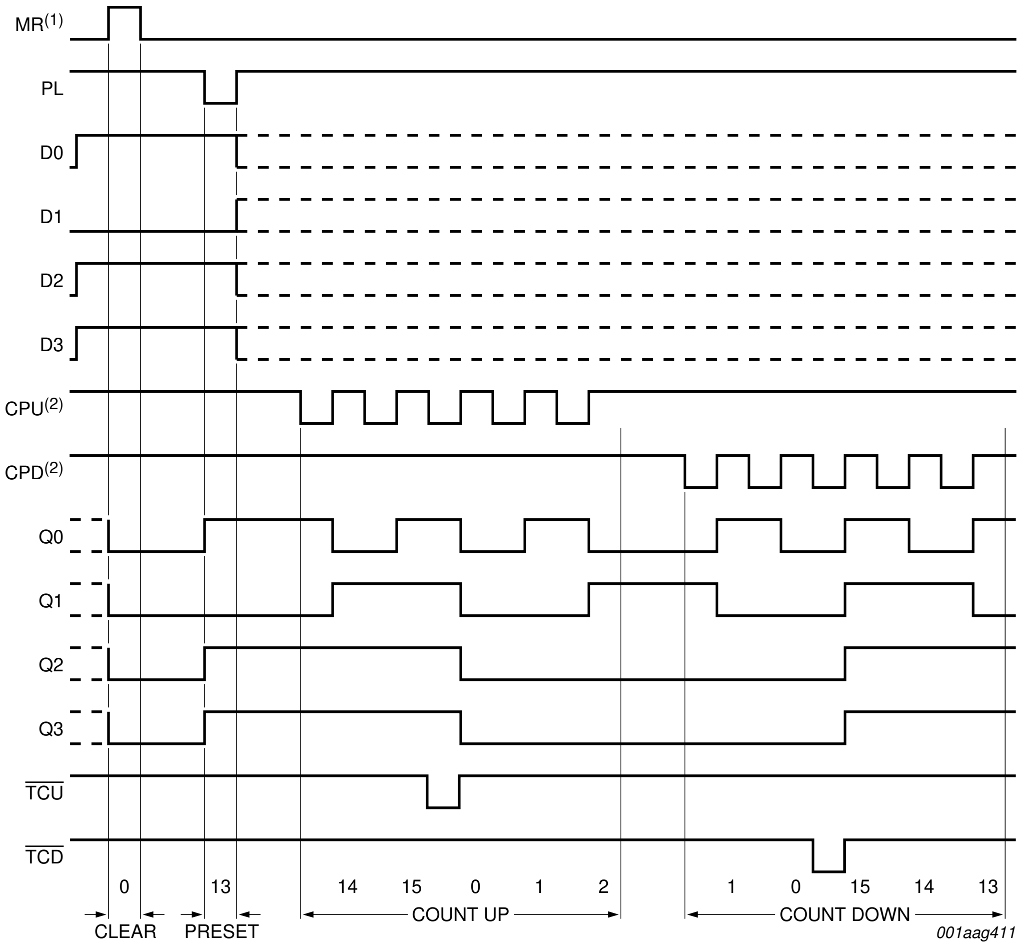
Table 3. Function table[1]

Operating mode	Inputs								Outputs					
	MR	$\overline{PL}$	CPU	CPD	D0	D1	D2	D3	Q0	Q1	Q2	Q3	$\overline{TCU}$	$\overline{TCD}$
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
Count up	L	H	↑	H	X	X	X	X	count up				H[2]	H
Count down	L	H	H	↑	X	X	X	X	count down				H	H[3]

[1] H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition.

[2] $\overline{TCU}$ = CPU at terminal count up (HHHH)

[3] $\overline{TCD}$ = CPD at terminal count down (LLLL).



(1) Clear overrides load, data and count inputs.

(2) When counting up, the count down clock input (CPD) must be HIGH, when counting down the count up clock input (CPU) must be HIGH.

Sequence

Clear (reset outputs to zero);

load (preset) to binary thirteen;

count up to fourteen, fifteen, terminal count up, zero, one and two;

count down to one, zero, terminal count down, fifteen, fourteen and thirteen.

Fig 8. Typical clear, load and count sequence

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$V_O = –0.5$ V to $V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			-	–50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	DIP16 package	[2]	-	750	mW
		SO16 package	[2]	-	500	mW
		SSOP16 package	[2]	-	500	mW
		TSSOP16 package	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP16 packages: above 70 °C the value of P_{tot} derates linearly at 12 mW/K.
For SO16 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
For SSOP16 and TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC193						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0$ V	-	-	625	ns/V
		$V_{CC} = 4.5$ V	-	1.67	139	ns/V
		$V_{CC} = 6.0$ V	-	-	83	ns/V
74HCT193						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 4.5$ V	-	1.67	139	ns/V

9. Static characteristics

Table 6. Static characteristics type 74HC193

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	-	-	-	
		I_O = −20 μA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = −4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	μA
C_i	input capacitance		-	3.5	-	pF
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −20 μA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = −4.0 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V

Table 6. Static characteristics type 74HC193 *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20\ \mu A$; $V_{CC} = 2.0$ V	-	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 6.0$ V	-	-	0.1	V
		$I_O = 4.0$ mA; $V_{CC} = 4.5$ V	-	-	0.33	V
		$I_O = 5.2$ mA; $V_{CC} = 6.0$ V	-	-	0.33	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	80	μA
$T_{amb} = -40$ °C to +125 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	-	-	V
		$V_{CC} = 4.5$ V	3.15	-	-	V
		$V_{CC} = 6.0$ V	4.2	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0$ V	-	-	0.5	V
		$V_{CC} = 4.5$ V	-	-	1.35	V
		$V_{CC} = 6.0$ V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20\ \mu A$; $V_{CC} = 2.0$ V	1.9	-	-	V
		$I_O = -20\ \mu A$; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -20\ \mu A$; $V_{CC} = 6.0$ V	5.9	-	-	V
		$I_O = -4.0$ mA; $V_{CC} = 4.5$ V	3.7	-	-	V
		$I_O = -5.2$ mA; $V_{CC} = 6.0$ V	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20\ \mu A$; $V_{CC} = 2.0$ V	-	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 6.0$ V	-	-	0.1	V
		$I_O = 4.0$ mA; $V_{CC} = 4.5$ V	-	-	0.4	V
		$I_O = 5.2$ mA; $V_{CC} = 6.0$ V	-	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	160	μA

Table 7. Static characteristics type 74HCT193

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V				
		$I_O = -20\ \mu A$	4.4	4.5	-	V
		$I_O = -4.0$ mA	3.98	4.32	-	V

Table 7. Static characteristics type 74HCT193 *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V				
		$I_O = 20$ μA	-	0	0.1	V
		$I_O = 4.0$ mA	-	0.15	0.26	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.1	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1$ V and other inputs at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 4.5$ V to 5.5 V				
		pin Dn	-	35	126	μA
		pins CPU, CPD	-	140	504	μA
		pin $\overline{PL}$	-	65	234	μA
		pin MR	-	105	378	μA
C_i	input capacitance		-	3.5	-	pF
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V				
		$I_O = -20$ μA	4.4	-	-	V
		$I_O = -4.0$ mA	3.84	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V				
		$I_O = 20$ μA	-	-	0.1	V
		$I_O = 4.0$ mA	-	-	0.33	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	80	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1$ V and other inputs at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 4.5$ V to 5.5 V				
		pin Dn	-	-	157.5	μA
		pins CPU, CPD	-	-	630	μA
		pin $\overline{PL}$	-	-	292.5	μA
		pin MR	-	-	472.5	μA
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V				
		$I_O = -20$ μA	4.4	-	-	V
		$I_O = -4.0$ mA	3.7	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V				
		$I_O = 20$ μA	-	-	0.1	V
		$I_O = 4.0$ mA	-	-	0.4	V

Table 7. Static characteristics type 74HCT193 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	160	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1$ V and other inputs at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 4.5$ V to 5.5 V				
		pin Dn	-	-	171.5	μA
		pins CPU, CPD	-	-	686	μA
		pin $\overline{PL}$	-	-	318.5	μA
		pin MR	-	-	514.5	μA

10. Dynamic characteristics

Table 8. Dynamic characteristics type 74HC193

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	CPU, CPD to Qn; see Figure 9 [1]	-							
		V_{CC} = 2.0 V	-	63	215	-	270	-	325	ns
		V_{CC} = 4.5 V	-	23	43	-	54	-	65	ns
		V_{CC} = 6.0 V	-	18	37	-	46	-	55	ns
		CPU to $\overline{TCU}$; see Figure 10								
		V_{CC} = 2.0 V	-	39	125	-	155	-	190	ns
		V_{CC} = 4.5 V	-	14	25	-	31	-	38	ns
		V_{CC} = 6.0 V	-	11	21	-	26	-	32	ns
		CPD to $\overline{TCD}$; see Figure 10								
		V_{CC} = 2.0 V	-	39	125	-	155	-	190	ns
		V_{CC} = 4.5 V	-	14	25	-	31	-	38	ns
		V_{CC} = 6.0 V	-	11	21	-	26	-	32	ns
		$\overline{PL}$ to Qn; see Figure 11								
		V_{CC} = 2.0 V	-	69	220	-	275	-	330	ns
		V_{CC} = 4.5 V	-	25	44	-	55	-	66	ns
		V_{CC} = 6.0 V	-	20	37	-	47	-	56	ns
		MR to Qn; see Figure 12								
		V_{CC} = 2.0 V	-	58	200	-	250	-	300	ns
		V_{CC} = 4.5 V	-	21	40	-	50	-	60	ns
		V_{CC} = 6.0 V	-	17	34		43	-	51	ns
		Dn to Qn; see Figure 11								
		V_{CC} = 2.0 V	-	69	210	-	265	-	315	ns
		V_{CC} = 4.5 V	-	25	42	-	53	-	63	ns
		V_{CC} = 6.0 V	-	20	36	-	45	-	54	ns
		$\overline{PL}$ to $\overline{TCU}$, $\overline{PL}$ to $\overline{TCD}$; see Figure 14								
		V_{CC} = 2.0 V	-	80	290	-	365	-	435	ns
		V_{CC} = 4.5 V	-	29	58	-	73	-	87	ns
		V_{CC} = 6.0 V	-	23	49	-	62	-	74	ns
		MR to $\overline{TCU}$, MR to $\overline{TCD}$; see Figure 14								
		V_{CC} = 2.0 V	-	74	285	-	355	-	430	ns
		V_{CC} = 4.5 V	-	27	57	-	71	-	86	ns
		V_{CC} = 6.0 V	-	22	48	-	60	-	73	ns

Table 8. Dynamic characteristics type 74HC193 *...continued*

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	Dn to $\overline{\mathrm{TCU}}$, Dn to $\overline{\mathrm{TCD}}$; see Figure 14								
		V_{CC} = 2.0 V	-	80	290	-	365	-	435	ns
		V_{CC} = 4.5 V	-	29	58	-	73	-	87	ns
		V_{CC} = 6.0 V	-	23	49	-	62	-	74	ns
t_{THL}	HIGH to LOW output transition time	see Figure 12								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_{TLH}	LOW to HIGH output transition time	see Figure 12								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	CPU, CPD (HIGH or LOW); see Figure 9								
		V_{CC} = 2.0 V	100	22	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	8	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	6	-	21	-	26	-	ns
		MR (HIGH); see Figure 12								
		V_{CC} = 2.0 V	100	25	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	9	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	7	-	21	-	26	-	ns
		$\overline{\mathrm{PL}}$ (LOW); see Figure 11								
		V_{CC} = 2.0 V	100	19	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	7	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	6	-	21	-	26	-	ns
t_{rec}	recovery time	$\overline{\mathrm{PL}}$ to CPU, CPD; see Figure 11								
		V_{CC} = 2.0 V	50	8	-	65	-	75	-	ns
		V_{CC} = 4.5 V	10	3	-	13	-	15	-	ns
		V_{CC} = 6.0 V	9	2	-	11	-	13	-	ns
		MR to CPU, CPD; see Figure 12								
		V_{CC} = 2.0 V	50	0	-	65	-	75	-	ns
		V_{CC} = 4.5 V	10	0	-	13	-	15	-	ns
		V_{CC} = 6.0 V	9	0	-	11	-	13	-	ns

Table 8. Dynamic characteristics type 74HC193 *…continued*

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{su}	set-up time	Dn to $\overline{PL}$; see Figure 13; note: CPU = CPD = HIGH								
		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t_h	hold time	Dn to $\overline{PL}$; see Figure 13								
		V_{CC} = 2.0 V	0	–14	-	0	-	0	-	ns
		V_{CC} = 4.5 V	0	–5	-	0	-	0	-	ns
		V_{CC} = 6.0 V	0	–4	-	0		0	-	ns
		CPU to CPD, CPD to CPU; see Figure 15								
		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	8	6	-	17	-	20	-	ns
f_{max}	maximum frequency	CPU, CPD; see Figure 9								
		V_{CC} = 2.0 V	4.0	13.5	-	3.2	-	2.6	-	MHz
		V_{CC} = 4.5 V	20	41	-	16	-	13	-	MHz
		V_{CC} = 6.0 V	24	49	-	19	-	15	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 5 V; f_i = 1 MHz [2]	-	24	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Table 9. Dynamic characteristics type 74HCT193

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	CPU, CPD to Qn; see Figure 9 [1]								
		V_{CC} = 4.5 V	-	23	43	-	54	-	65	ns
		CPU to $\overline{TCU}$; see Figure 10								
		V_{CC} = 4.5 V	-	15	27	-	34	-	41	ns
		CPD to $\overline{TCD}$; see Figure 10								
		V_{CC} = 4.5 V	-	15	27	-	34	-	41	ns
		$\overline{PL}$ to Qn; see Figure 11								
		V_{CC} = 4.5 V	-	26	46	-	58	-	69	ns
		MR to Qn; see Figure 12								
		V_{CC} = 4.5 V	-	22	40	-	50	-	60	ns
		Dn to Qn; see Figure 11								
		V_{CC} = 4.5 V	-	27	46	-	58	-	69	ns
		$\overline{PL}$ to $\overline{TCU}$, $\overline{PL}$ to $\overline{TCD}$; see Figure 14								
		V_{CC} = 4.5 V	-	31	55	-	69	-	83	ns
		MR to $\overline{TCU}$, MR to $\overline{TCD}$; see Figure 14								
		V_{CC} = 4.5 V	-	29	55	-	69	-	83	ns
		Dn to $\overline{TCU}$, Dn to $\overline{TCD}$; see Figure 14								
		V_{CC} = 4.5 V	-	32	58	-	73	-	87	ns
t_{THL}	HIGH to LOW output transition time	see Figure 12								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t_{TLH}	LOW to HIGH output transition time	see Figure 12								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t_W	pulse width	CPU, CPD (HIGH or LOW); see Figure 9								
		V_{CC} = 4.5 V	25	11	-	31	-	38	-	ns
		MR (HIGH); see Figure 12								
		V_{CC} = 4.5 V	20	7	-	25	-	30	-	ns
		$\overline{PL}$ (LOW); see Figure 11								
		V_{CC} = 4.5 V	20	8	-	25	-	30	-	ns

Table 9. Dynamic characteristics type 74HCT193 *…continued*

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{rec}	recovery time	$\overline{PL}$ to CPU, CPD; see Figure 11									
		V_{CC} = 4.5 V		10	2	-	13	-	15	-	ns
		MR to CPU, CPD; see Figure 12									
		V_{CC} = 4.5 V		10	0	-	13	-	15	-	ns
t_{su}	set-up time	Dn to $\overline{PL}$; see Figure 13; note: CPU = CPD = HIGH									
		V_{CC} = 4.5 V		16	8	-	20	-	24	-	ns
t_h	hold time	Dn to $\overline{PL}$; see Figure 13									
		V_{CC} = 4.5 V		0	–6	-	0	-	0	-	ns
		CPU to CPD, CPD to CPU; see Figure 15									
		V_{CC} = 4.5 V		16	7	-	20	-	24	-	ns
f_{max}	maximum frequency	CPU, CPD; see Figure 9									
		V_{CC} = 4.5 V		20	43	-	16	-	13	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} – 1.5 V; V_{CC} = 5 V; f_i = 1 MHz	[2]	-	26	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

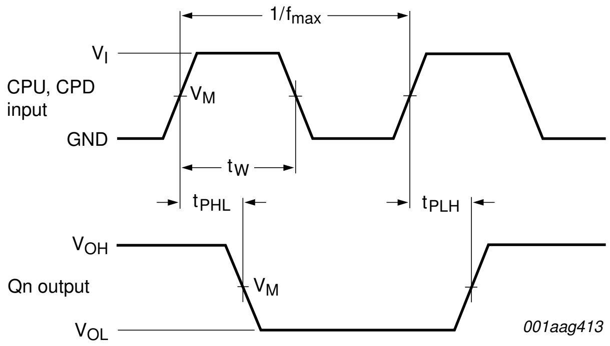
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms

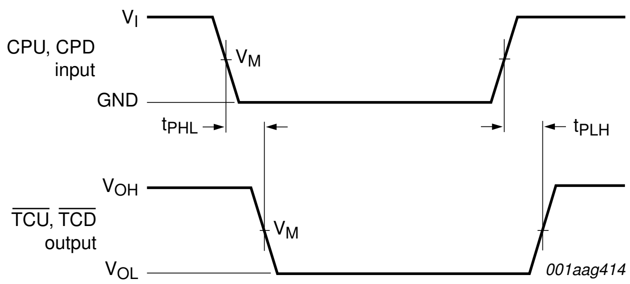


Measurement points are given in Table 10.

t_{PLH} and t_{PHL} are the same as t_{pd}.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. The clock (CPU, CPD) to output (Qn) propagation delays, the clock pulse width, and the maximum clock pulse frequency

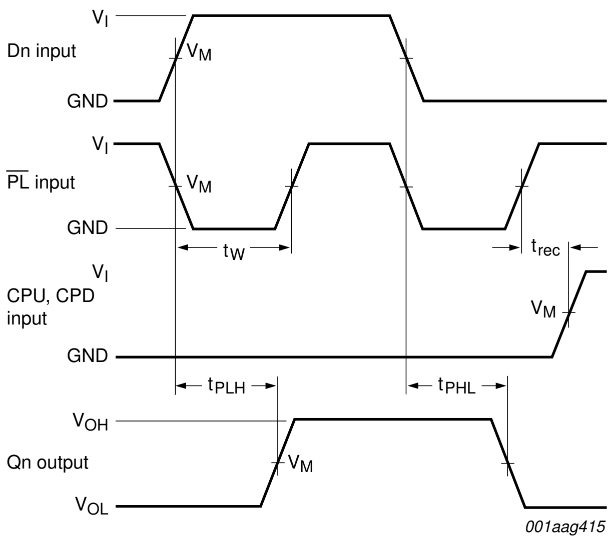


Measurement points are given in Table 10.

t_{PLH} and t_{PHL} are the same as t_{pd}.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 10. The clock (CPU, CPD) to terminal count output ($\overline{TCU}$, $\overline{TCD}$) propagation delays

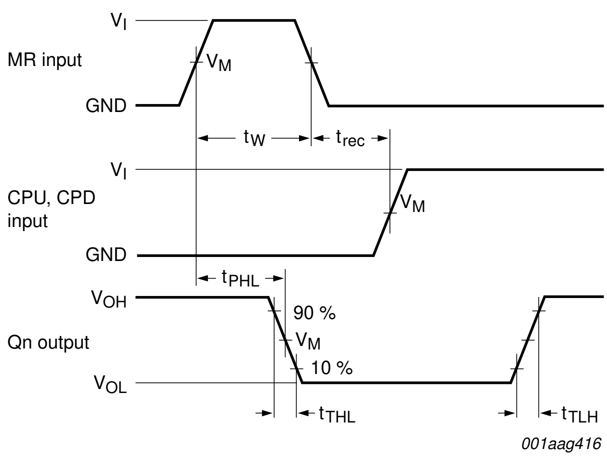


Measurement points are given in Table 10.

t_{PLH} and t_{PHL} are the same as t_{pd}.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 11. The parallel load input ($\overline{PL}$) and data (Dn) to Qn output propagation delays and $\overline{PL}$ removal time to clock input (CPU, CPD)

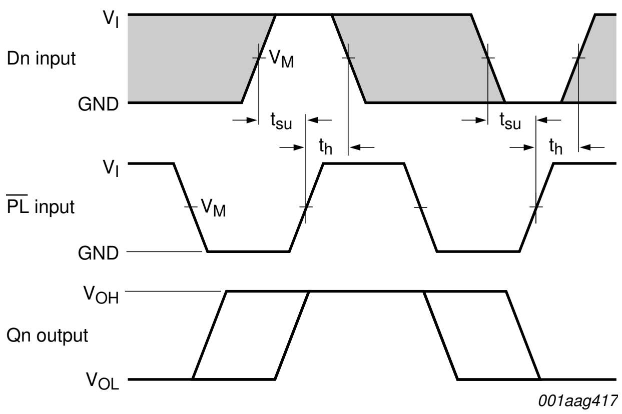


Measurement points are given in Table 10.

t_{PLH} and t_{PHL} are the same as t_{pd}.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 12. The master reset input (MR) pulse width, MR to Qn propagation delays, MR to CPU, CPD removal time and output transition times

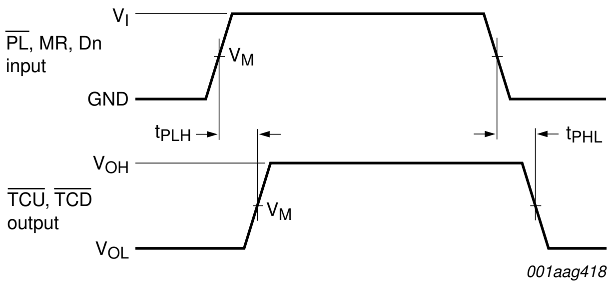


The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in Table 10.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 13. The data input (Dn) to parallel load input ($\overline{\text{PL}}$) set-up and hold times

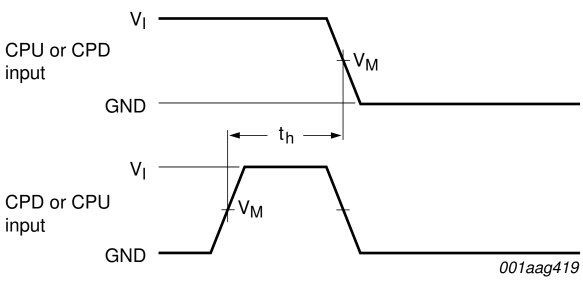


Measurement points are given in Table 10.

t_{PLH} and t_{PHL} are the same as t_{pd}.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 14. The data input (Dn), parallel load input ($\overline{\text{PL}}$) and the master reset input (MR) to the terminal count outputs ($\overline{\text{TCU}}$, $\overline{\text{TCD}}$) propagation delays

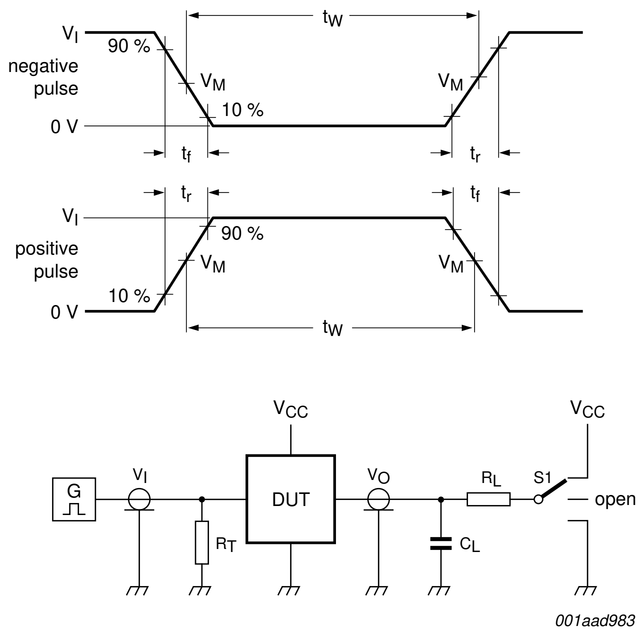


Measurement points are given in Table 10.

Fig 15. The CPU to CPD or CPD to CPU hold times

Table 10. Measurement points

Type	Input		Output
	V_M	V_I	V_M
74HC193	$0.5 \times V_{CC}$	GND to V_{CC}	$0.5 \times V_{CC}$
74HCT193	1.3 V	GND to 3 V	1.3 V



Test data is given in Table 11.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistor

S1 = Test selection switch

Fig 16. Load circuitry for measuring switching times

Table 11. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC193	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open
74HCT193	3 V	6 ns	15 pF, 50 pF	1 kΩ	open

12. Application information

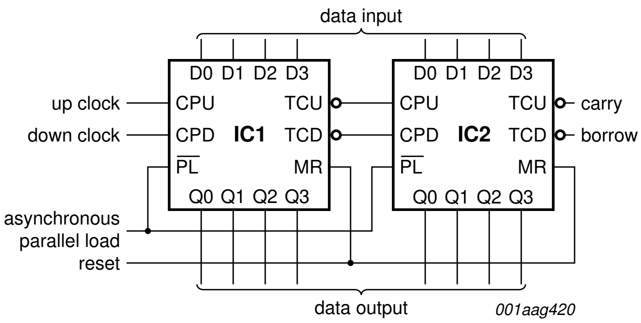
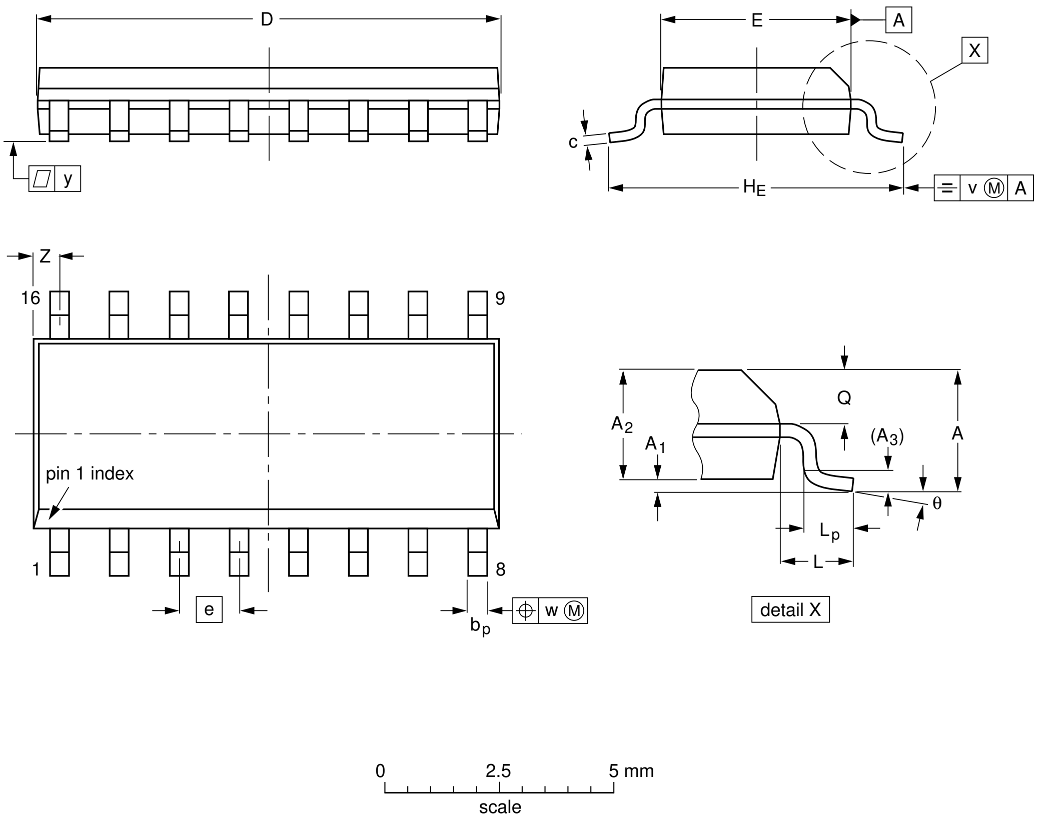


Fig 17. Application for cascaded up/down counter with parallel load

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

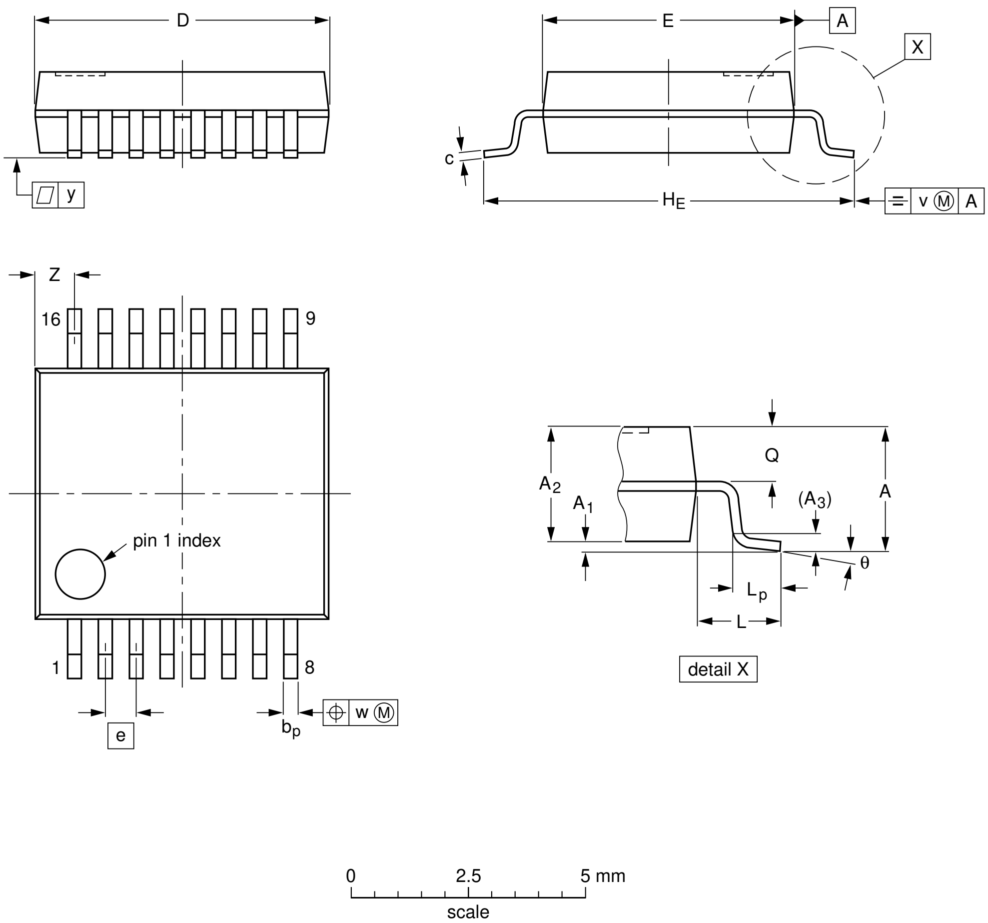
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 18. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

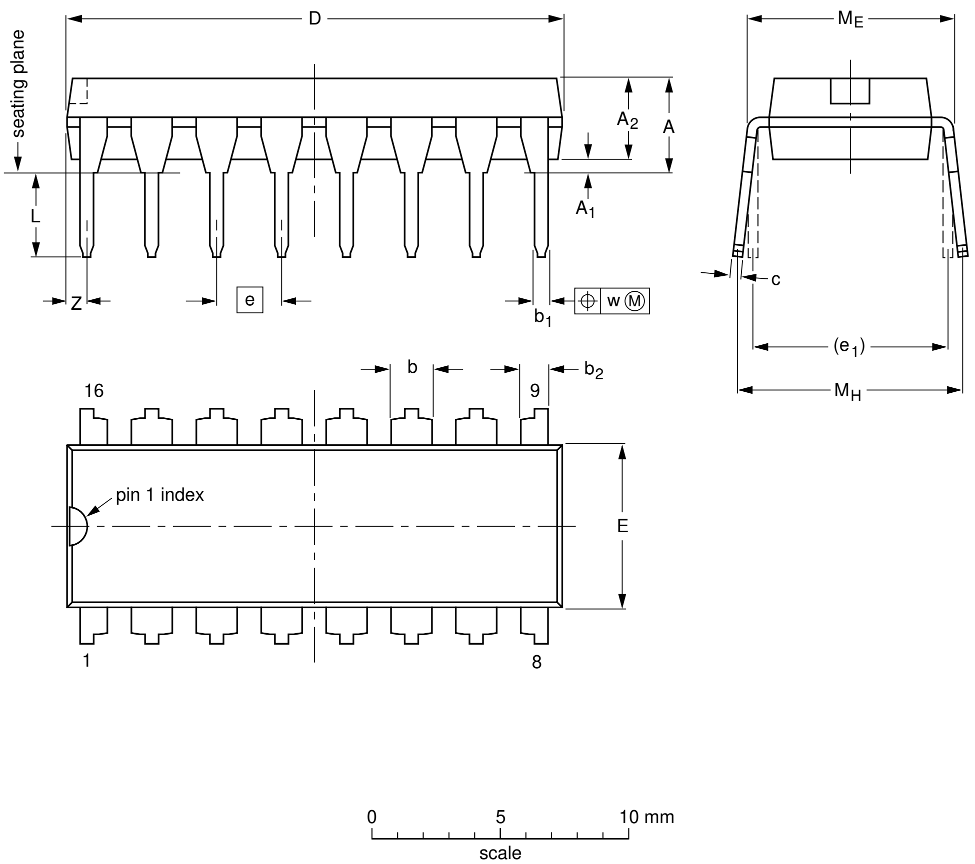
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 19. Package outline SOT338-1 (SSOP16)

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D [(1)]	E [(1)]	e	e_1	L	M_E	M_H	w	Z [(1)] max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 20. Package outline SOT38-4 (DIP16)