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74HCT9046A

PLL with band gap controlled VCO

Rev. 7 — 29 February 2016 Product data sheet

1. General description

The 74HCT9046A. This device features reduced input threshold levels to allow interfacing to TTL logic levels. Inputs also include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Operation power supply voltage range from 4.5 V to 5.5 V
- Low power consumption
- Complies with JEDEC standard no. 7A
- Inhibit control for ON/OFF keying and for low standby power consumption
- center frequency up to 17 MHz (typical) at V_{CC} = 5.5 V
- Choice of two phase comparators:
  - PC1: EXCLUSIVE-OR
  - PC2: Edge-triggered JK flip-flop
- No dead zone of PC2
- Charge pump output on PC2, whose current is set by an external resistor R_{bias}
- center frequency tolerance ±10 %
- Excellent Voltage Controlled Oscillator (VCO) linearity
- Low frequency drift with supply voltage and temperature variations
- On-chip band gap reference
- Glitch free operation of VCO, even at very low frequencies
- Zero voltage offset due to operational amplifier buffering
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

nexperia

3. Applications

- FM modulation and demodulation where a small center frequency tolerance is essential
- Frequency synthesis and multiplication where a low jitter is required (e.g. video picture-in-picture)
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HCT9046AD	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT9046APW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Block diagram

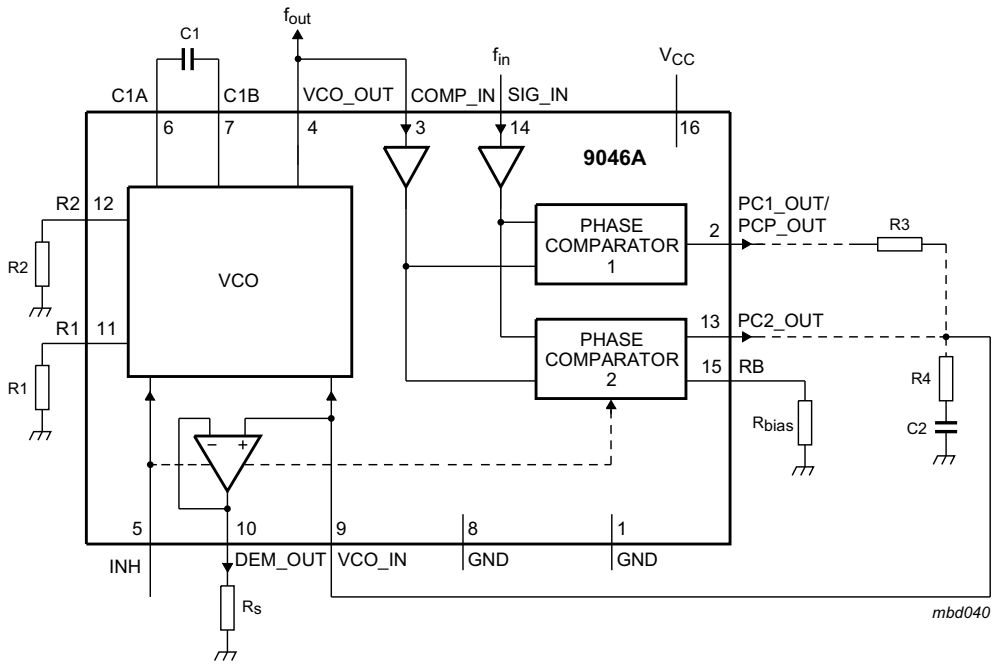


Fig 1. Block diagram

6. Functional diagram

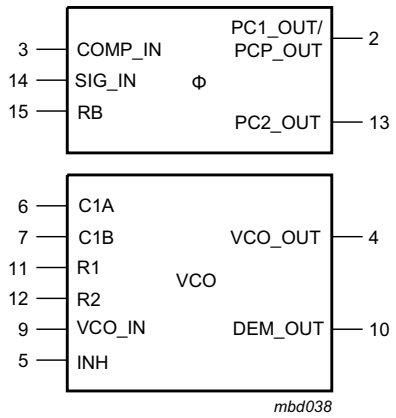


Fig 2. Logic symbol

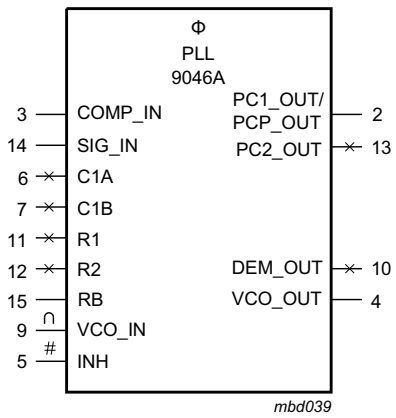


Fig 3. IEC logic symbol

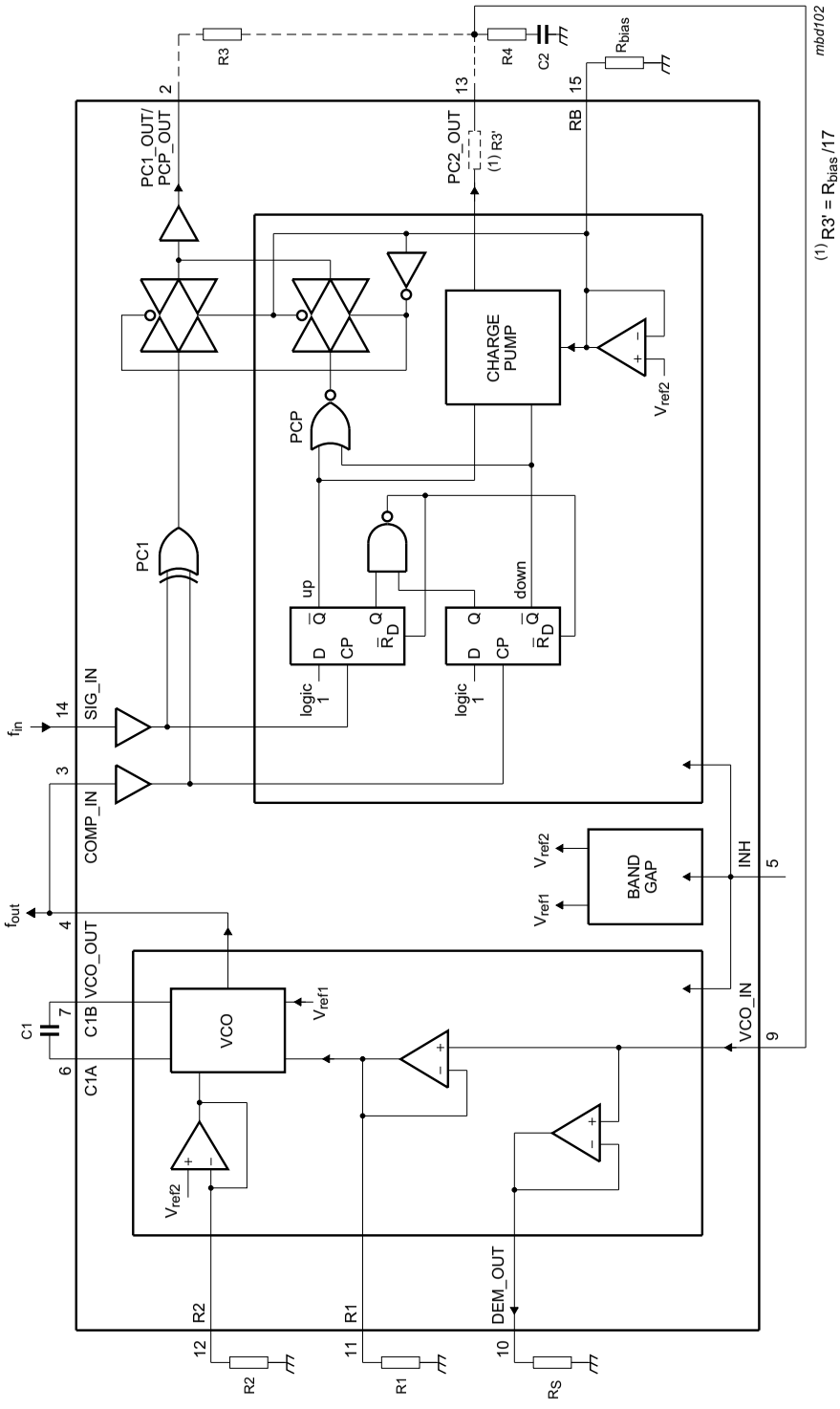


Fig 4. Logic diagram

7. Pinning information

7.1 Pinning

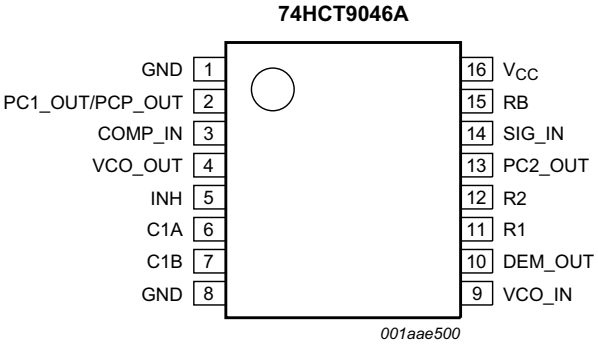


Fig 5. Pin configuration

7.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
GND	1	ground (0 V) of phase comparators
PC1_OUT/PCP_OUT	2	phase comparator 1 output or phase comparator pulse output
COMP_IN	3	comparator input
VCO_OUT	4	VCO output
INH	5	inhibit input
C1A	6	capacitor C1 connection A
C1B	7	capacitor C1 connection B
GND	8	ground (0 V) VCO
VCO_IN	9	VCO input
DEM_OUT	10	demodulator output
R1	11	resistor R1 connection
R2	12	resistor R2 connection
PC2_OUT	13	phase comparator 2 output; current source adjustable with R_{bias}
SIG_IN	14	signal input
RB	15	bias resistor (R_{bias}) connection
V_{CC}	16	supply voltage

8. Functional description

The 74HCT9046A is a phase-locked-loop circuit that comprises a linear VCO and two different phase comparators (PC1 and PC2) with a common signal input amplifier and a common comparator input, see Figure 1. The signal input can be directly coupled to large voltage signals (CMOS level), or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the 74HCT9046A forms a second-order loop PLL.

The principle of this phase-locked-loop is based on the familiar 74HCT4046A. However extra features are built-in, allowing very high-performance phase-locked-loop applications. This is done, at the expense of PC3, which is skipped in this 74HCT9046A. The PC2 is equipped with a current source output stage here. Further a band gap is applied for all internal references, allowing a small center frequency tolerance. The details are summed up in Section 8.1. If one is familiar with the 74HCT4046A already, it will do to read this section only.

8.1 Differences with respect to the familiar 74HCT4046A

- A center frequency tolerance of maximum ±10 %.
- The on board band gap sets the internal references resulting in a minimal frequency shift at supply voltage variations and temperature variations.
- The value of the frequency offset is determined by an internal reference voltage of 2.5 V instead of V_{CC} − 0.7 V; In this way the offset frequency will not shift over the supply voltage range.
- A current switch charge pump output on pin PC2_OUT allows a virtually ideal performance of PC2; The gain of PC2 is independent of the voltage across the low-pass filter; Further a passive low-pass filter in the loop achieves an active performance. The influence of the parasitic capacitance of the PC2 output plays no role here, resulting in a true correspondence of the output correction pulse and the phase difference even up to phase differences as small as a few nanoseconds.
- Because of its linear performance without dead zone, higher impedance values for the filter, hence lower C-values, can be chosen; correct operation will not be influenced by parasitic capacitances as in case of the voltage source output using the 74HCT4046A.
- No PC3 on pin RB but instead a resistor connected to GND, which sets the load/unload currents of the charge pump (PC2).
- Extra GND pin 1 to allow an excellent FM demodulator performance even at 10 MHz and higher.
- Combined function of pin PC1_OUT/PCP_OUT. If pin RB is connected to V_{CC} (no bias resistor R_{bias}) pin PC1_OUT/PCP_OUT has its familiar function viz. output of PC1. If at pin RB a resistor (R_{bias}) is connected to GND it is assumed that PC2 has been chosen as phase comparator. Connection of R_{bias} is sensed by internal circuitry and this changes the function of pin PC1_OUT/PCP_OUT into a lock detect output (PCP_OUT) with the same characteristics as PCP_OUT of pin 1 of the 74HCT4046A.

- The inhibit function differs. For the 74HCT4046A a HIGH-level at the inhibit input (pin INH) disables the VCO and demodulator, while a LOW-level turns both on. For the 74HCT9046A a HIGH-level on the inhibit input disables the whole circuit to minimize standby power consumption.

8.2 VCO

The VCO requires one external capacitor C1 (between pins C1A and C1B) and one external resistor R1 (between pins R1 and GND) or two external resistors R1 and R2 (between pins R1 and GND, and R2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required (see Figure 4).

The high input impedance of the VCO simplifies the design of the low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin DEM_OUT. The DEM_OUT voltage equals that of the VCO input. If DEM_OUT is used, a series resistor (R_s) should be connected from pin DEM_OUT to GND; if unused, DEM_OUT should be left open. The VCO output (pin VCO_OUT) can be connected directly to the comparator input (pin COMP_IN), or connected via a frequency divider. The output signal has a duty cycle of 50 % (maximum expected deviation 1 %), if the VCO input is held at a constant DC level. A LOW-level at the inhibit input (pin INH) enables the VCO and demodulator, while a HIGH-level turns both off to minimize standby power consumption.

8.3 Phase comparators

The signal input (pin SIG_IN) can be directly coupled to the self-biasing amplifier at pin SIG_IN, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

8.3.1 Phase Comparator 1 (PC1)

This circuit is an EXCLUSIVE-OR network. The signal and comparator input frequencies (f_i) must have a 50 % duty cycle to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is:

$$V_{DEM\_OUT} = \frac{V_{CC}}{\pi}(\Phi_{SIG\_IN} - \Phi_{COMP\_IN})$$

where:

V_{DEM_OUT} is the demodulator output at pin DEM_OUT

$V_{DEM\_OUT} = V_{PC1\_OUT}$ (via low-pass)

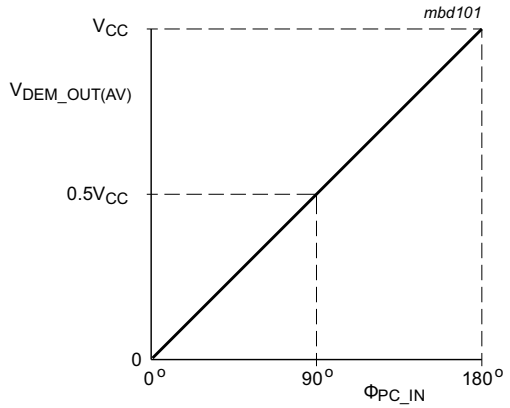
The phase comparator gain is: $K_p = \frac{V_{CC}}{\pi}(V/r)$

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin DEM_OUT (V_{DEM_OUT}), is the resultant of the phase differences of signals (SIG_IN) and the comparator input (COMP_IN) as shown in Figure 6. The average of V_{DEM_OUT} is equal to $0.5V_{CC}$ when there is no signal or noise at SIG_IN and with this input the VCO oscillates at the center frequency (f_0). Typical waveforms for the PC1 loop locked at f_0 are shown in Figure 7. This figure also shows the

actual waveforms across the VCO capacitor at pins C1A and C1B (V_{C1A} and V_{C1B}) to show the relation between these ramps and the VCO_OUT voltage.

The frequency capture range ($2f_0$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is defined as the frequency range of the input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration remains locked even with very noisy input signals. Typical behavior of this type of phase comparator is that it may lock to input frequencies close to the harmonics of the VCO center frequency.



$$V_{DEM\_OUT} = V_{PCI\_OUT} = \frac{V_{CC}}{\pi}\Phi_{SIG\_IN} - \Phi_{COMP\_IN}$$

$$\Phi_{PC\_IN} = (\Phi_{SIG\_IN} - \Phi_{COMP\_IN})$$

Fig 6. Phase comparator 1; average output voltage as a function of input phase difference

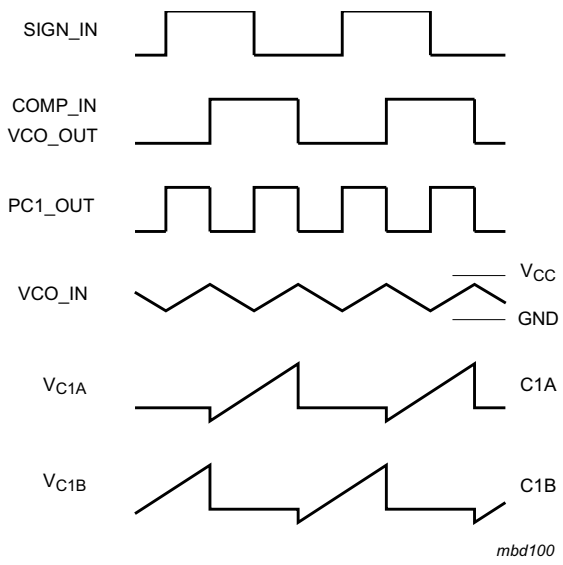


Fig 7. Typical waveforms for PLL using phase comparator 1; loop-locked at f_0

8.3.2 Phase Comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty cycles of SIG_IN and COMP_IN are not important. PC2 comprises two D-type flip-flops, control gating and a 3-state output stage with sink and source transistors acting as current sources, henceforth called charge pump output of PC2. The circuit functions as an up-down counter (see Figure 4) where SIG_IN causes an up-count and COMP_IN a down count. The current switch charge pump output allows a virtually ideal performance of PC2, due to appliance of some pulse overlap of the up and down signals, see Figure 8a.

The pump current I_{cp} is independent from the supply voltage and is set by the internal band gap reference of 2.5 V.

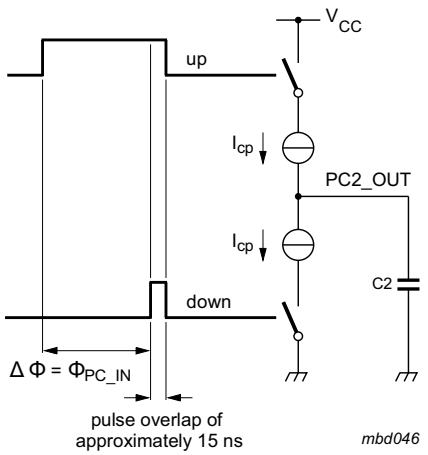
$$I_{cp} = 17 \times \frac{2.5}{R_{bias}}(A)$$

Where R_{bias} is the external bias resistor between pin RB and ground.

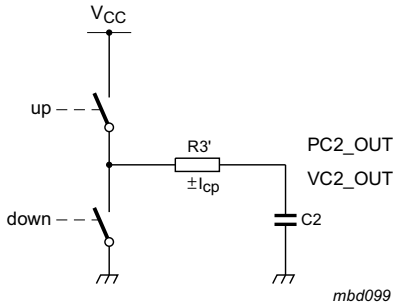
The current and voltage transfer function of PC2 are shown in Figure 9.

The phase comparator gain is:

$$K_P = \frac{|I_{cp}|}{2\pi}(A/r)$$

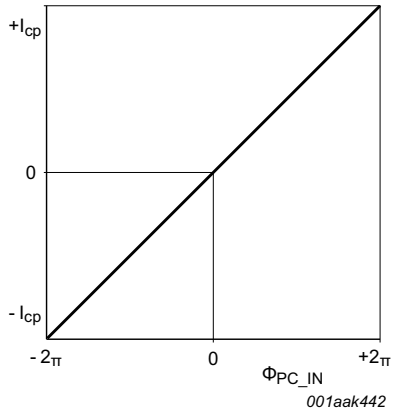


a. At every ΔΦ, even at zero ΔΦ both switches are closed simultaneously for a short period (typically 15 ns).



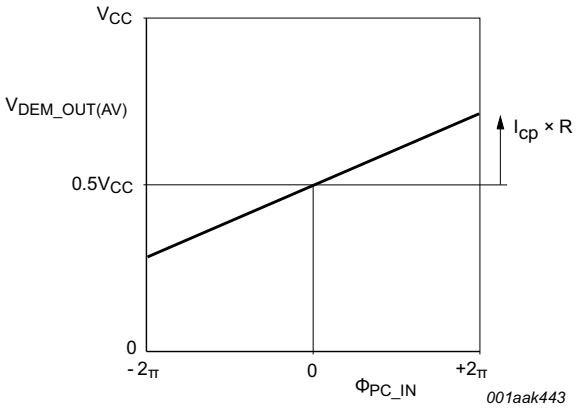
b. Comparable voltage-controlled switch

Fig 8. The current switch charge pump output of PC2



a. Current transfer

$$pump\ current\ \frac{|I_{cp}|}{2\pi}\Phi_{PC\_IN}$$



b. Voltage transfer. This transfer can be observed at PC2_OUT by connecting a resistor (R = 10 kΩ) between PC2_OUT and $0.5V_{CC}$.

$$V_{DEM\_OUT} = V_{PC2\_OUT} = \frac{5}{4\pi}\Phi_{PC\_IN}$$

$$\Phi_{PC\_IN} = (\Phi_{SIG\_IN} - \Phi_{COMP\_IN})$$

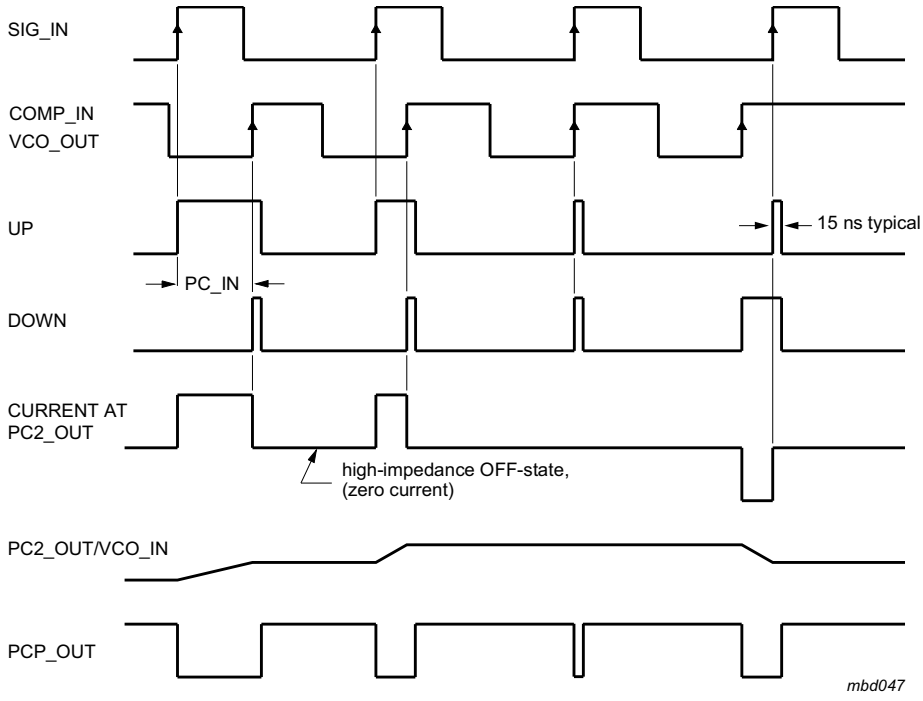
Fig 9. Phase comparator 2 current and voltage transfer characteristics

When the frequencies of SIG_IN and COMP_IN are equal but the phase of SIG_IN leads that of COMP_IN, the up output driver at PC2_OUT is held 'ON' for a time corresponding to the phase difference (Φ_{PC_IN}). When the phase of SIG_IN lags that of COMP_IN, the down or sink driver is held 'ON'.

When the frequency of SIG_IN is higher than that of COMP_IN, the source output driver is held 'ON' for most of the input signal cycle time and for the remainder of the cycle time both drivers are 'OFF' (3-state). If the SIG_IN frequency is lower than the COMP_IN frequency, then it is the sink driver that is held 'ON' for most of the cycle. Subsequently the voltage at the capacitor (C2) of the low-pass filter connected to PC2_OUT varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high-impedance. Also in this condition the signal at the phase comparator pulse output (PCP_OUT) has a minimum output pulse width equal to the overlap time, so can be used for indicating a locked condition.

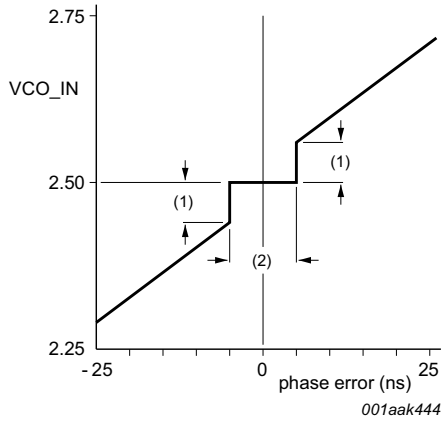
Thus for PC2 no phase difference exists between SIG_IN and COMP_IN over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_IN the VCO adjust, via PC2, to its lowest frequency.

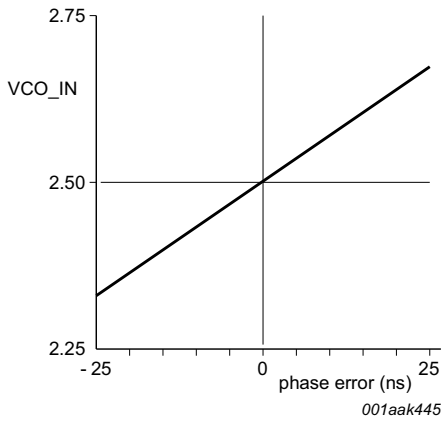
By using current sources as charge pump output on PC2, the dead zone or backlash time could be reduced to zero. Also, the pulse widening due to the parasitic output capacitance plays no role here. This enables a linear transfer function, even in the vicinity of the zero crossing. The differences between a voltage switch charge pump and a current switch charge pump are shown in Figure 11.



The pulse overlap of the up and down signals (typically 15 ns).

Fig 10. Timing diagram for PC2





(1) Due to parasitic capacitance on PC2_OUT.

(2) Backlash time (dead zone).

a. Response with traditional voltage-switch charge-pump PC2_OUT (74HCT4046A).

b. Response with current switch charge-pump PC2_OUT as applied in the 74HCT9046A.

Fig 11. The response of a locked-loop in the vicinity of the zero crossing of the phase error

The design of the low-pass filter is somewhat different when using current sources. The external resistor R3 is no longer present when using PC2 as phase comparator.
The current source is set by R_{bias}. A simple capacitor behaves as an ideal integrator now, because the capacitor is charged by a constant current. The transfer function of the voltage switch charge pump may be used. In fact it is even more valid, because the transfer function is no longer restricted for small changes only. Further the current is independent from both the supply voltage and the voltage across the filter. For one that is familiar with the low-pass filter design of the 74HCT4046A a relation may show how R_{bias} relates with a fictive series resistance, called R3'.

This relation can be derived by assuming first that a voltage controlled switch PC2 of the 74HCT4046A is connected to the filter capacitance C2 via this fictive R3' (see Figure 8b). Then during the PC2 output pulse the charge current equals:

$$|I_{cp}| = \frac{V_{CC} - V_{C2(0)}}{R3'}$$

With the initial voltage $V_{C2(0)}$ at: $0.5V_{CC}$ = 2.5 V, $|I_{cp}| = \frac{2.5}{R3'}$

As shown before the charge current of the current switch of the 74HCT9046A is:

$$|I_{cp}| = 17 \times \frac{2.5}{R_{bias}}$$

Hence:

$$R3' = \frac{R_{bias}}{17}(\Omega)$$

Using this equivalent resistance R3' for the filter design the voltage can now be expressed as a transfer function of PC2; assuming ripple ($f_r = f_i$) is suppressed, as:

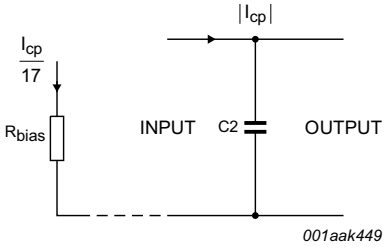
$$K_{PC2} = \frac{5}{4\pi}(V/r)$$

Again this illustrates the supply voltage independent behavior of PC2.

8.4 Loop filter component selection

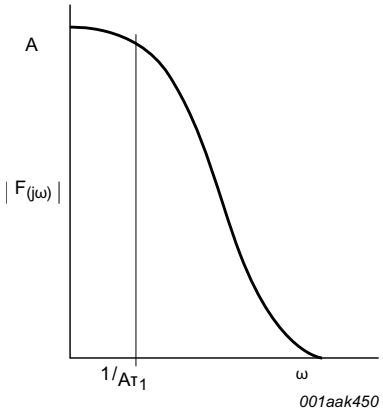
Examples of PC2 combined with a passive filter are shown in Figure 12 and 13. Figure 12 shows that PC2 with only a C2 filter behaves as a high-gain filter. For stability the damped version of Figure 13 with series resistance R4 is preferred.

Practical design values for R_{bias} are between 25 kΩ and 250 kΩ with R3' = 1.5 kΩ to 15 kΩ for the filter design. Higher values for R3' require lower values for the filter capacitance which is very advantageous at low values of the loop natural frequency ω_n.



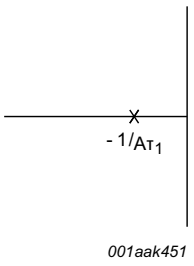
a. Simple loop filter for PC2 without damping

$$\tau_1 = \frac{R_{bias}}{17} \times C2 = R3' \times C2$$



b. Amplitude characteristic

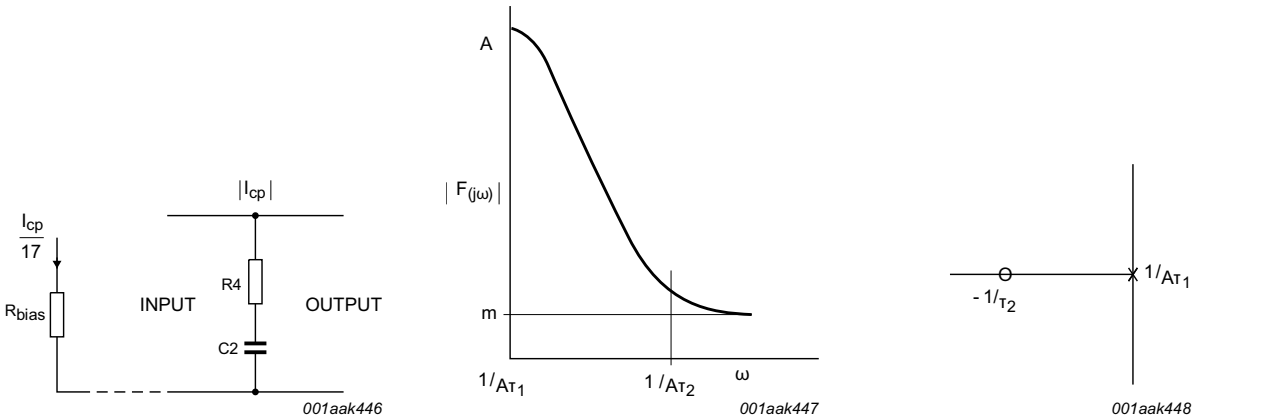
$$F_{(j\omega)} = \frac{1}{1/A + j\omega\tau_1} \approx \frac{1}{j\omega\tau_1}$$



c. Pole zero diagram

A = DC gain limit, due to leakage

Fig 12. Simple loop filter for PC2 without damping



a. Simple loop filter for PC2 with damping

$$\tau_1 = \frac{R_{bias}}{17} \times C2 = R3' \times C2$$

$$\tau_2 = R4 \times C2$$

b. Amplitude characteristic

$$F_{(j\omega)} = \frac{1 + j\omega\tau_2}{1/A + j\omega\tau_1}$$

c. Pole zero diagram

A = DC gain limit, due to leakage

Fig 13. Simple loop filter for PC2 with damping

9. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		−50	-	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C			
		SO16 package [1]	-	500	mW
		TSSOP16 package [2]	-	500	mW

[1] P_{tot} derates linearly with 8 mW/K above 70 °C.

[2] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

10. Recommended operating conditions

Table 4. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		−40		+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	pin INH; V_{CC} = 4.5 V	-	1.67	139	ns/V

11. Static characteristics

Table 5. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
Phase comparator section						
V_{IH}	HIGH-level input voltage	pins SIG_IN and COMP_IN; V_{CC} = 4.5 V; DC coupled	3.15	2.4	-	V
V_{IL}	LOW-level input voltage	pins SIG_IN and COMP_IN; V_{CC} = 4.5 V; DC coupled	-	2.1	1.35	V
V_{OH}	HIGH-level output voltage	pins PCP_OUT and PCn_OUT; V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}				
		I_O = −20 μA	4.4	4.5	-	V
		I_O = −4.0 mA	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	pins PCP_OUT and PCn_OUT; V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}				
		I_O = 20 μA	-	0	0.1	V
		I_O = 4.0 mA	-	0.15	0.26	V
I_I	input leakage current	pins SIG_IN and COMP_IN; V_{CC} = 5.5 V; V_I = V_{CC} or GND	-	-	±30	μA
I_{OZ}	OFF-state output current	pin PC2_OUT; V_{CC} = 5.5 V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	-	-	±0.5	μA
R_I	input resistance	SIG_IN and COMP_IN; V_{CC} = 4.5 V; V_I at self-bias operating point; ΔV_I = 0.5 V; see Figure 14, 15 and 16	-	250	-	kΩ
R_{bias}	bias resistance	V_{CC} = 4.5 V	25	-	250	kΩ
I_{cp}	charge pump current	V_{CC} = 4.5 V; R_{bias} = 40 kΩ	±0.53	±1.06	±2.12	mA
VCO section						
V_{IH}	HIGH-level input voltage	pin INH; V_{CC} = 4.5 V to 5.5 V; DC coupled	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	pin INH; V_{CC} = 4.5 V to 5.5 V; DC coupled	-	1.2	0.8	V

Table 5. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	pin VCO_OUT; V_{CC} = 4.5 V; $V_I = V_{IH}$ or V_{IL}				
		I_O = −20 μA	4.4	4.5	-	V
		I_O = −4.0 mA	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	pin VCO_OUT; V_{CC} = 4.5 V; $V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA	-	0	0.1	V
		I_O = 4.0 mA	-	0.15	0.26	V
		pins C1A and C1B; V_{CC} = 4.5 V; $V_I = V_{IH}$ or V_{IL}; I_O = 4.0 mA	-	-	0.40	V
I_I	input leakage current	pins INH and VCO_IN; V_{CC} = 5.5 V; $V_I = V_{CC}$ or GND	-	-	±0.1	μA
R1	resistor 1	V_{CC} = 4.5 V	3	-	300	kΩ
R2	resistor 2	V_{CC} = 4.5 V	3	-	300	kΩ
C1	capacitor 1	V_{CC} = 4.5 V	40	-	no limit	pF
V_{VCO_IN}	voltage on pin VCO_IN	over the range specified for R1				
		V_{CC} = 4.5 V	1.1	-	3.4	V
		V_{CC} = 5.0 V	1.1	-	3.9	V
		V_{CC} = 5.5 V	1.1	-	4.4	V
Demodulator section						
R_s	series resistance	V_{CC} = 4.5 V; at R_s > 300 kΩ the leakage current can influence V_{DEM_OUT}	50	-	300	kΩ
V_{offset}	offset voltage	VCO_IN to V_{DEM_OUT}; V_{CC} = 4.5 V; $V_I = V_{VCO\_IN} = 0.5V_{CC}$; values taken over R_s range; see Figure 17	-	±20	-	mV
R_{dyn}	dynamic resistance	DEM_OUT; V_{CC} = 4.5 V; $V_{DEM\_OUT} = 0.5V_{CC}$	-	25	-	Ω
General						
I_{CC}	supply current	disabled; V_{CC} = 5.5 V; pin INH at V_{CC}	-	-	8.0	μA
ΔI_{CC}	additional supply current	pin INH; $V_I = V_{CC}$ − 2.1 V; V_{CC} = 4.5 V; other inputs at V_{CC} or GND;	-	100	360	μA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = −40 °C to +85 °C						
Phase comparator section						
V_{IH}	HIGH-level input voltage	pins SIG_IN and COMP_IN; V_{CC} = 4.5 V; DC coupled	3.15	-	-	V
V_{IL}	LOW-level input voltage	pins SIG_IN and COMP_IN; V_{CC} = 4.5 V; DC coupled	-	-	1.35	V

Table 5. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	pins PCP_OUT and PCn_OUT; V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}				
		I_O = −20 μA	4.4	-	-	V
		I_O = −4.0 mA	3.84	-	-	V
V_{OL}	LOW-level output voltage	pins PCP_OUT and PCn_OUT; V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}				
		I_O = 20 μA	-	-	0.1	V
		I_O = 4.0 mA	-	-	0.33	V
I_I	input leakage current	SIG_IN and COMP_IN; V_{CC} = 5.5 V; V_I = V_{CC} or GND	-	-	±38	μA
I_{OZ}	OFF-state output current	PC2_OUT; V_{CC} = 5.5 V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	-	-	±5.0	μA
VCO section						
V_{IH}	HIGH-level input voltage	pin INH; V_{CC} = 4.5 V to 5.5 V; DC coupled	2.0	-	-	V
V_{IL}	LOW-level input voltage	pin INH; V_{CC} = 4.5 V to 5.5 V; DC coupled	-	-	0.8	V
V_{OH}	HIGH-level output voltage	pin VCO_OUT; V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}				
		I_O = −20 μA	4.4	-	-	V
		I_O = −4.0 mA	3.84	-	-	V
V_{OL}	LOW-level output voltage	pin VCO_OUT; V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}				
		I_O = 20 μA	-	-	0.1	V
		I_O = 4.0 mA	-	-	0.33	V
		pins C1A and C1B; V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; I_O = 4.0 mA	-	-	0.47	V
I_I	input leakage current	pins INH and VCO_IN; V_{CC} = 5.5 V; V_I = V_{CC} or GND	-	-	±1.0	μA
General						
I_{CC}	supply current	disabled; V_{CC} = 5.5 V; pin INH at V_{CC}	-	-	80.0	μA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} − 2.1 V; V_{CC} = 4.5 V; other inputs at V_{CC} or GND;	-	-	450	μA
T_{amb} = −40 °C to +125 °C						
Phase comparator section						
V_{IH}	HIGH-level input voltage	pins SIG_IN and COMP_IN; V_{CC} = 4.5 V; DC coupled	3.15	-	-	V
V_{IL}	LOW-level input voltage	pins SIG_IN and COMP_IN; V_{CC} = 4.5 V; DC coupled	-	-	1.35	V

Table 5. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	pins PCP_OUT and PCn_OUT; V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}				
		I_O = −20 μA	4.4	-	-	V
		I_O = −4.0 mA	3.7	-	-	V
V_{OL}	LOW-level output voltage	pins PCP_OUT and PCn_OUT; V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}				
		I_O = 20 μA	-	-	0.1	V
		I_O = 4.0 mA	-	-	0.4	V
I_I	input leakage current	pins SIG_IN and COMP_IN; V_{CC} = 5.5 V; V_I = V_{CC} or GND	-	-	±45	μA
I_{OZ}	OFF-state output current	pin PC2_OUT; V_{CC} = 5.5 V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	-	-	±10.0	μA
VCO section						
V_{IH}	HIGH-level input voltage	pin INH; V_{CC} = 4.5 V to 5.5 V; DC coupled	2.0	-	-	V
V_{IL}	LOW-level input voltage	pin INH; V_{CC} = 4.5 V to 5.5 V; DC coupled	-	-	0.8	V
V_{OH}	HIGH-level output voltage	pin VCO_OUT; V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}				
		I_O = −20 μA	4.4	-	-	V
		I_O = −4.0 mA	3.7	-	-	V
V_{OL}	LOW-level output voltage	pin VCO_OUT; V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}				
		I_O = 20 μA	-	-	0.1	V
		I_O = 4.0 mA	-	-	0.4	V
		pins C1A and C1B; V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; I_O = 4.0 mA	-	-	0.54	V
I_I	input leakage current	pins INH and VCO_IN; V_{CC} = 5.5 V; V_{CC} or GND	-	-	±1.0	μA
General						
I_{CC}	supply current	disabled; V_{CC} = 5.5 V; pin INH at V_{CC}	-	-	160.0	μA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} − 2.1 V; V_{CC} = 4.5 V; other inputs at V_{CC} or GND;	-	-	490	μA

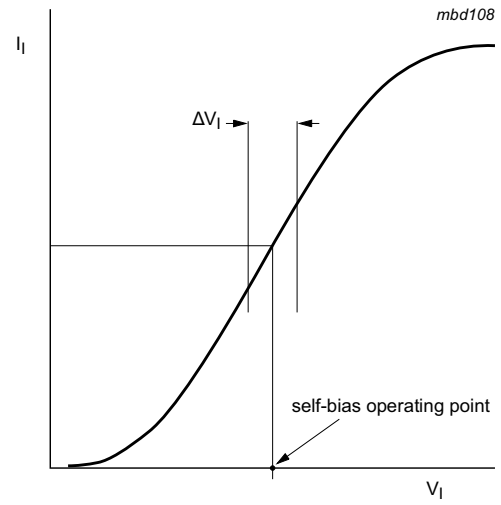


Fig 14. Typical input resistance curve at SIG_IN and COMP_IN

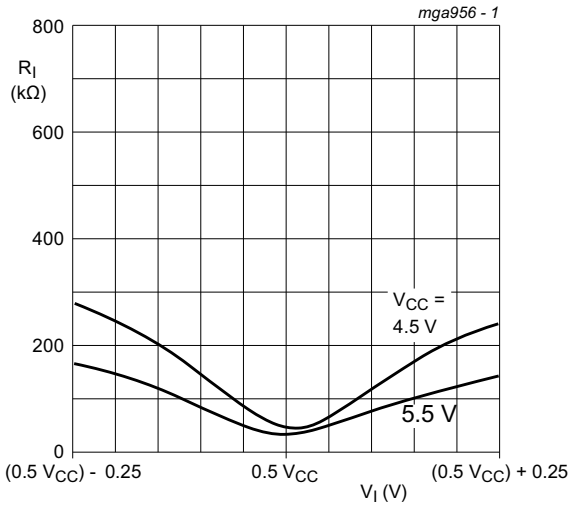


Fig 15. Input resistance at SIG_IN; COMP_IN with ΔV_I = 0.5 V at self-bias point

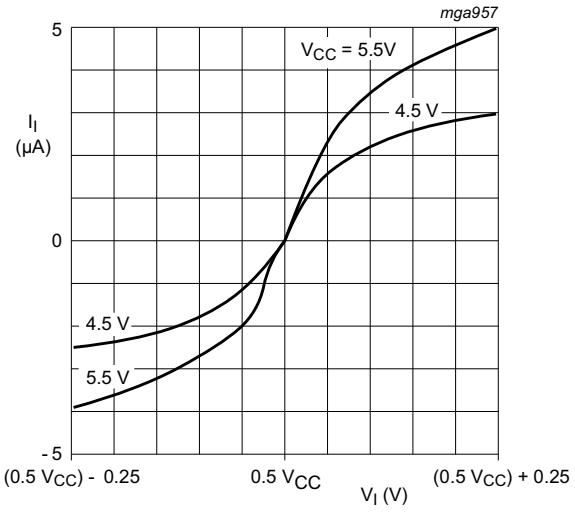


Fig 16. Input current at SIG_IN; COMP_IN with ΔV_I = 0.5 V at self-bias point

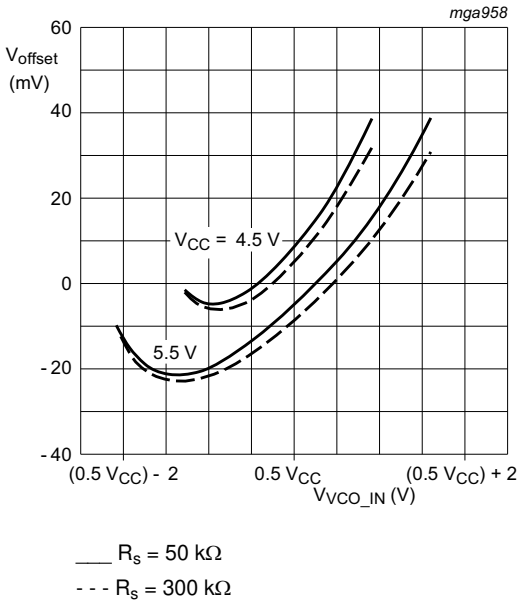


Fig 17. Offset voltage at demodulator output as a function of VCO_IN and R_s

12. Dynamic characteristics

Table 6. Dynamic characteristics[1]

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
Phase comparator section						
t_{pd}	propagation delay	SIG_IN, COMP_IN to PC1_OUT; V_{CC} = 4.5 V; see Figure 18	-	23	40	ns
		SIG_IN, COMP_IN to PCP_OUT; V_{CC} = 4.5 V; see Figure 18	-	35	68	ns
t_{en}	enable time	SIG_IN, COMP_IN to PC2_OUT; V_{CC} = 4.5 V; see Figure 19	-	30	56	ns
t_{dis}	disable time	SIG_IN, COMP_IN to PC2_OUT; V_{CC} = 4.5 V; see Figure 19	-	36	65	ns
t_t	transition time	V_{CC} = 4.5 V; see Figure 18	-	7	15	ns
$V_{i(p-p)}$	peak-to-peak input voltage	pin SIGN_IN or COMP_IN; [4] V_{CC} = 4.5 V; AC coupled; f_i = 1 MHz	-	50	-	mV
VCO section						
Δf	frequency deviation	V_{CC} = 5.0 V; V_{VCO_IN} = 3.9 V; [5] R1 = 10 kΩ; R2 = 10 kΩ; C1 = 1 nF	−10	-	+10	%
f_0	center frequency	V_{CC} = 4.5 V; duty cycle = 50 %; $V_{VCO\_IN} = 0.5V_{CC}$; R1 = 4.3 kΩ; R2 = ∞ Ω; C1 = 40 pF; see Figure 23 and 31	11.0	15.0	-	MHz
		V_{CC} = 5 V; duty cycle = 50 %; $V_{VCO\_IN} = 0.5V_{CC}$; R1 = 3 kΩ; R2 = ∞ Ω; C1 = 40 pF; see Figure 23 and 31	-	16.0	-	MHz
$\Delta f/f$	relative frequency variation	V_{CC} = 4.5 V; R1 = 100 kΩ; R2 = ∞ Ω; [6] C1 = 100 pF; see Figure 24 and 25	-	0.4	-	%
δ	duty cycle	VCO_OUT; V_{CC} = 4.5 V	-	50	-	%
General						
C_{PD}	power dissipation capacitance	[2][3]	-	20	-	pF
T_{amb} = −40 °C to +85 °C						
Phase comparator section						
t_{pd}	propagation delay	SIG_IN, COMP_IN to PC1_OUT; V_{CC} = 4.5 V; see Figure 18	-	-	50	ns
		SIG_IN, COMP_IN to PCP_OUT; V_{CC} = 4.5 V; see Figure 18	-	-	85	ns
t_{en}	enable time	SIG_IN, COMP_IN to PC2_OUT; V_{CC} = 4.5 V; see Figure 19	-	-	70	ns
t_{dis}	disable time	SIG_IN, COMP_IN to PC2_OUT; V_{CC} = 4.5 V; see Figure 19	-	-	81	ns
t_t	transition time	V_{CC} = 4.5 V; see Figure 18	-	-	19	ns

Table 6. Dynamic characteristics[1] *…continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCO section						
$\Delta f/\Delta T$	frequency variation with temperature	V_{CC} = 4.5 V; V_{VCO_IN} = 0.5V_{CC}; recommended range: R1 = 10 kΩ; R2 = 10 kΩ; C1 = 1 nF; see Figure 20, 21 and 22 [7]	-	0.06	-	%/K
T_{amb} = −40 °C to +125 °C						
Phase comparator section						
t_{pd}	propagation delay	SIG_IN, COMP_IN to PC1_OUT; V_{CC} = 4.5 V; see Figure 18	-	-	60	ns
		SIG_IN, COMP_IN to PCP_OUT; V_{CC} = 4.5 V; see Figure 18	-	-	102	ns
t_{en}	enable time	SIG_IN, COMP_IN to PC2_OUT; V_{CC} = 4.5 V; see Figure 19	-	-	84	ns
t_{dis}	disable time	SIG_IN, COMP_IN to PC2_OUT; V_{CC} = 4.5 V; see Figure 19	-	-	98	ns
t_t	transition time	V_{CC} = 4.5 V; see Figure 18	-	-	22	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}; t_t is the same as t_{TLH} and t_{THL}.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = total load switching outputs;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

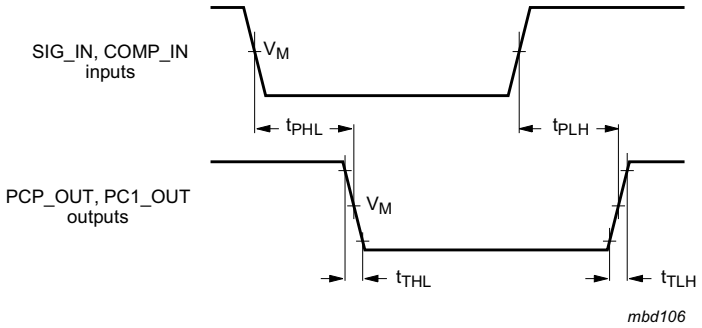
[3] Applies to the phase comparator section only (pin INH = HIGH). For power dissipation of the VCO and demodulator sections, see Figure 26, 27 and 28.

[4] This is the (peak to peak) input sensitivity.

[5] This is the center frequency tolerance.

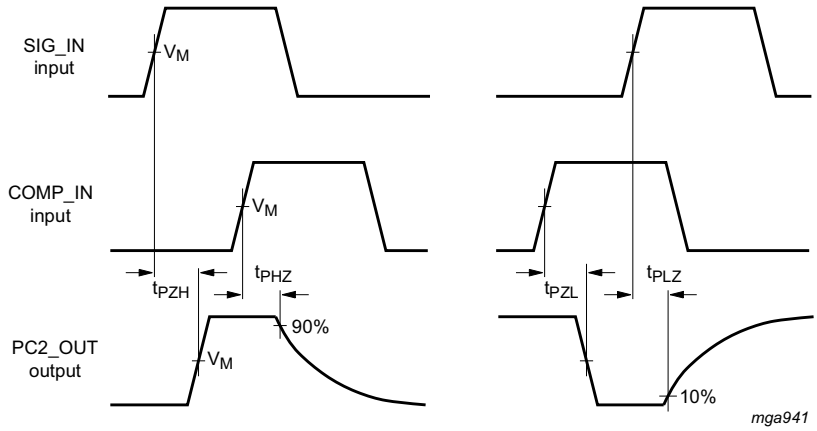
[6] This is the frequency linearity.

[7] This is the frequency stability with temperature change.



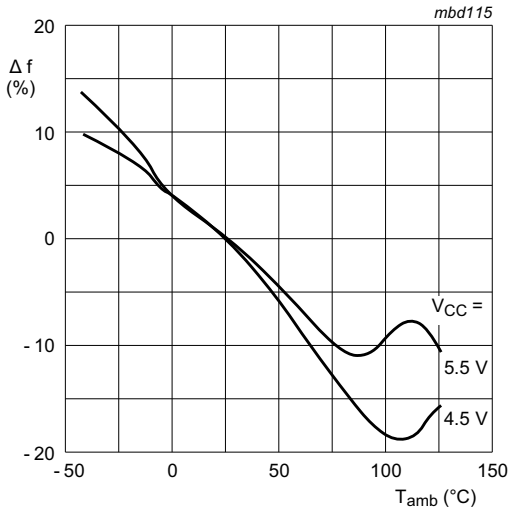
$V_M = 0.5V_{CC}$; V_I = GND to V_{CC}.

Fig 18. Waveforms showing input (SIG_IN and COMP_IN) to output (PCP_OUT and PC1_OUT) propagation delays and the output transition times

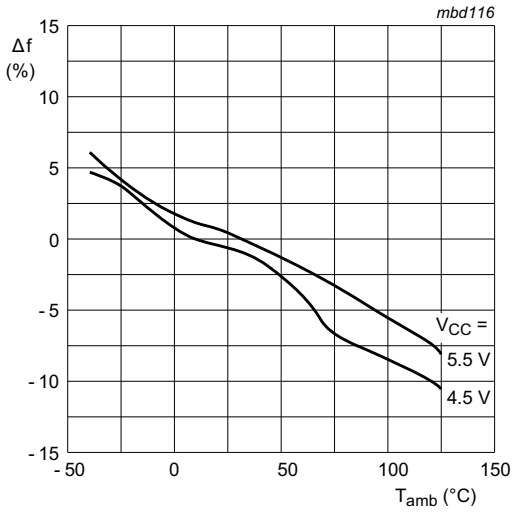


$V_M = 0.5V_{CC}$; V_I = GND to V_{CC}.

Fig 19. Waveforms showing the enable and disable times for PC2_OUT

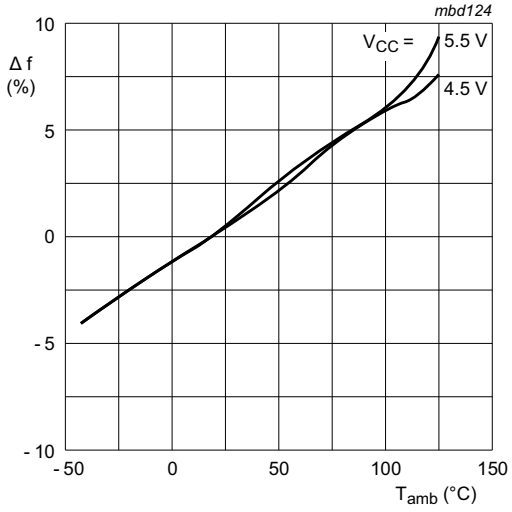


a. R1 = 3 kΩ; R2 = ∞ Ω; C1 = 100 pF.

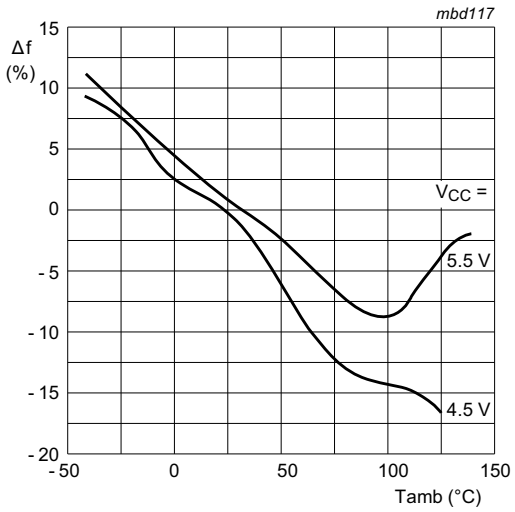


b. R1 = 10 kΩ; R2 = ∞ Ω; C1 = 100 pF.

Fig 20. Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter

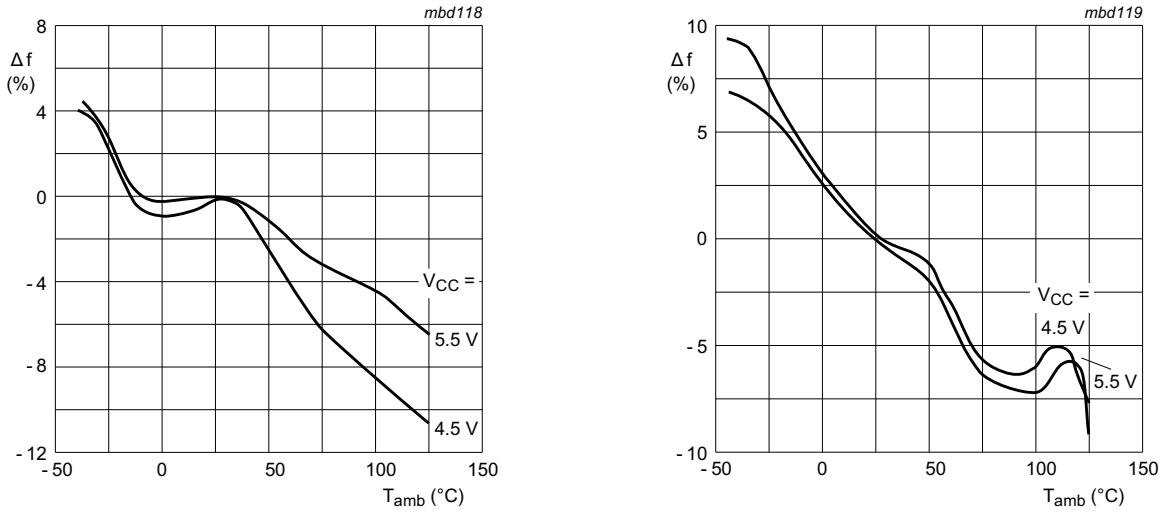


a. R1 = 300 kΩ; R2 = ∞ Ω; C1 = 100 pF.



b. R1 = ∞ Ω; R2 = 3 kΩ; C1 = 100 pF.

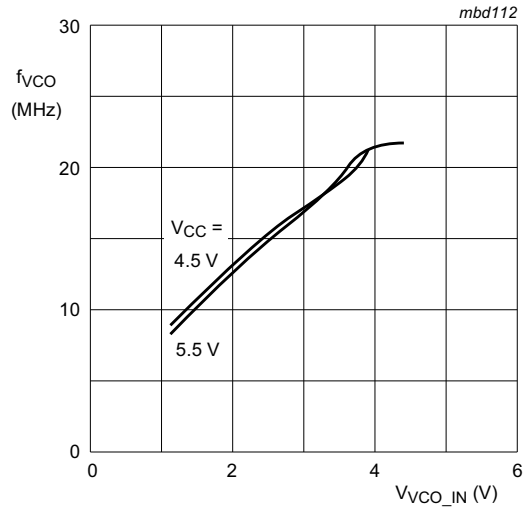
Fig 21. Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter



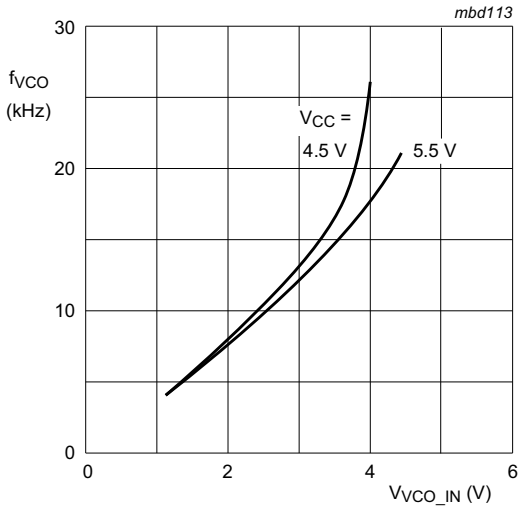
a. R1 = ∞ Ω; R2 = 10 kΩ; C1 = 100 pF.

b. R1 = ∞ Ω; R2 = 300 kΩ; C1 = 100 pF.

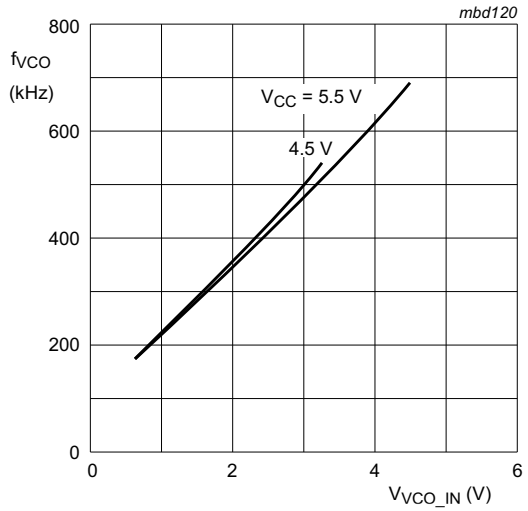
Fig 22. Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter



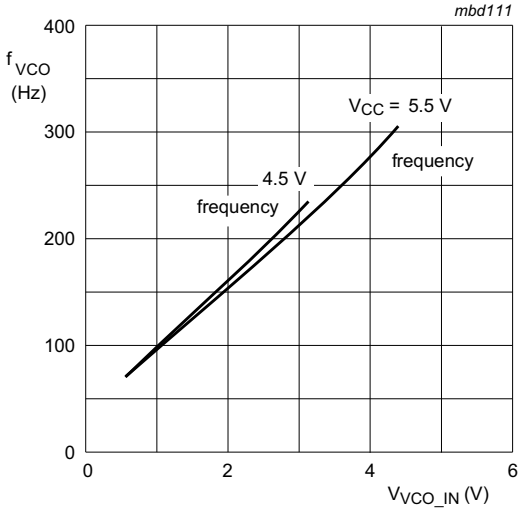
a. R1 = 4.3 kΩ; C1 = 39 pF.



b. R1 = 4.3 kΩ; C1 = 100 nF.



c. R1 = 300 kΩ; C1 = 39 pF.



d. R1 = 300 kΩ; C1 = 100 nF.

Fig 23. Graphs showing VCO frequency as a function of the VCO input voltage (V_{VCO_IN})