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FAIRCHILD SEMICONDUCTOR®

December 2013

# 74LCX574
# Low Voltage Octal D-Type Flip-Flop with 5V Tolerant Inputs and Outputs

## Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V $V_{CC}$ specifications provided
- 7.5ns $t_{PD}$ max. ($V_{CC}$ = 3.3V), 10µA $I_{CC}$ max.
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal(1)
- ±24mA output drive ($V_{CC}$ = 3.0V)
- Implements proprietary noise/EMI reduction circuitry
- Latch-up performance exceeds JEDEC 78 conditions
- ESD performance
  - – Human body model > 2000V
  - – Machine model > 200V

**Note:**

1. To ensure the high impedance state during power up or down, $\overline{OE}$ should be tied to $V_{CC}$ through a pull-up resistor: the minimum value of the resistor is determined by the current-sourcing capability of the driver.

## General Description

The LCX574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The LCX574 is functionally identical to the LCX374 except for the pinouts.

The LCX574 is designed for low voltage applications with capability of interfacing to a 5V signal environment. The LCX574 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

## Ordering Information

| Order Number | Package Number | Package Description |
|---|---|---|
| 74LCX574WM | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74LCX574SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74LCX574BQX(2) | MLP20B | 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm |
| 74LCX574MSA | MSA20 | 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide |
| 74LCX574MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

**Note:**

2. DQFN package available in Tape and Reel only.

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

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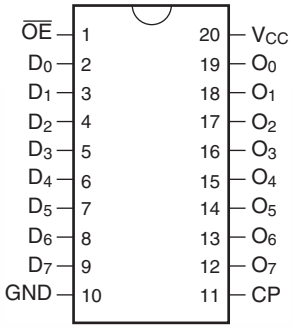
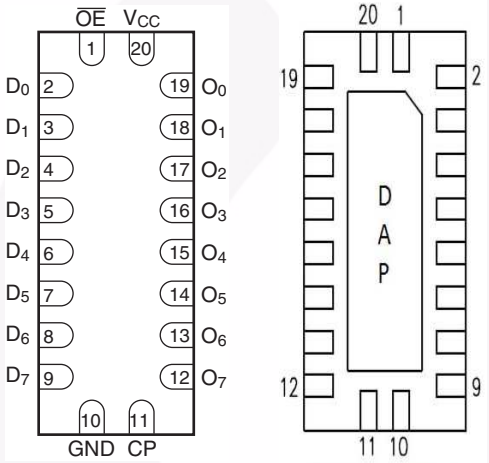
## Connection Diagrams

**Pin Assignments for SOIC, SOP, SSOP, TSSOP**




**Pad Assignments for DQFN**



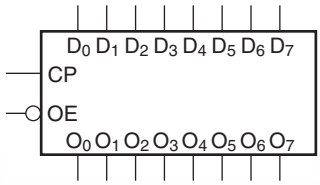

**(Top View)** **(Bottom View)**

## Pin Descriptions

| Pin Names | Description |
|---|---|
| $D_0$–$D_7$ | Data Inputs |
| CP | Clock Pulse Input |
| $\overline{OE}$ | 3-STATE Output Enable Input |
| $O_0$–$O_7$ | 3-STATE Outputs |
| DAP | No Connect |

Note: DAP (Die Attach Pad)

## Logic Symbol




## Truth Table

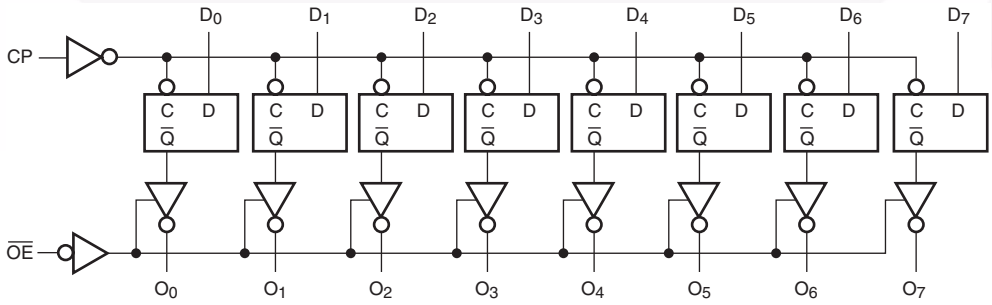
| Inputs | | | Internal | Outputs | |
|---|---|---|---|---|---|
| $\overline{OE}$ | CP | D | $\overline{Q}$ | $O_n$ | Function |
| H | H | L | NC | Z | Hold |
| H | H | H | NC | Z | Hold |
| H | ↗ | L | H | Z | Load |
| H | ↗ | H | L | Z | Load |
| L | ↗ | L | H | L | Data Available |
| L | ↗ | H | L | H | Data Available |
| L | H | L | NC | NC | No Change in Data |
| L | H | H | NC | NC | No Change in Data |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

## Functional Description

The LCX574 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the loading of the flip-flops.

## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Conditions | Value | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | –0.5 to +7.0 | V |
| $V_I$ | DC Input Voltage | | –0.5 to +7.0 | V |
| $V_O$ | DC Output Voltage | Output in 3-STATE | –0.5 to +7.0 | V |
| | | Output in HIGH or LOW State(3) | –0.5 to $V_{CC}$ + 0.5 | |
| $I_{IK}$ | DC Input Diode Current | $V_I$ < GND | –50 | mA |
| $I_{OK}$ | DC Output Diode Current | $V_O$ < GND | –50 | mA |
| | | $V_O$ > $V_{CC}$ | +50 | |
| $I_O$ | DC Output Source/Sink Current | | ±50 | mA |
| $I_{CC}$ | DC Supply Current per Supply Pin | | ±100 | mA |
| $I_{GND}$ | DC Ground Current per Ground Pin | | ±100 | mA |
| $T_{STG}$ | Storage Temperature | | –65 to +150 | °C |

## Recommended Operating Conditions(4)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Operating | 2.0 | 3.6 | V |
| | | Data Retention | 1.5 | 3.6 | |
| $V_I$ | Input Voltage | | 0 | 5.5 | V |
| $V_O$ | Output Voltage | HIGH or LOW State | 0 | $V_{CC}$ | V |
| | | 3-STATE | 0 | 5.5 | |
| $I_{OH}/I_{OL}$ | Output Current | $V_{CC}$ = 3.0V–3.6V | | ±24 | mA |
| | | $V_{CC}$ = 2.7V–3.0V | | ±12 | |
| | | $V_{CC}$ = 2.3V–2.7V | | ±8 | |
| $T_A$ | Free-Air Operating Temperature | | –40 | 85 | °C |
| $\Delta t/\Delta V$ | Input Edge Rate | $V_{IN}$ = 0.8V–2.0V, $V_{CC}$ = 3.0V | 0 | 10 | ns/V |

**Notes:**

3. $I_O$ Absolute Maximum Rating must be observed.

4. Unused inputs must be held HIGH or LOW. They may not float.

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## DC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | Conditions | $T_A$ = –40°C to +85°C | | Units |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| $V_{IH}$ | HIGH Level Input Voltage | 2.3–2.7 | | 1.7 | | V |
| | | 2.7–3.6 | | 2.0 | | |
| $V_{IL}$ | LOW Level Input Voltage | 2.3–2.7 | | | 0.7 | V |
| | | 2.7–3.6 | | | 0.8 | |
| $V_{OH}$ | HIGH Level Output Voltage | 2.3–3.6 | $I_{OH}$ = –100µA | $V_{CC}$ – 0.2 | | V |
| | | 2.3 | $I_{OH}$ = –8mA | 1.8 | | |
| | | 2.7 | $I_{OH}$ = –12mA | 2.2 | | |
| | | 3.0 | $I_{OH}$ = –18mA | 2.4 | | |
| | | | $I_{OH}$ = –24mA | 2.2 | | |
| $V_{OL}$ | LOW Level Output Voltage | 2.3–3.6 | $I_{OL}$ = 100µA | | 0.2 | V |
| | | 2.3 | $I_{OL}$ = 8mA | | 0.6 | |
| | | 2.7 | $I_{OL}$ = 12mA | | 0.4 | |
| | | 3.0 | $I_{OL}$ = 16mA | | 0.4 | |
| | | | $I_{OL}$ = 24mA | | 0.55 | |
| $I_I$ | Input Leakage Current | 2.3–3.6 | $0 \le V_I \le 5.5V$ | | ±5.0 | µA |
| $I_{OZ}$ | 3-STATE Output Leakage | 2.3–3.6 | $0 \le V_O \le 5.5V$, $V_I = V_{IH}$ or $V_{IL}$ | | ±5.0 | µA |
| $I_{OFF}$ | Power-Off Leakage Current | 0 | $V_I$ or $V_O$ = 5.5V | | 10 | µA |
| $I_{CC}$ | Quiescent Supply Current | 2.3–3.6 | $V_I = V_{CC}$ or GND | | 10 | µA |
| | | 2.3–3.6 | $3.6V \le V_I, V_O \le 5.5V$[5] | | ±10 | |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | 2.3–3.6 | $V_{IH} = V_{CC}$ –0.6V | | 500 | µA |

## AC Electrical Characteristics

| Symbol | Parameter | $T_A$ = –40°C to +85°C, $R_L$ = 500Ω | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ = 3.3V ± 0.3V, $C_L$ = 50pF | | $V_{CC}$ = 2.7V, $C_L$ = 50pF | | $V_{CC}$ = 2.5 ± 0.2V, $C_L$ = 30pF | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $f_{MAX}$ | Maximum Clock Frequency | 150 | | | | | | MHz |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay, CP to $O_n$ | 1.5 | 8.5 | 1.5 | 9.5 | 1.5 | 10.5 | ns |
| $t_{PZL}$, $t_{PZH}$ | Output Enable Time | 1.5 | 8.5 | 1.5 | 9.5 | 1.5 | 10.5 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time | 1.5 | 6.5 | 1.5 | 7.0 | 1.5 | 7.8 | ns |
| $t_S$ | Setup Time | 2.5 | | 2.5 | | 4.0 | | ns |
| $t_H$ | Hold Time | 1.5 | | 1.5 | | 2.0 | | ns |
| $t_W$ | Pulse Width | 3.3 | | 3.3 | | 4.0 | | ns |
| $t_{OSHL}$, $t_{OSLH}$ | Output to Output Skew[6] | | 1.0 | | | | | ns |

**Notes:**

5. Outputs disabled or 3-STATE only.
6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) or LOW-to-HIGH ($t_{OSLH}$).

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## Dynamic Switching Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | Conditions | $T_A = 25°C$ Typical | Units |
|---|---|---|---|---|---|
| $V_{OLP}$ | Quiet Output Dynamic Peak $V_{OL}$ | 3.3 | $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$ | 0.8 | V |
| | | 2.5 | $C_L = 30pF$, $V_{IH} = 2.5V$, $V_{IL} = 0V$ | 0.6 | |
| $V_{OLV}$ | Quiet Output Dynamic Valley $V_{OL}$ | 3.3 | $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$ | –0.8 | V |
| | | 2.5 | $C_L = 30pF$, $V_{IH} = 2.5V$, $V_{IL} = 0V$ | –0.6 | |

## Capacitance

| Symbol | Parameter | Conditions | Typical | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = Open, $V_I = 0V$ or $V_{CC}$ | 7 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{CC} = 3.3V$, $V_I = 0V$ or $V_{CC}$ | 8 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | $V_{CC} = 3.3V$, $V_I = 0V$ or $V_{CC}$, f = 10MHz | 25 | pF |

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## AC Loading and Waveforms (Generic for LCX Family)

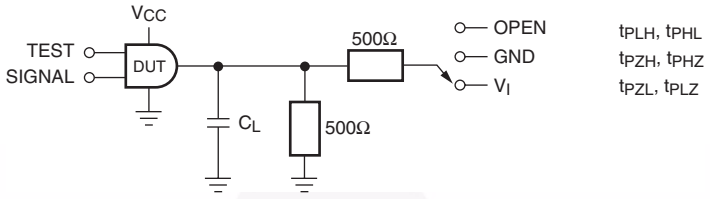
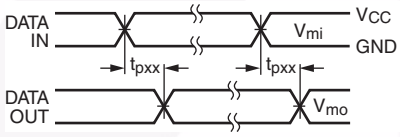
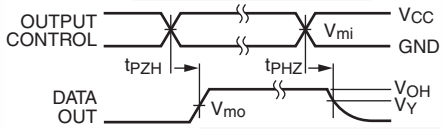



**Figure 1. AC Test Circuit ($C_L$ includes probe and jig capacitance)**

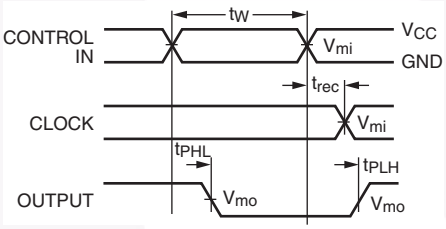
| Test | Switch |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | 6V at $V_{CC}$ = 3.3 ± 0.3V<br>$V_{CC}$ x 2 at $V_{CC}$ = 2.5 ± 0.2V |
| $t_{PZH}$, $t_{PHZ}$ | GND |



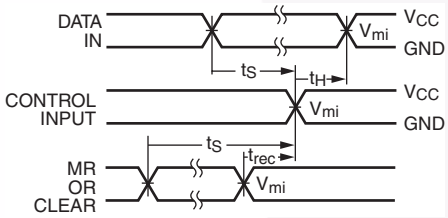

**Waveform for Inverting and Non-Inverting Functions**



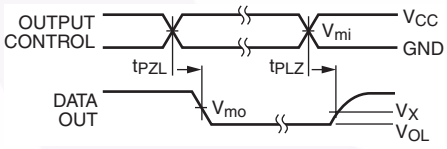

**3-STATE Output High Enable and Disable Times for Logic**



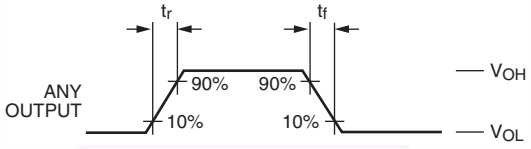

**Propagation Delay, Pulse Width and $t_{rec}$ Waveforms**




**Setup Time, Hold Time and Recovery Time for Logic**




**3-STATE Output Low Enable and Disable Times for Logic**




**$t_{rise}$ and $t_{fall}$**

**Figure 2. Waveforms (Input Characteristics; f =1MHz, $t_r$ = $t_f$ = 3ns)**

| Symbol | $V_{CC}$ | | |
|---|---|---|---|
| | 3.3V ± 0.3V | 2.7V | 2.5V ± 0.2V |
| $V_{mi}$ | 1.5V | 1.5V | $V_{CC}$ / 2 |
| $V_{mo}$ | 1.5V | 1.5V | $V_{CC}$ / 2 |
| $V_x$ | $V_{OL}$ + 0.3V | $V_{OL}$ + 0.3V | $V_{OL}$ + 0.15V |
| $V_y$ | $V_{OH}$ – 0.3V | $V_{OH}$ – 0.3V | $V_{OH}$ – 0.15V |

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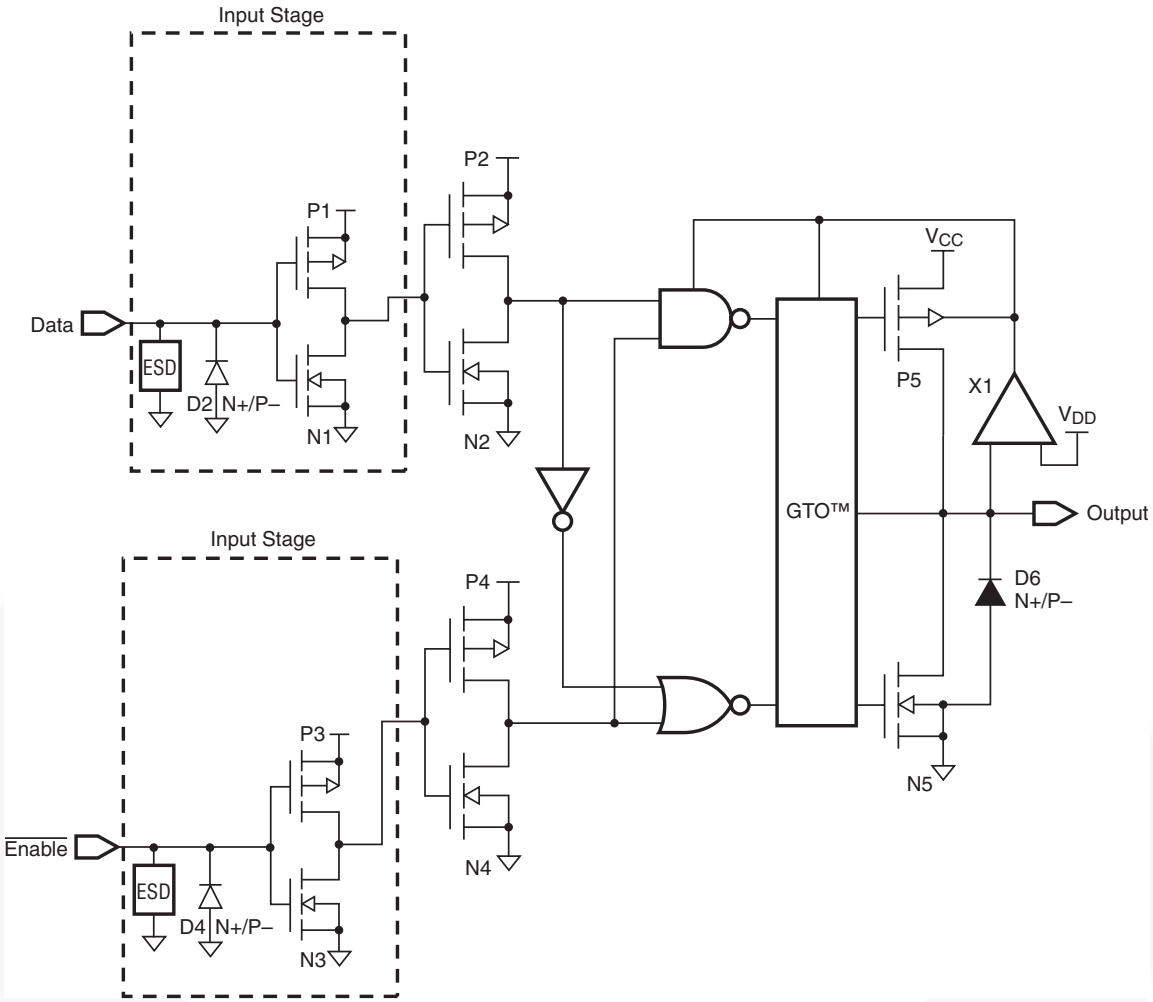
## Schematic Diagram (Generic for LCX Family)

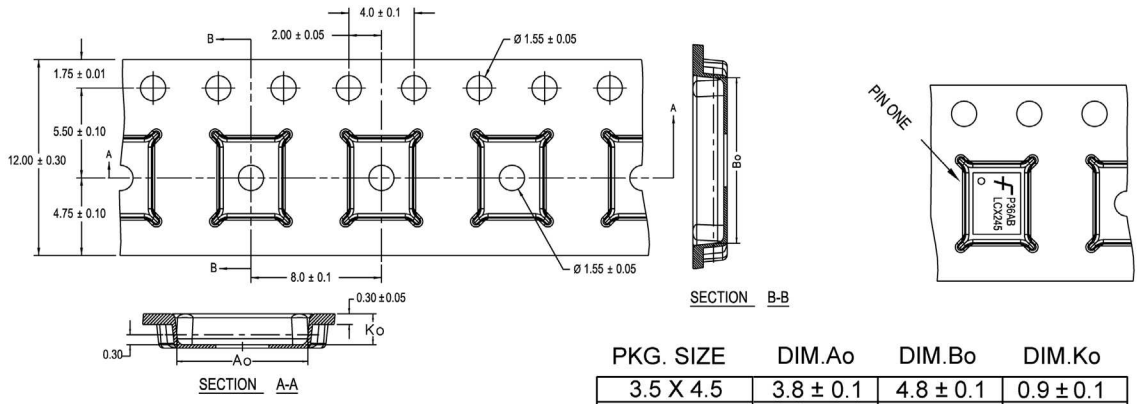


## Tape and Reel Specification

### Tape Format for DQFN

| Package Designator | Tape Section | Number Cavities | Cavity Status | Cover Tape Status |
|---|---|---|---|---|
| BQX | Leader (Start End) | 125 (typ) | Empty | Sealed |
| | Carrier | 3000 | Filled | Sealed |
| | Trailer (Hub End) | 75 (typ) | Empty | Sealed |

### Tape Dimensions inches (millimeters)



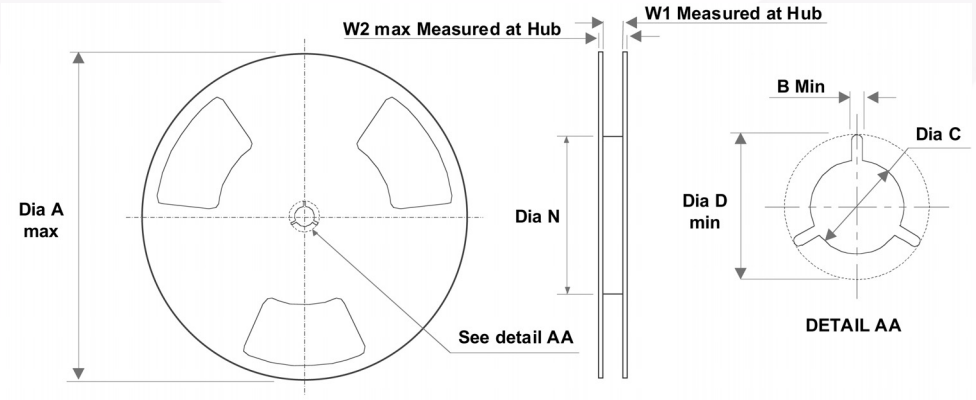

| PKG. SIZE | DIM.Ao | DIM.Bo | DIM.Ko |
|---|---|---|---|
| 3.5 X 4.5 | 3.8 ± 0.1 | 4.8 ± 0.1 | 0.9 ± 0.1 |
| 3.0 X 3.0 | 3.3 ± 0.1 | 3.3 ± 0.1 | 0.9 ± 0.1 |
| 2.5 X 4.5 | 2.8 ± 0.1 | 4.8 ± 0.1 | 0.9 ± 0.1 |
| 2.5 X 3.5 | 2.8 ± 0.1 | 3.8 ± 0.1 | 0.9 ± 0.1 |
| 2.5 X 3.0 | 2.8 ± 0.1 | 3.3 ± 0.1 | 0.9 ± 0.1 |
| 2.5 X 2.5 | 2.8 ± 0.1 | 2.8 ± 0.1 | 0.9 ± 0.1 |

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

1. Cummulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Diemension in inches rounded.

### Reel Dimensions inches (millimeters)




| Tape Size | A | B | C | D | N | W1 | W2 |
|---|---|---|---|---|---|---|---|
| 12mm | 13.0 (330.0) | 0.059 (1.50) | 0.512 (13.00) | 0.795 (20.20) | 2.165 (55.00) | 0.488 (12.4) | 0.724 (18.4) |

## Physical Dimensions

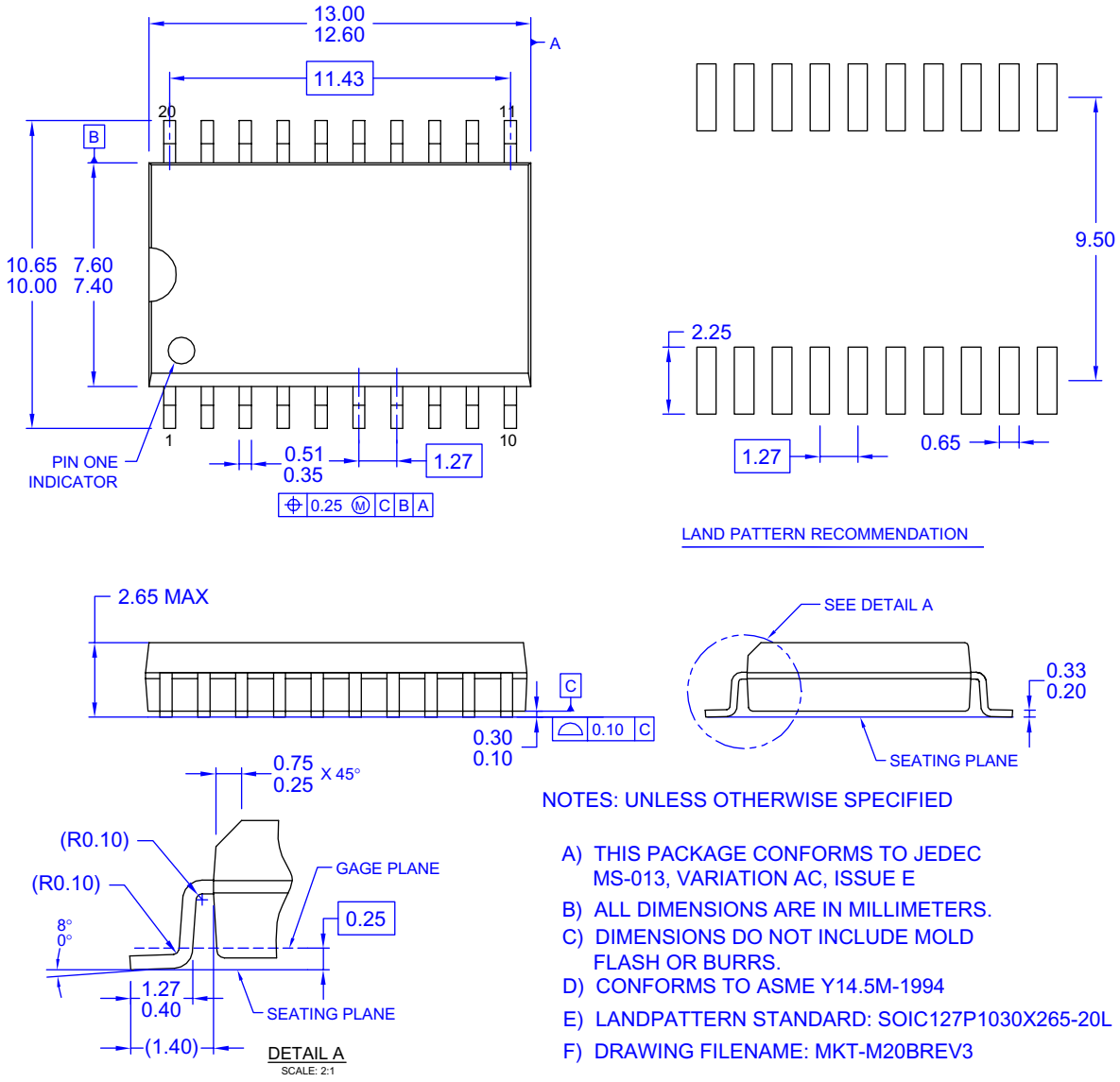



**Figure 3. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide**

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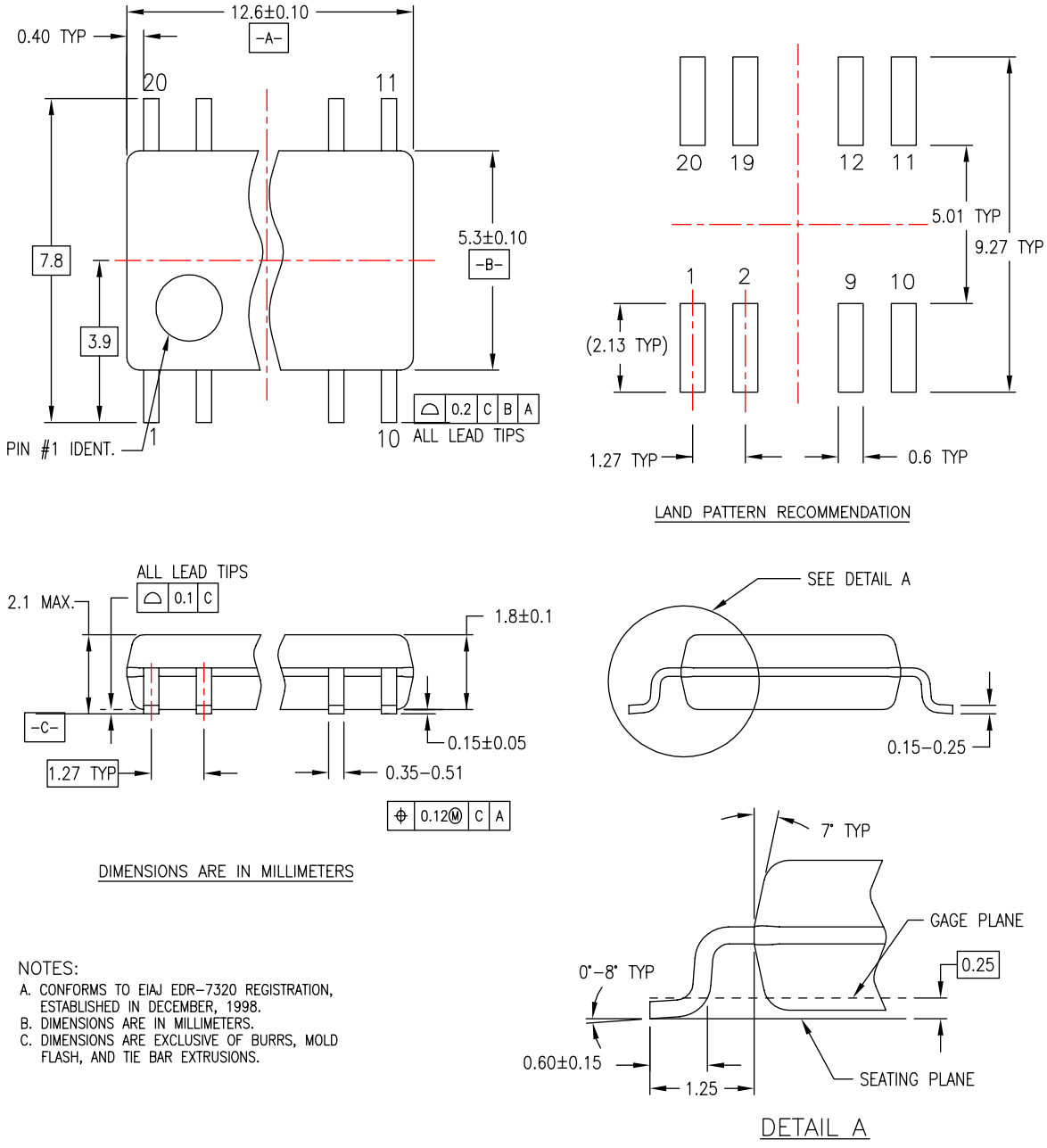
## Physical Dimensions (Continued)




NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

**Figure 4. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**

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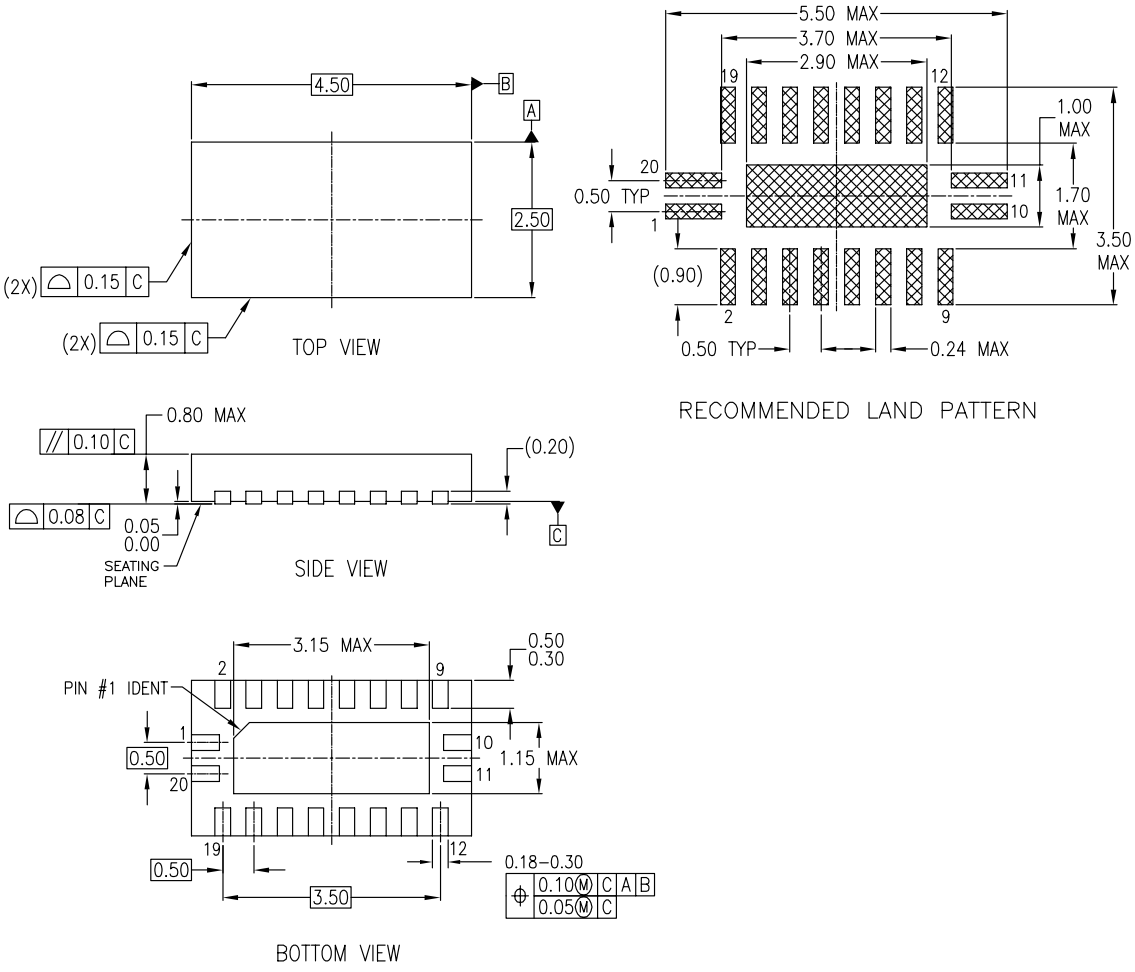
## Physical Dimensions (Continued)




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–241, VARIATION AC
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP20BrevA

**Figure 5. 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm**

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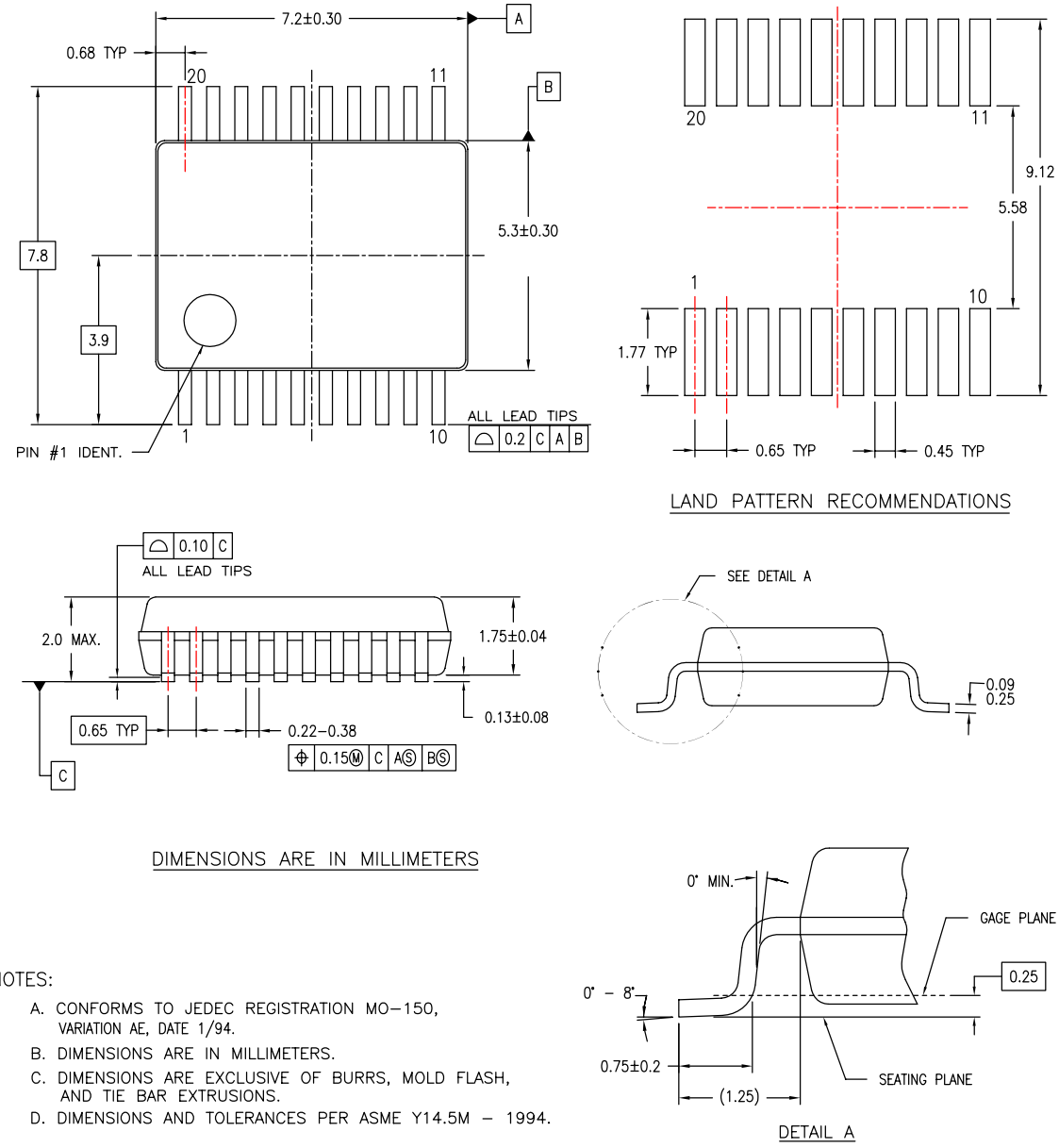
## Physical Dimensions (Continued)




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–150, VARIATION AE, DATE 1/94.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M – 1994.

MSA20REVB

**Figure 6. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide**

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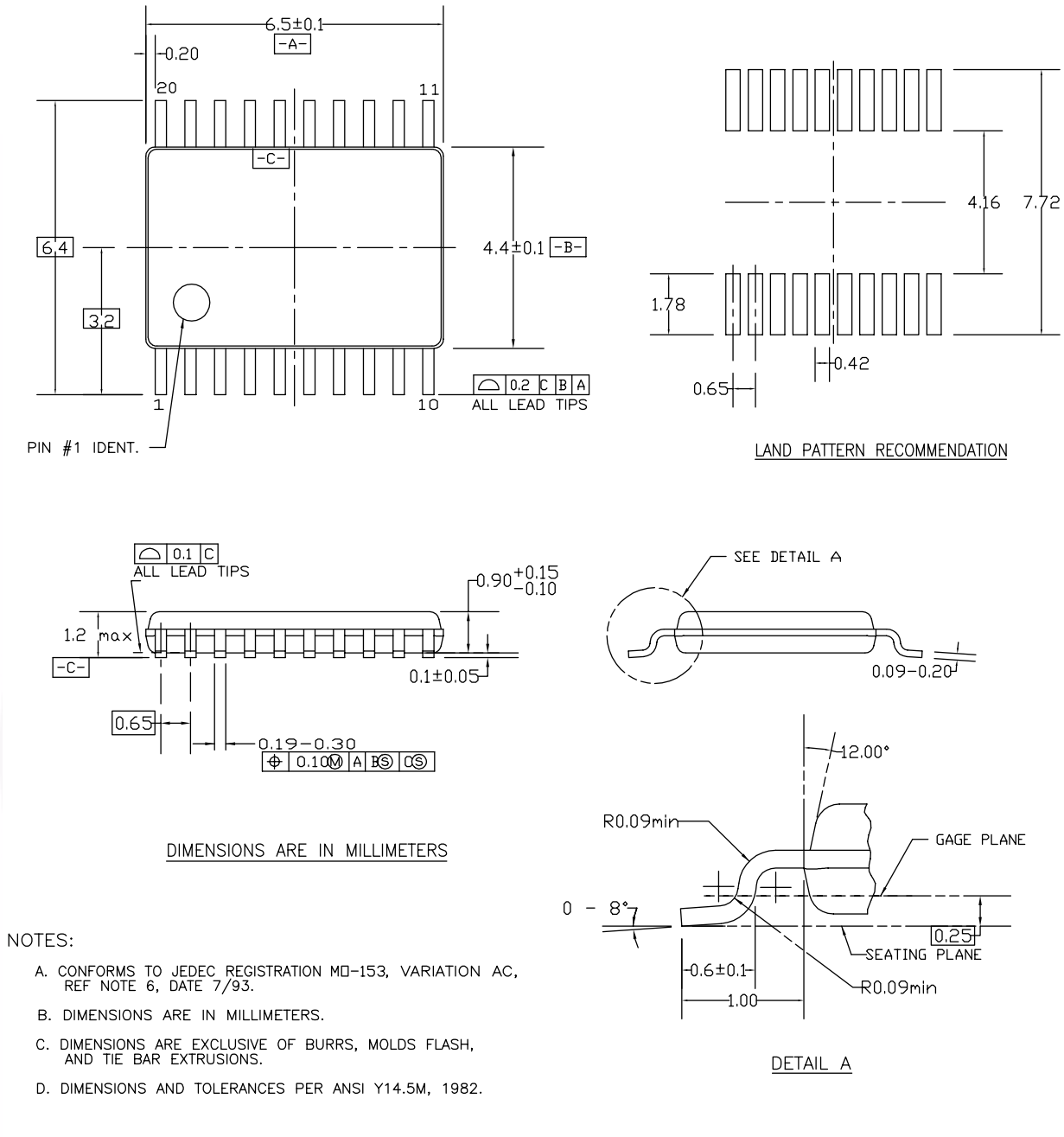
## Physical Dimensions (Continued)




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

**Figure 7. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**

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