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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD

SEMICONDUCTOR®

March 2008

74LCX86
Low Voltage Quad 2-Input Exclusive-OR Gate with 5V Tolerant Inputs

Features

■ 5V tolerant inputs

■ 2.3V–3.6V V_{CC} specifications provided

■ 6.5ns t_{PD} max. (V_{CC} = 3.3V), 10µA I_{CC} max.

■ Power down high impedance inputs and outputs

■ ±24mA output drive (V_{CC} = 3.0V)

■ Implements proprietary noise/EMI reduction circuitry

■ Latch-up performance exceeds 500mA

■ ESD performance:

   – Machine model > 2000V

   – Human model > 200V

General Description

The LCX86 contains four 2-input exclusive-OR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The 74LCX86 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Ordering Information

Order Number	Package Number	Package Description
74LCX86M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LCX86SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX86MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

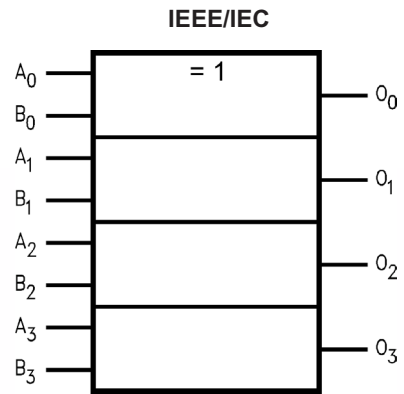| Pin		Pin	
A$_0$	1	14	V$_{CC}$
B$_0$	2	13	A$_2$
O$_0$	3	12	B$_2$
A$_1$	4	11	O$_2$
B$_1$	5	10	A$_3$
O$_1$	6	9	B$_3$
GND	7	8	O$_3$

Logic Symbol

IEEE/IEC

= 1

Inputs: A$_0$, B$_0$, A$_1$, B$_1$, A$_2$, B$_2$, A$_3$, B$_3$
Outputs: O$_0$, O$_1$, O$_2$, O$_3$
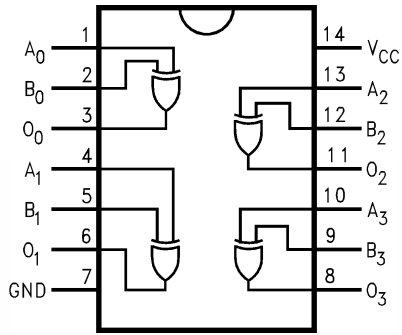
Pin Description

Pin Names	Description
A$_0$–A$_3$	Inputs
B$_0$–B$_3$	Inputs
O$_0$–O$_3$	Outputs

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_I	DC Input Voltage	–0.5V to +7.0V
V_O	DC Output Voltage, Output in HIGH or LOW State[1]	–0.5V to V_{CC} + 0.5V
I_{IK}	DC Input Diode Current, V_I < GND	–50mA
I_{OK}	DC Output Diode Current	
	V_O < GND	–50mA
	V_O > V_{CC}	+50mA
I_O	DC Output Source/Sink Current	±50mA
I_{CC}	DC Supply Current per Supply Pin	±100mA
I_{GND}	DC Ground Current per Ground Pin	±100mA
T_{STG}	Storage Temperature	–65°C to +150°C

Note:
1. I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions[2]

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage			
	Operating	2.0	3.6	V
	Data Retention	1.5	3.6	
V_I	Input Voltage	0	5.5	V
V_O	Output Voltage, HIGH or LOW State	0	V_{CC}	V
I_{OH} / I_{OL}	Output Current			
	V_{CC} = 3.0V–3.6V		±24	mA
	V_{CC} = 2.7V–3.0V		±12	
	V_{CC} = 2.3V–2.7V		±8	
T_A	Free-Air Operating Temperature	–40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

Note:
2. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V$_{CC}$ (V)	Conditions	T$_A$ = −40°C to +85°C		Units
				Min.	Max.	
V$_{IH}$	HIGH Level Input Voltage	2.3–2.7		1.7		V
		2.7–3.6		2.0		
V$_{IL}$	LOW Level Input Voltage	2.3–2.7			0.7	V
		2.7–3.6			0.8	
V$_{OH}$	HIGH Level Output Voltage	2.3–3.6	I$_{OH}$ = −100µA	V$_{CC}$ − 0.2		V
		2.3	I$_{OH}$ = −8mA	1.8		
		2.7	I$_{OH}$ = −12mA	2.2		
		3.0	I$_{OH}$ = −18mA	2.4		
			I$_{OH}$ = −24mA	2.2		
V$_{OL}$	LOW Level Output Voltage	2.3–3.6	I$_{OL}$ = 100µA		0.2	V
		2.3	I$_{OL}$ = 8mA		0.6	
		2.7	I$_{OL}$ = 12mA		0.4	
		3.0	I$_{OL}$ = 16mA		0.4	
			I$_{OL}$ = 24mA		0.55	
I$_I$	Input Leakage Current	2.3–3.6	0 ≤ V$_I$ ≤ 5.5V		±5.0	µA
I$_{OFF}$	Power-Off Leakage Current	0	V$_I$ or V$_O$ = 5.5V		10	µA
I$_{CC}$	Quiescent Supply Current	2.3–3.6	V$_I$ = V$_{CC}$ or GND		10	µA
			3.6V ≤ V$_I$ ≤ 5.5V		±10	
ΔI$_{CC}$	Increase in I$_{CC}$ per Input	2.3–3.6	V$_{IH}$ = V$_{CC}$ − 0.6V		500	µA

AC Electrical Characteristics

Symbol	Parameter	T$_A$ = −40°C to +85°C, R$_L$ = 500Ω						Units
		V$_{CC}$ = 3.3V ± 0.3V, C$_L$ = 50pF		V$_{CC}$ = 2.7V, C$_L$ = 50pF		V$_{CC}$ = 2.5V ± 0.2V, C$_L$ = 30pF		
		Min.	Max.	Min.	Max.	Min.	Max.	
t$_{PHL}$, t$_{PLH}$	Propagation Delay	1.5	6.5	1.5	7.0	1.5	7.8	ns
t$_{OSHL}$, t$_{OSLH}$	Output to Output Skew[3]		1.0					ns

Note:

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t$_{OSHL}$) or LOW-to-HIGH (t$_{OSLH}$).

Dynamic Switching Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25°C$ Typical	Unit
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	3.3	$C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$	0.8	V
		2.5	$C_L = 30pF$, $V_{IH} = 2.5V$, $V_{IL} = 0V$	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	3.3	$C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$	−0.8	V
		2.5	$C_L = 30pF$, $V_{IH} = 2.5V$, $V_{IL} = 0V$	−0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10MHz	25	pF

AC Loading and Waveforms (Generic for LCX Family)

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V
t_{PZH}, t_{PHZ}	GND
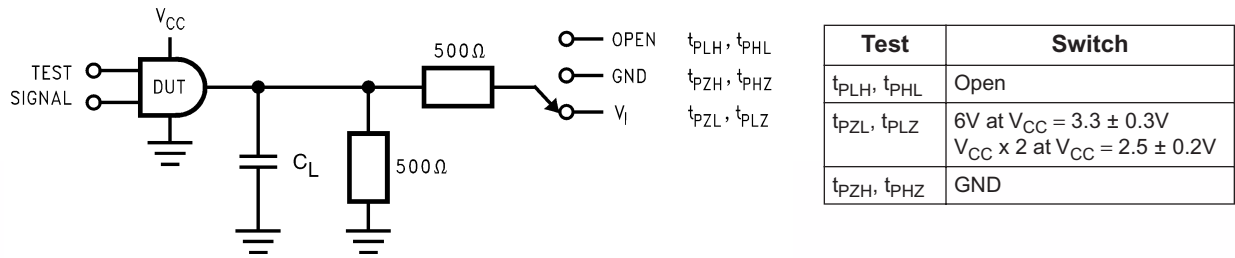
Figure 1. AC Test Circuit (C_L includes probe and jig capacitance)

Waveform for Inverting and Non-Inverting Functions

3-STATE Output Low Enable and Disable Times for Logic

Propagation Delay. Pulse Width and t_{rec} Waveforms

Setup Time, Hold Time and Recovery Time for Logic
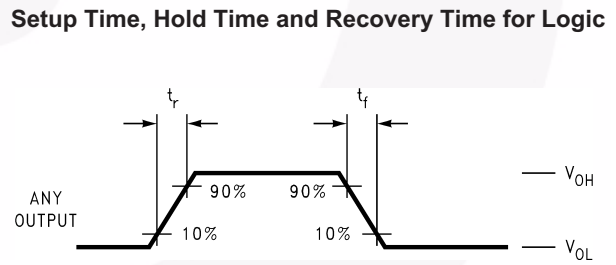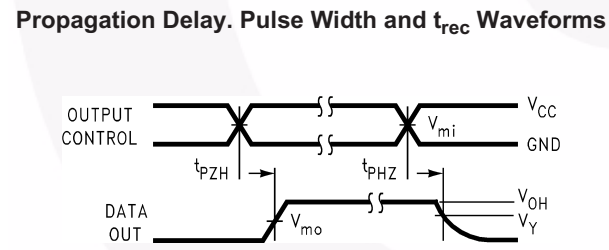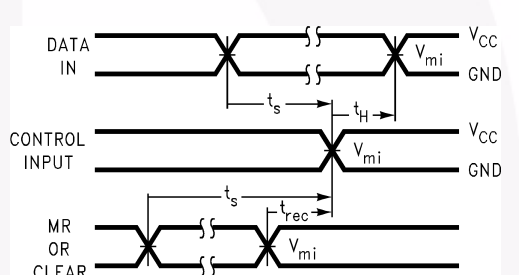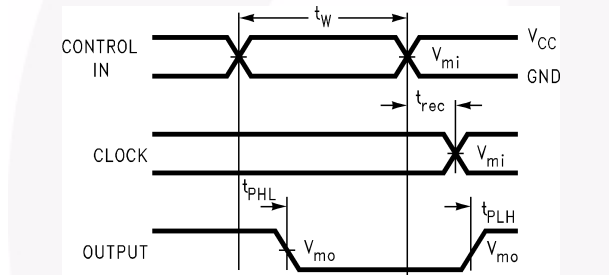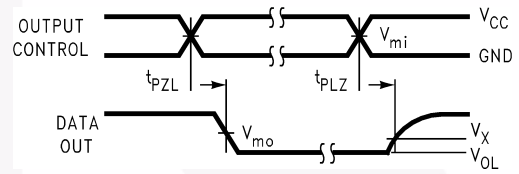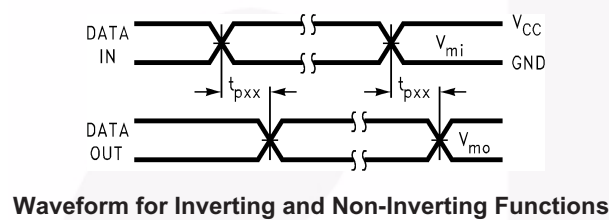
3-STATE Output High Enable and Disable Times for Logic

t_{rise} and t_{fall}

Symbol	V_{CC}		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V

Figure 2. Waveforms (Input Characteristics; f = 1MHz, t_r = t_f = 3ns)
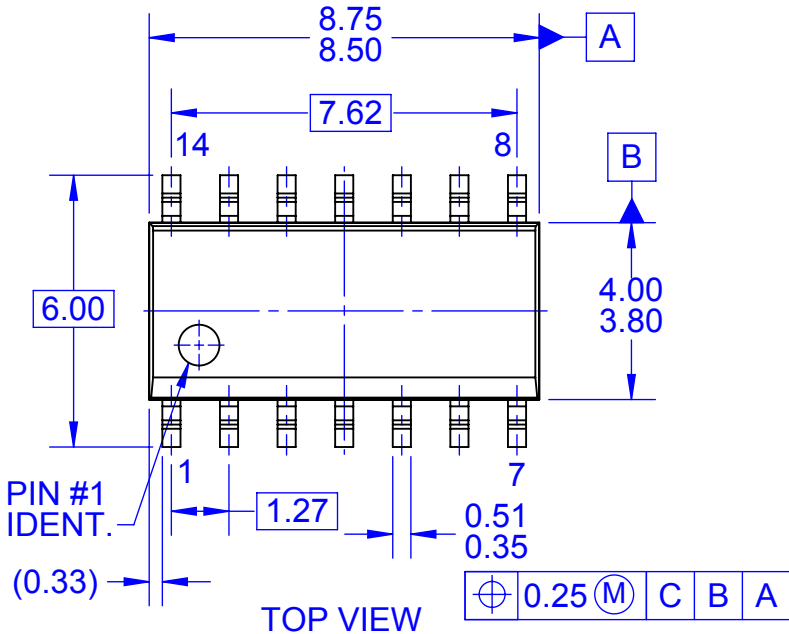
Schematic Diagram (Generic for LCX Family)

5.00±0.10 A

0.43TYP

14   8

B

6.4

4.40±0.10

3.2

PIN#1 IDENT

1   TOP VIEW   7

⌒ 0.2 C B A
ALL LEAD TIPS

0.65

6.10

1.65

0.45

RECOMMENDED LAND PATTERN

1.2 MAX

0.90 +0.15 −0.10

0.10±0.05

ALL LEAD TIPS

⌒ 0.1 C

0.65

0.30
0.19

C

⊕ 0.13Ⓜ A BⓈ CⓈ

FRONT VIEW

SEE DETAIL A

0.20
0.09

12.00° TOP & BOTTOM

0.09 MIN

GAGE PLANE

0°- 8°

0.09 MIN

0.6±0.1

0.25

1.00

SEATING PLANE

DETAIL A
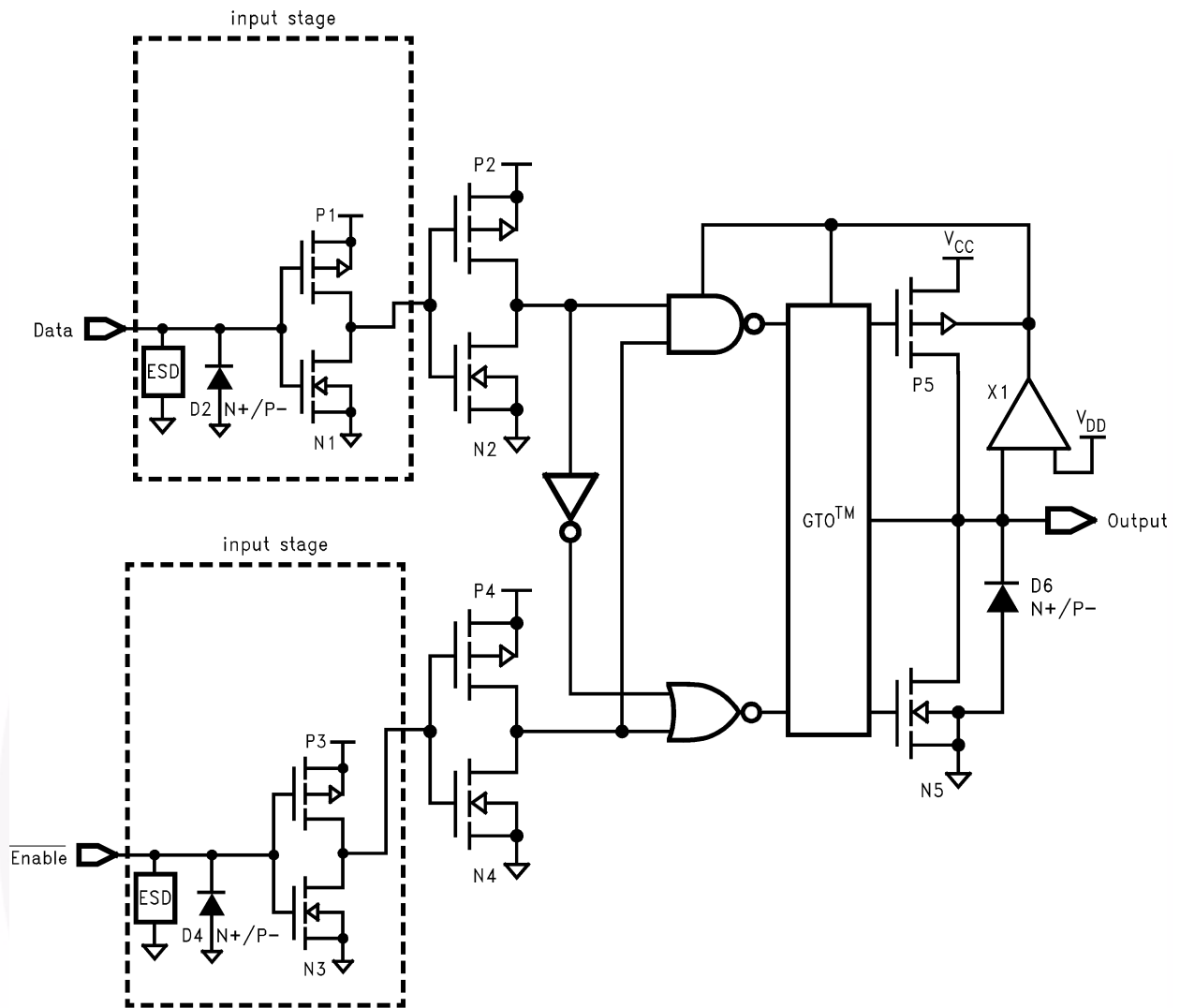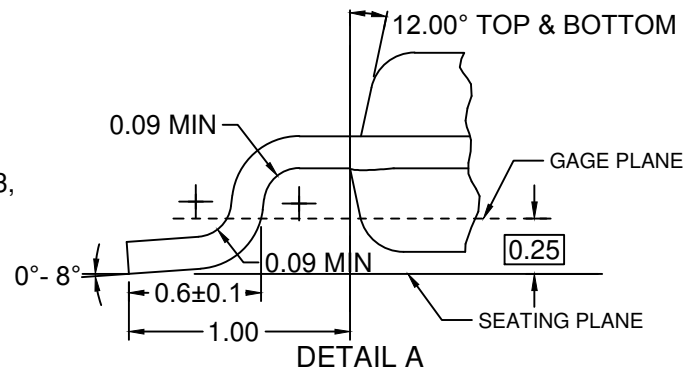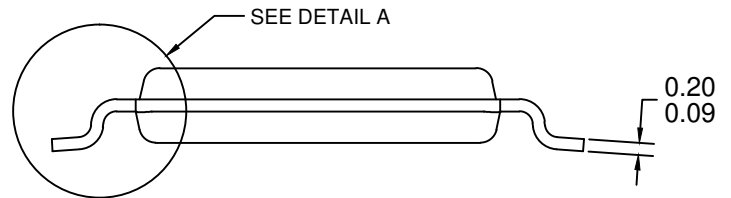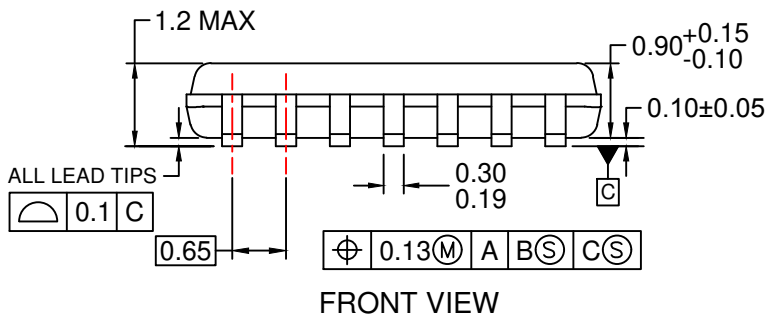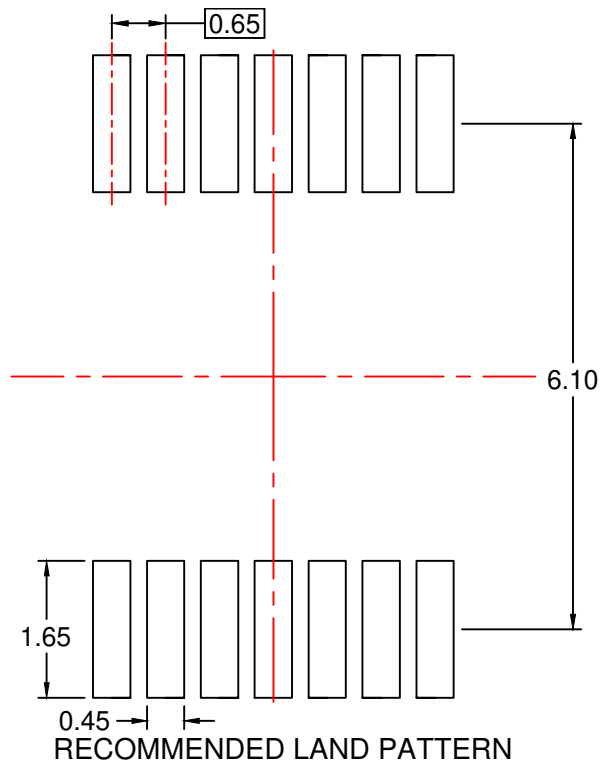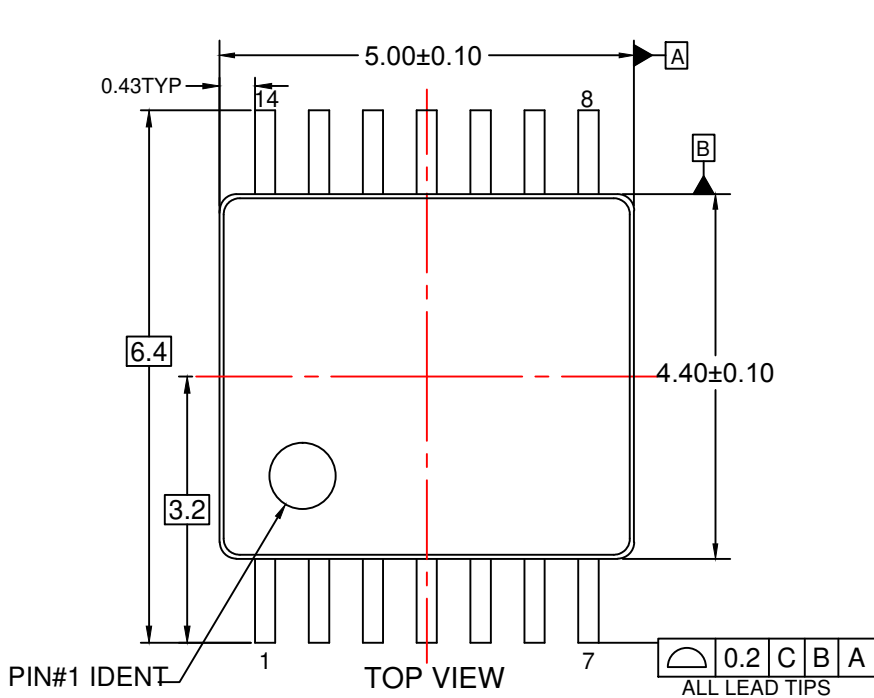
NOTES:
 A. CONFORMS TO JEDEC REGISTRATION MO-153,
    VARIATION AB, REF NOTE 6
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS,
    MOLD FLASH, AND TIE BAR EXTRUSIONS
 D. DIMENSIONING AND TOLERANCES PER ANSI
    Y14.5M, 2009.
 E. LANDPATTERN STANDARD: SOP65P640X110-14M.
 F. DRAWING FILE NAME: MKT-MTC14rev7.

FAIRCHILD.

TOP VIEW

8.75 / 8.50 — A

7.62

14 | 8 — B

6.00

4.00 / 3.80

PIN #1 IDENT.

1 | 7

1.27

0.51 / 0.35

(0.33)

TOP VIEW

⊕ | 0.25 Ⓜ | C | B | A

LAND PATTERN RECOMMENDATION

14 | 0.65 | 8

5.60

1.70

1 | 7

1.27

LAND PATTERN RECOMMENDATION

FRONT VIEW

1.75 MAX

C

1.50 / 1.25

0.25 / 0.10

⌒ | 0.10 | C

FRONT VIEW

SIDE VIEW

A

0.25 / 0.19

SIDE VIEW
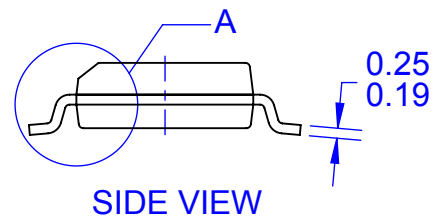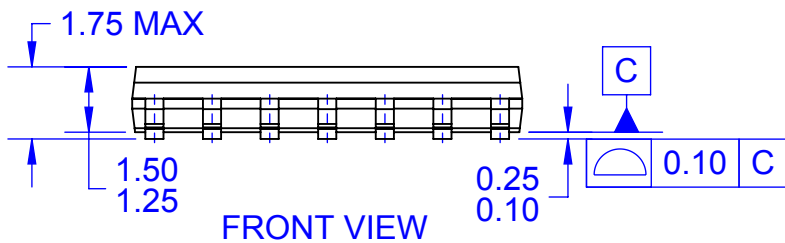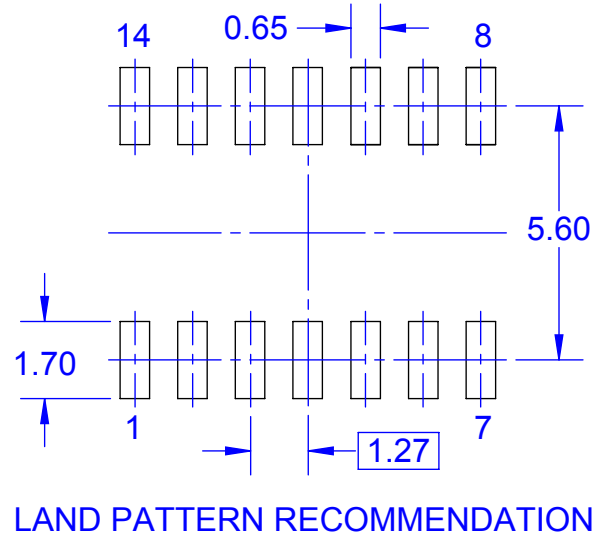
NOTES:

A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145-14M
E. CONFORMS TO ASME Y14.5M, 2009
D. DRAWING FILENAME: MKT-M14Arev14

FAIRCHILD ™

DETAIL A

0.50 / 0.25 x 45°

R0.10

GAGE PLANE

R0.10

0.36

8° / 0°

0.90 / 0.50

(1.04)

SEATING PLANE

DETAIL A
SCALE 16 : 1

PUBLICATION ORDERING INFORMATION
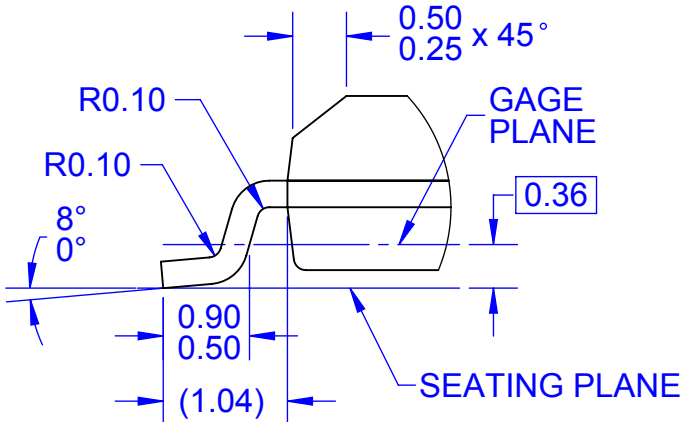
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