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# 74LV138

## 3-to-8 line decoder/demultiplexer; inverting

Rev. 4 — 4 March 2016 Product data sheet

## 1. General description

The 74LV138 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC138 and 74HCT138.

The 74LV138 is a 3-to-8 line decoder/demultiplexer. It accepts three binary weighted address inputs (A0, A1 and A2) and, when enabled, provides eight mutually exclusive active LOW outputs ($\overline{Y}0$ to $\overline{Y}7$).

There are three enable inputs: two active LOW ($\overline{E}1$ and $\overline{E}2$) and one active HIGH (E3). Every output will be HIGH unless $\overline{E}1$ and $\overline{E}2$ are LOW and E3 is HIGH.

This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 74LV138 devices and one inverter. The 74LV138 can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

## 2. Features and benefits

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between $V_{CC}$ = 2.7 V and $V_{CC}$ = 3.6 V
- Typical output ground bounce < 0.8 V at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C
- Typical HIGH-level output voltage ($V_{OH}$) undershoot: > 2 V at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LV138D | −40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74LV138DB | −40 °C to +125 °C | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74LV138PW | −40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74LV138BQ | −40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |

## 4. Functional diagram

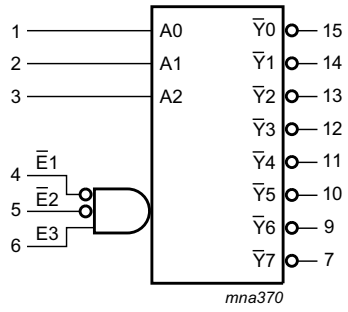



**Fig 1. Logic symbol**

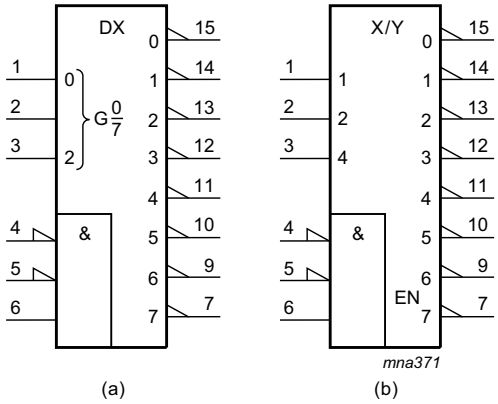



**Fig 2. IEC logic symbol**

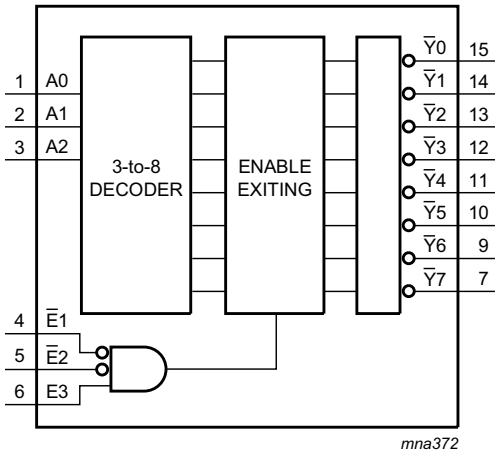



**Fig 3. Functional diagram**

# 5. Pinning information

## 5.1 Pinning

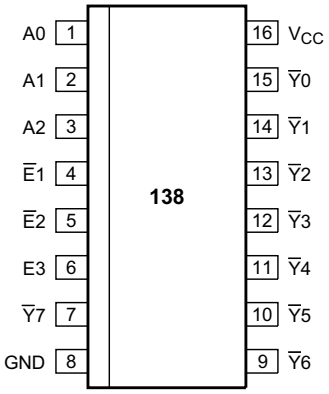
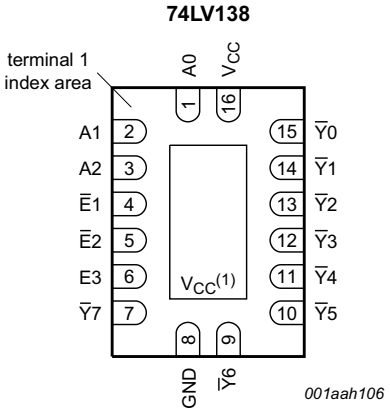



Fig 4. Pin configuration SO16 and (T)SSOP16




Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to $V_{CC}$.

Fig 5. Pin configuration DHVQFN16

## 5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|---|---|---|
| A0 | 1 | address input |
| A1 | 2 | address input |
| A2 | 3 | address input |
| $\overline{E}1$ | 4 | enable input (active LOW) |
| $\overline{E}2$ | 5 | enable input (active LOW) |
| E3 | 6 | enable input (active HIGH) |
| GND | 8 | ground (0 V) |
| $\overline{Y}0$ to $\overline{Y}7$ | 15, 14, 13, 12, 11, 10, 9, 7 | output |
| $V_{CC}$ | 16 | supply voltage |

# 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care*

| Input | | | | | | Output | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{E1}$ | $\overline{E2}$ | E3 | A0 | A1 | A2 | $\overline{Y0}$ | $\overline{Y1}$ | $\overline{Y2}$ | $\overline{Y3}$ | $\overline{Y4}$ | $\overline{Y5}$ | $\overline{Y6}$ | $\overline{Y7}$ |
| H | X | X | X | X | X | H | H | H | H | H | H | H | H |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | L | X | X | X | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | L | H | H | H | H | H | H | H |
| L | L | H | H | L | L | H | L | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | L | H | H | H | H | H |
| L | L | H | H | H | L | H | H | H | L | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | L | H | H | H |
| L | L | H | H | L | H | H | H | H | H | H | L | H | H |
| L | L | H | L | H | H | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | L |

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | −0.5 | +7.0 | V |
| $I_{IK}$ | input clamping current | $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V | [1] | - | ±20 | mA |
| $I_{OK}$ | output clamping current | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V | [1] | - | ±50 | mA |
| $I_O$ | output current | $V_O = -0.5$ V to $(V_{CC} + 0.5$ V) | | - | ±25 | mA |
| $I_{CC}$ | supply current | | | - | 50 | mA |
| $I_{GND}$ | ground current | | | −50 | - | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb} = -40$ °C to +125 °C | | | | |
| | | SO16 package | [2] | - | 500 | mW |
| | | (T)SSOP16 package | [3] | - | 500 | mW |
| | | DHVQFN16 package | [4] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] $P_{tot}$ derates linearly with 8 mW/K above 70 °C.

[3] $P_{tot}$ derates linearly with 5.5 mW/K above 60 °C.

[4] $P_{tot}$ derates linearly with 4.5 mW/K above 60 °C.

# 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage[1] | | 1.0 | 3.3 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | $V_{CC}$ | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | −40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 1.0 V to 2.0 V | - | - | 500 | ns/V |
| | | $V_{CC}$ = 2.0 V to 2.7 V | - | - | 200 | ns/V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | - | 100 | ns/V |
| | | $V_{CC}$ = 3.6 V to 5.5 V | - | - | 50 | ns/V |

[1] The static characteristics are guaranteed from $V_{CC}$ = 1.2 V to $V_{CC}$ = 5.5 V, but LV devices are guaranteed to function down to $V_{CC}$ = 1.0 V (with input levels GND or $V_{CC}$).

# 9. Static characteristics

**Table 6. Static characteristics**

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 1.2 V | 0.9 | - | - | 0.9 | - | V |
| | | $V_{CC}$ = 2.0 V | 1.4 | - | - | 1.4 | - | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $0.7V_{CC}$ | - | - | $0.7V_{CC}$ | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 1.2 V | - | - | 0.3 | - | 0.3 | V |
| | | $V_{CC}$ = 2.0 V | - | - | 0.6 | - | 0.6 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | - | - | $0.3V_{CC}$ | - | $0.3V_{CC}$ | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = −100 µA; $V_{CC}$ = 1.2 V | - | 1.2 | - | - | - | V |
| | | $I_O$ = −100 µA; $V_{CC}$ = 2.0 V | 1.8 | 2.0 | - | 1.8 | - | V |
| | | $I_O$ = −100 µA; $V_{CC}$ = 2.7 V | 2.5 | 2.7 | - | 2.5 | - | V |
| | | $I_O$ = −100 µA; $V_{CC}$ = 3.0 V | 2.8 | 3.0 | - | 2.8 | - | V |
| | | $I_O$ = −100 µA; $V_{CC}$ = 4.5 V | 4.3 | 4.5 | - | 4.3 | - | V |
| | | $I_O$ = −6 mA; $V_{CC}$ = 3.0 V | 2.4 | 2.82 | - | 2.2 | - | V |
| | | $I_O$ = −12 mA; $V_{CC}$ = 4.5 V | 3.6 | 4.2 | - | 3.5 | - | V |

**Table 6. Static characteristics** *…continued*

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = 100 μA; $V_{CC}$ = 1.2 V | - | 0 | - | - | - | V |
| | | $I_O$ = 100 μA; $V_{CC}$ = 2.0 V | - | 0 | 0.2 | - | 0.2 | V |
| | | $I_O$ = 100 μA; $V_{CC}$ = 2.7 V | - | 0 | 0.2 | - | 0.2 | V |
| | | $I_O$ = 100 μA; $V_{CC}$ = 3.0 V | - | 0 | 0.2 | - | 0.2 | V |
| | | $I_O$ = 100 μA; $V_{CC}$ = 4.5 V | - | 0 | 0.2 | - | 0.2 | V |
| | | $I_O$ = 6 mA; $V_{CC}$ = 3.0 V | - | 0.25 | 0.40 | - | 0.50 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 4.5 V | - | 0.35 | 0.55 | - | 0.65 | V |
| $I_I$ | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | 1.0 | - | 1.0 | μA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 20.0 | - | 160 | μA |
| $\Delta I_{CC}$ | additional supply current | per input; $V_I = V_{CC} - 0.6$ V; $V_{CC}$ = 2.7 V to 3.6 V | - | - | 500 | - | 850 | μA |
| $C_I$ | input capacitance | | - | 3.5 | - | - | - | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*GND = 0 V; For test circuit see Figure 8.*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | An to $\overline{Y}$n; see Figure 6 [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | - | 75 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | - | 26 | 44 | - | 55 | ns |
| | | $V_{CC}$ = 2.7 V | - | 19 | 31 | - | 39 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V; $C_L$ = 15 pF [3] | - | 12 | - | - | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V [3] | - | 15 | 26 | - | 32 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 17 | - | 22 | ns |
| | | E3, $\overline{E}$n to $\overline{Y}$n; see Figure 6 and Figure 7 | | | | | | |
| | | $V_{CC}$ = 1.2 V | - | 75 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | - | 26 | 43 | - | 53 | ns |
| | | $V_{CC}$ = 2.7 V | - | 19 | 30 | - | 38 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V; $C_L$ = 15 pF [3] | - | 14 | - | - | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V [3] | - | 15 | 25 | - | 31 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 19 | - | 24 | ns |

**Table 7. Dynamic characteristics** *…continued*

*GND = 0 V; For test circuit see Figure 8.*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $C_{PD}$ | power dissipation capacitance | $C_L$ = 50 pF; $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$ [4] | - | 45 | - | - | - | pF |

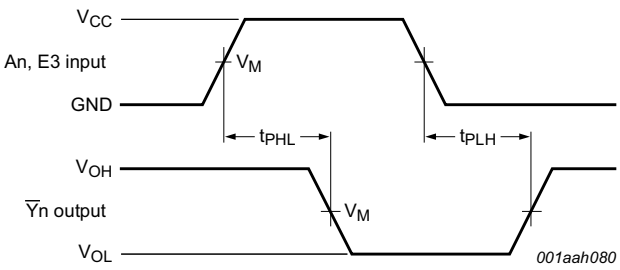
[1] All typical values are measured at $T_{amb}$ = 25 °C.

[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.

[3] Typical values are measured at nominal supply voltage ($V_{CC}$ = 3.3 V).

[4] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz, $f_o$ = output frequency in MHz
$C_L$ = output load capacitance in pF
$V_{CC}$ = supply voltage in V
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

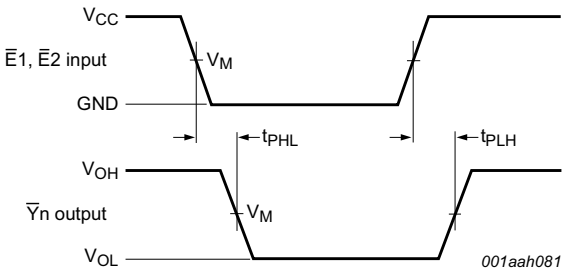
## 11. Waveforms




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 6. The inputs An, E3 to outputs $\overline{Y}$n propagation delays**



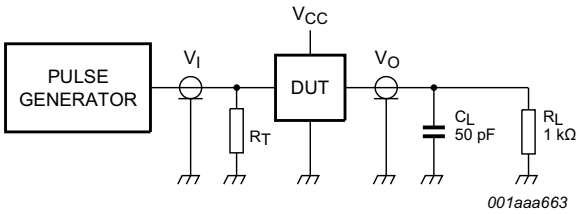

Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 7. The inputs $\overline{E}$n to outputs $\overline{Y}$n propagation delays**

**Table 8. Measurement points**

| Supply voltage | Input | Output |
|---|---|---|
| $V_{CC}$ | $V_M$ | $V_M$ |
| < 2.7 V | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 2.7 V to 3.6 V | 1.5 V | 1.5 V |
| ≥ 4.5 V | $0.5V_{CC}$ | $0.5V_{CC}$ |




Test data is given in Table 9.

Definitions test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

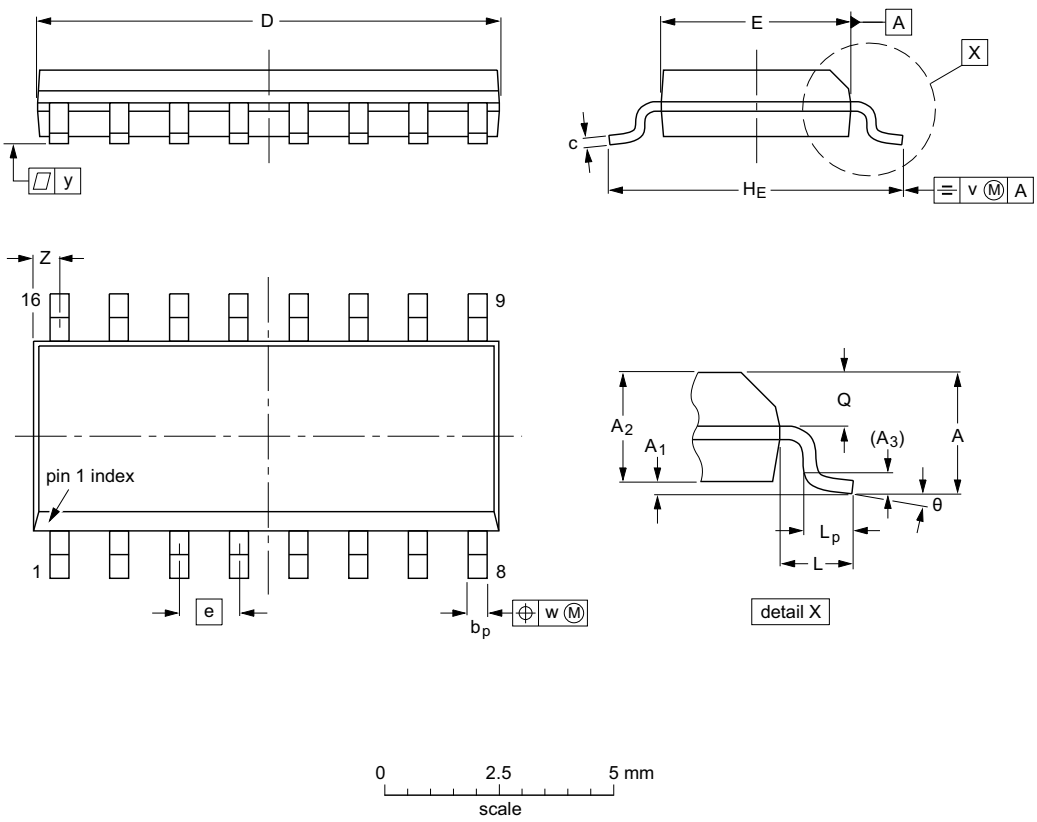
**Fig 8. Test circuit for measuring switching times**

**Table 9. Test data**

| Supply voltage | Input | |
|---|---|---|
| $V_{CC}$ | $V_I$ | $t_r$, $t_f$ |
| < 2.7 V | $V_{CC}$ | ≤ 2.5 ns |
| 2.7 V to 3.6 V | 2.7 V | ≤ 2.5 ns |
| ≥ 4.5 V | $V_{CC}$ | ≤ 2.5 ns |

## 12. Package outline

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

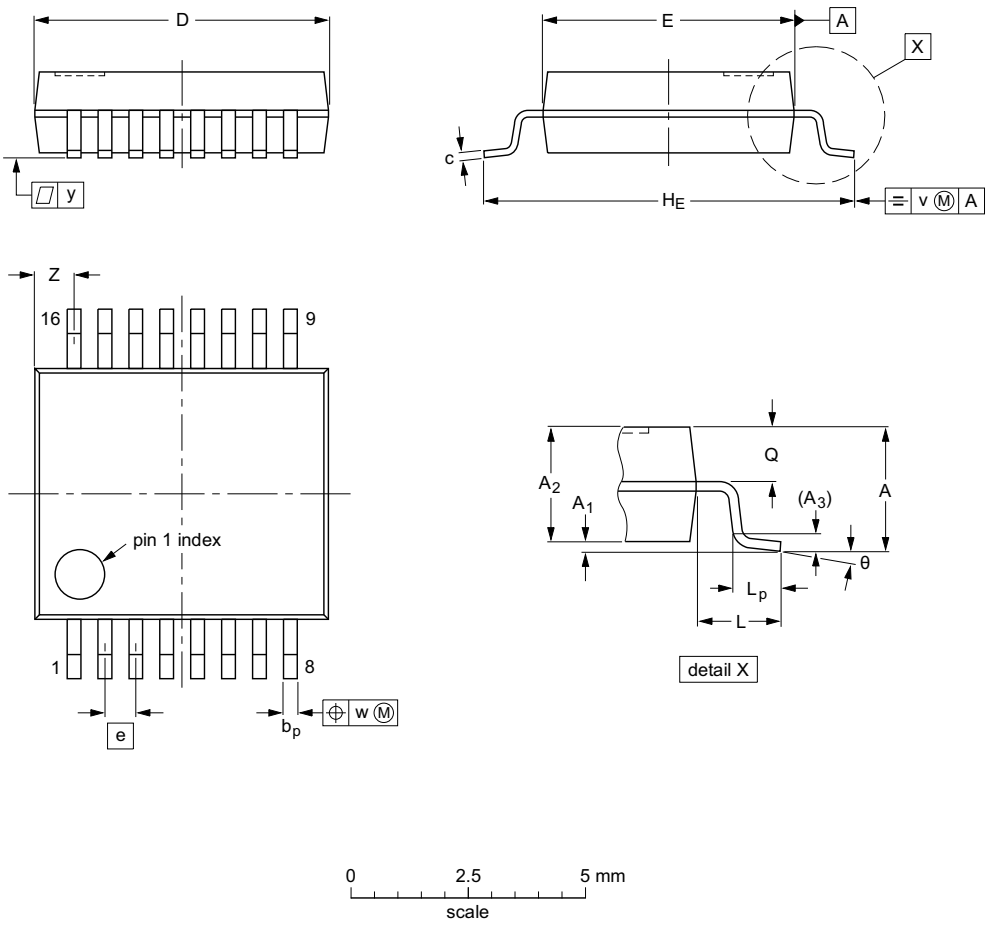
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 9. Package outline SOT109-1 (SO16)**

**SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm** **SOT338-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 6.4<br>6.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 1.00<br>0.55 | 8°<br>0° |

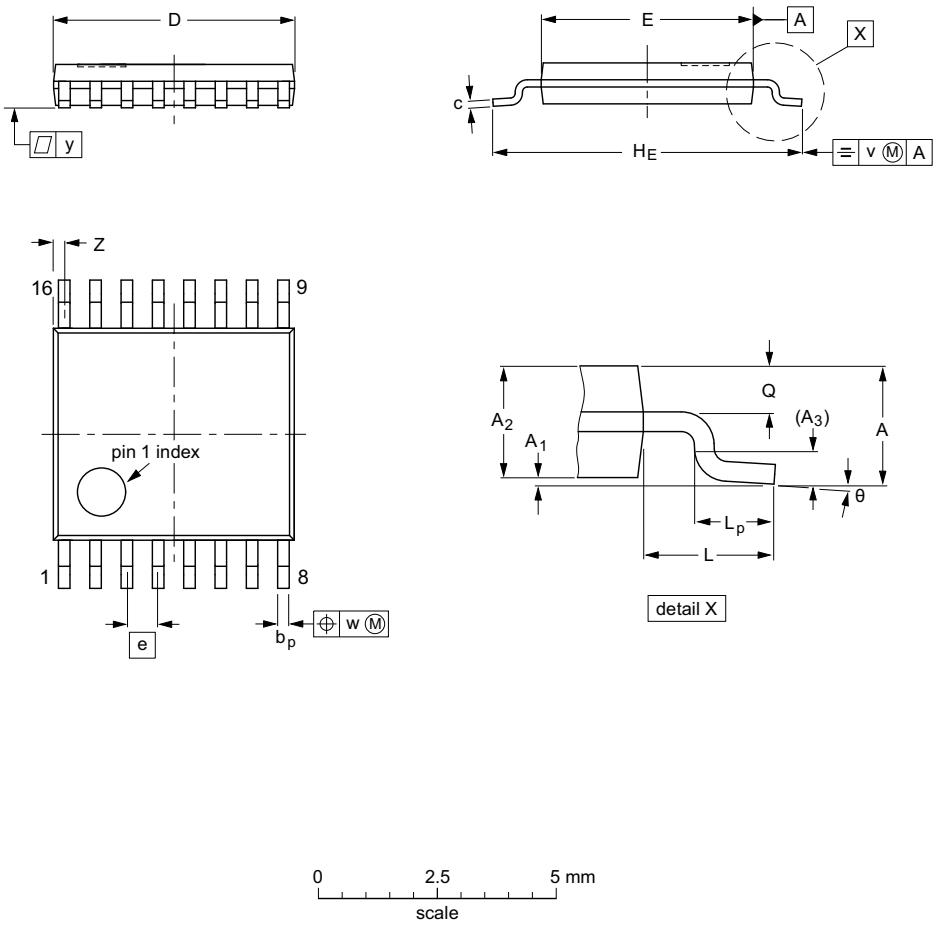
**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT338-1 | | MO-150 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 10. Package outline SOT338-1 (SSOP16)**

**TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm** **SOT403-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.40<br>0.06 | 8°<br>0° |

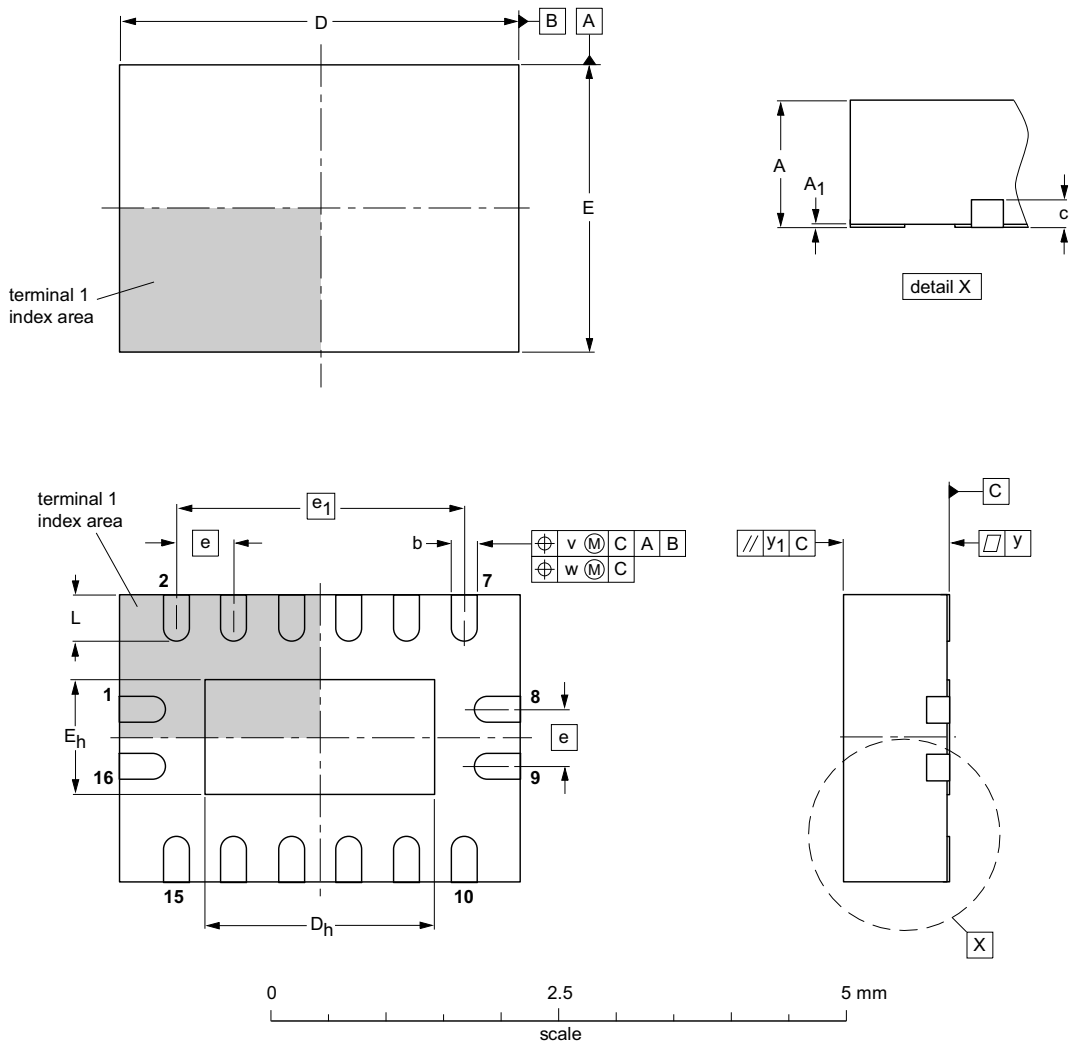
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT403-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 11. Package outline SOT403-1 (TSSOP16)**

**DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm** **SOT763-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | $A^{(1)}$ max. | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 3.6<br>3.4 | 2.15<br>1.85 | 2.6<br>2.4 | 1.15<br>0.85 | 0.5 | 2.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT763-1 | - - - | MO-241 | - - - | | | ~~02-10-17~~<br>03-01-27 |

**Fig 12. Package outline SOT763-1 (DHVQFN16)**

## 13. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LV138 v.4 | 20160304 | Product data sheet | - | 74LV138 v.3 |
| Modifications: | • Type number 74LV138N (SOT38-4) removed. | | | |
| 74LV138 v.3 | 20071115 | Product data sheet | - | 74LV138 v.2 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Section 3: DHVQFN16 package added.<br>• Section 8: derating values added for DHVQFN16 package.<br>• Section 12: outline drawing added for DHVQFN16 package. | | | |
| 74LV138 v.2 | 19980428 | Product specification | - | 74LV138 v.1 |
| 74LV138 v.1 | 19970203 | Product specification | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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## 17. Contents





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**Date of release: 04 March 2016**