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74LV164

8-bit serial-in/parallel-out shift register

Rev. 03 — 4 February 2005 Product data sheet

1. General description

The 74LV164 is a low-voltage, Si-gate CMOS device and is pin and function compatible with the 74HC164 and 74HCT164.

The 74LV164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (DSA or DSB) and either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock input (CP) and enters into Q0, which is the logical AND-function of the two data inputs (DSA and DSB) that existed one set-up time prior to the rising clock edge.

A LOW on the master reset input (MR) overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

2. Features

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low-voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce): < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Typical V_{OHV} (output V_{OH} undershoot): > 2 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Gated serial data inputs
- Asynchronous master reset
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +80 °C and from –40 °C to +125 °C.

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay	V_{CC} = 3.3 V; C_L = 15 pF				
	CP to Qn		-	12	-	ns
	$\overline{MR}$ to Qn		-	12	-	ns

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Table 1: Quick reference data *...continued*

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{max}	maximum clock frequency	V_{CC} = 3.3 V; C_L = 15 pF		-	78	-	MHz
C_I	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V	[1] [2]	-	40	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV164N	–40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74LV164D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV164DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LV164PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LV164BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

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5. Functional diagram

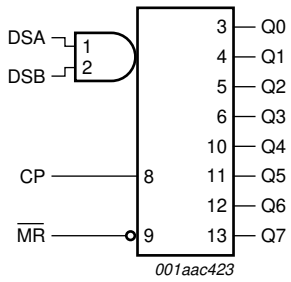

Fig 1. Logic symbol

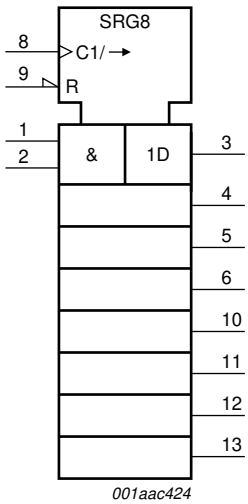

Fig 2. IEC logic symbol

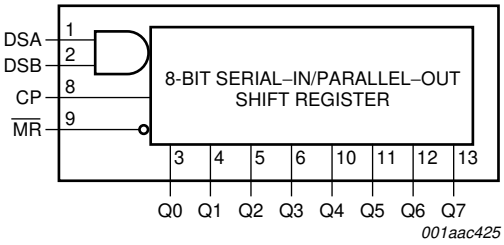

Fig 3. Functional diagram

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6. Pinning information

6.1 Pinning

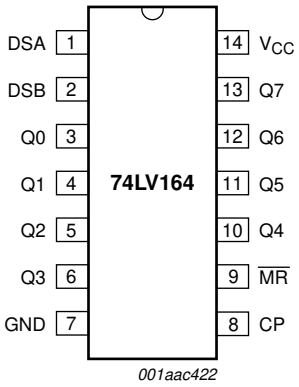
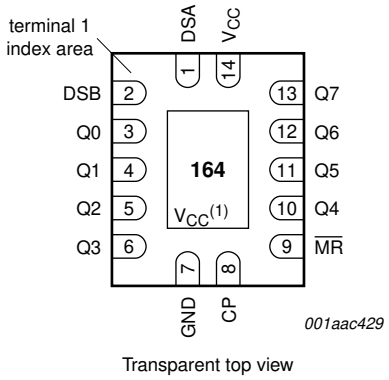


Fig 4. Pin configuration DIP14, SO14, SSOP14 and TSSOP14



Transparent top view

(1) The die substrate is attached to the exposed die pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 5. Pin configuration DHVQFN14

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
DSA	1	data input SA
DSB	2	data input SB
Q0	3	output 0
Q1	4	output 1
Q2	5	output 2
Q3	6	output 3
GND	7	ground (0 V)
CP	8	clock input (edge triggered LOW-to-HIGH)
$\overline{MR}$	9	master reset input (active LOW)
Q4	10	output 4
Q5	11	output 5
Q6	12	output 6
Q7	13	output 7
V_{CC}	14	supply voltage

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7. Functional description

7.1 Function table

Table 4: Function table [1]

Operating mode	Input				Output	
	$\overline{MR}$	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
	H	↑	l	h	L	q0 to q6
	H	↑	h	l	L	q0 to q6
	H	↑	h	h	H	q0 to q6

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH clock transition;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
q = lower case letter indicates the state of referenced input one set-up time prior to the LOW-to-HIGH CP transition.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±50	mA
I_O	output source or sink current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	[1]	-	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C				
	DIP14 package		[2]	-	750	mW
	SO14, (T)SSOP14 and DHVQFN14 packages		[3]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] DIP14 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
(T)SSOP14 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
DHVQFN14 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

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9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage		[1]	1.0	3.3	5.5	V
V_I	input voltage			0	-	V_{CC}	V
V_O	output voltage			0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air		−40	-	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.0 V to 2.0 V		-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V		-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V		-	-	100	ns/V
		V_{CC} = 3.6 V to 5.5 V		-	-	50	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	V
		V_{CC} = 2.0 V	1.4	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −100 µA; V_{CC} = 1.2 V	-	1.2	-	V
		I_O = −100 µA; V_{CC} = 2.0 V	1.8	2.0	-	V
		I_O = −100 µA; V_{CC} = 2.7 V	2.5	2.7	-	V
		I_O = −100 µA; V_{CC} = 3.0 V	2.8	3.0	-	V
		I_O = −6 mA; V_{CC} = 3.0 V	2.40	2.82	-	V
		I_O = −100 µA; V_{CC} = 4.5 V	4.3	4.5	-	V
		I_O = −12 mA; V_{CC} = 4.5 V	3.60	4.20	-	V

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Table 7: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 µA; V_{CC} = 1.2 V	-	0	-	V
		I_O = 100 µA; V_{CC} = 2.0 V	-	0	0.2	V
		I_O = 100 µA; V_{CC} = 2.7 V	-	0	0.2	V
		I_O = 100 µA; V_{CC} = 3.0 V	-	0	0.2	V
		I_O = 6 mA; V_{CC} = 3.0 V	-	0.25	0.40	V
		I_O = 100 µA; V_{CC} = 4.5 V	-	0	0.2	V
		I_O = 12 mA; V_{CC} = 4.5 V	-	0.35	0.55	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	20.0	µA
ΔI_{CC}	additional quiescent supply current per input	$V_I = V_{CC}$ – 0.6 V; V_{CC} = 2.7 V to 3.6 V	-	-	500	µA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	V
		V_{CC} = 2.0 V	1.4	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –100 µA; V_{CC} = 1.2 V	-	-	-	V
		I_O = –100 µA; V_{CC} = 2.0 V	1.8	-	-	V
		I_O = –100 µA; V_{CC} = 2.7 V	2.5	-	-	V
		I_O = –100 µA; V_{CC} = 3.0 V	2.8	-	-	V
		I_O = –6 mA; V_{CC} = 3.0 V	2.20	-	-	V
		I_O = –100 µA; V_{CC} = 4.5 V	4.3	-	-	V
		I_O = –12 mA; V_{CC} = 4.5 V	3.50	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 µA; V_{CC} = 1.2 V	-	-	-	V
		I_O = 100 µA; V_{CC} = 2.0 V	-	-	0.2	V
		I_O = 100 µA; V_{CC} = 2.7 V	-	-	0.2	V
		I_O = 100 µA; V_{CC} = 3.0 V	-	-	0.2	V
		I_O = 6 mA; V_{CC} = 3.0 V	-	-	0.50	V
		I_O = 100 µA; V_{CC} = 4.5 V	-	-	0.2	V
		I_O = 12 mA; V_{CC} = 4.5 V	-	-	0.65	V

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Table 7: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	160	µA
ΔI_{CC}	additional quiescent supply current per input	$V_I = V_{CC}$ – 0.6 V; V_{CC} = 2.7 V to 3.6 V	-	-	850	µA

[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF; R_L = 1 kΩ; for test circuit see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]						
t_{PHL}, t_{PLH}	propagation delay CP to Qn	see Figure 6				
		V_{CC} = 1.2 V	-	75	-	ns
		V_{CC} = 2.0 V	-	26	39	ns
		V_{CC} = 2.7 V	-	19	29	ns
		V_{CC} = 3.0 V to 3.6 V	-	14	23	ns
		V_{CC} = 4.5 V to 5.5 V	-	12	19	ns
		V_{CC} = 3.3 V; C_L = 15 pF	-	12	-	ns
t_{PHL}	propagation delay $\overline{MR}$ to Qn	see Figure 7				
		V_{CC} = 1.2 V	-	75	-	ns
		V_{CC} = 2.0 V	-	26	39	ns
		V_{CC} = 2.7 V	-	19	29	ns
		V_{CC} = 3.0 V to 3.6 V	-	14	23	ns
		V_{CC} = 4.5 V to 5.5 V	-	12	19	ns
		V_{CC} = 3.3 V; C_L = 15 pF	-	12	-	ns
t_W	pulse width CP	see Figure 6				
		V_{CC} = 2.0 V	34	9	-	ns
		V_{CC} = 2.7 V	25	6	-	ns
		V_{CC} = 3.0 V to 3.6 V	20	5	-	ns
		V_{CC} = 4.5 V to 5.5 V	13	4	-	ns
t_W	pulse width $\overline{MR}$	see Figure 7				
		V_{CC} = 2.0 V	34	10	-	ns
		V_{CC} = 2.7 V	25	8	-	ns
		V_{CC} = 3.0 V to 3.6 V	20	6	-	ns
		V_{CC} = 4.5 V to 5.5 V	13	5	-	ns

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Table 8: Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 1$ kΩ; for test circuit see Figure 9.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{rem}	removal time $\overline{MR}$ to CP	see Figure 7					
		V_{CC} = 1.2 V		-	30	-	ns
		V_{CC} = 2.0 V		19	10	-	ns
		V_{CC} = 2.7 V		14	8	-	ns
		V_{CC} = 3.0 V to 3.6 V		11	6	-	ns
		V_{CC} = 4.5 V to 5.5 V		8	5	-	ns
t_{su}	set-up time Dn to CP	see Figure 8					
		V_{CC} = 1.2 V		-	15	-	ns
		V_{CC} = 2.0 V		22	5	-	ns
		V_{CC} = 2.7 V		16	4	-	ns
		V_{CC} = 3.0 V to 3.6 V		13	3	-	ns
		V_{CC} = 4.5 V to 5.5 V		9	2	-	ns
t_h	hold time Dn to CP	see Figure 8					
		V_{CC} = 1.2 V		-	–10	-	ns
		V_{CC} = 2.0 V		5	–3	-	ns
		V_{CC} = 2.7 V		5	–2	-	ns
		V_{CC} = 3.0 V to 3.6 V		5	–2	-	ns
		V_{CC} = 4.5 V to 5.5 V		5	–1	-	ns
f_{max}	maximum clock frequency	see Figure 6					
		V_{CC} = 2.0 V		14	40	-	MHz
		V_{CC} = 2.7 V		19	58	-	MHz
		V_{CC} = 3.0 V to 3.6 V		24	70	-	MHz
		V_{CC} = 4.5 V to 5.5 V		36	100	-	MHz
		V_{CC} = 3.3 V; C_L = 15 pF		-	78	-	MHz
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V	[2] [3]	-	40	-	pF
T_{amb} = –40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay CP to Qn	see Figure 6					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.0 V		-	-	49	ns
		V_{CC} = 2.7 V		-	-	36	ns
		V_{CC} = 3.0 V to 3.6 V		-	-	29	ns
		V_{CC} = 4.5 V to 5.5 V		-	-	24	ns
t_{PHL}	propagation delay $\overline{MR}$ to Qn	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.0 V		-	-	49	ns
		V_{CC} = 2.7 V		-	-	36	ns
		V_{CC} = 3.0 V to 3.6 V		-	-	29	ns
		V_{CC} = 4.5 V to 5.5 V		-	-	24	ns

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Table 8: Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 1$ kΩ; for test circuit see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_W	pulse width CP	see Figure 6				
		V_{CC} = 2.0 V	41	-	-	ns
		V_{CC} = 2.7 V	30	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	24	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	16	-	-	ns
t_W	pulse width $\overline{MR}$	see Figure 7				
		V_{CC} = 2.0 V	41	-	-	ns
		V_{CC} = 2.7 V	30	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	24	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	16	-	-	ns
t_{rem}	removal time $\overline{MR}$ to CP	see Figure 7				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.0 V	24	-	-	ns
		V_{CC} = 2.7 V	18	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	14	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	10	-	-	ns
t_{su}	set-up time Dn to CP	see Figure 8				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.0 V	26	-	-	ns
		V_{CC} = 2.7 V	19	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	15	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	10	-	-	ns
t_h	hold time Dn to CP	see Figure 8				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.0 V	5	-	-	ns
		V_{CC} = 2.7 V	5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	5	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5	-	-	ns
f_{max}	maximum clock frequency	see Figure 6				
		V_{CC} = 2.0 V	12	-	-	MHz
		V_{CC} = 2.7 V	16	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V	20	-	-	MHz
		V_{CC} = 4.5 V to 5.5 V	30	-	-	MHz

[1] Typical values are measured at nominal V_{CC} and T_{amb} = 25 °C.

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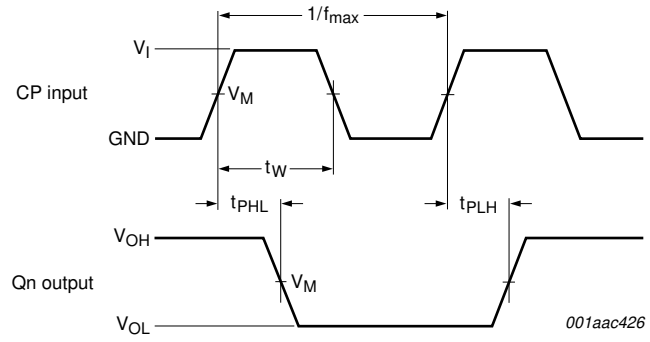
[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[3] The condition is V_I = GND to V_{CC}.

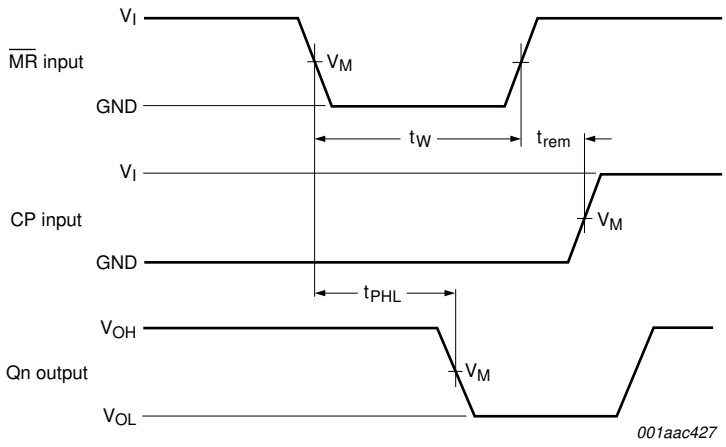
12. Waveforms



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 6. Propagation delay clock (CP) to output (Qn), clock pulse width and maximum clock frequency



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 7. Pulse width master reset ($\overline{MR}$), propagation delay master reset ($\overline{MR}$) to output (Qn) and removal time master reset ($\overline{MR}$) to clock (CP)

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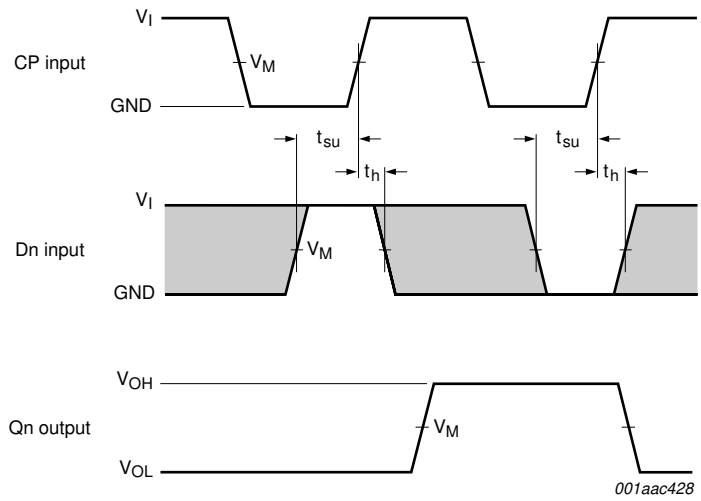

Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 8. Data set-up and hold times inputs (Dn) to clock (CP)

Table 9: Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.0 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

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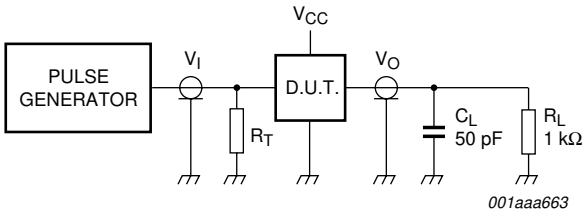

Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 9. Load circuitry for switching times

Table 10: Test data

Supply voltage	Input		Load		Test
V_{CC}	V_I	t_r , t_f	C_L	R_L	
1.2 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}
2.0 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF, 15 pF	1 kΩ	t_{PHL}, t_{PLH}
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}

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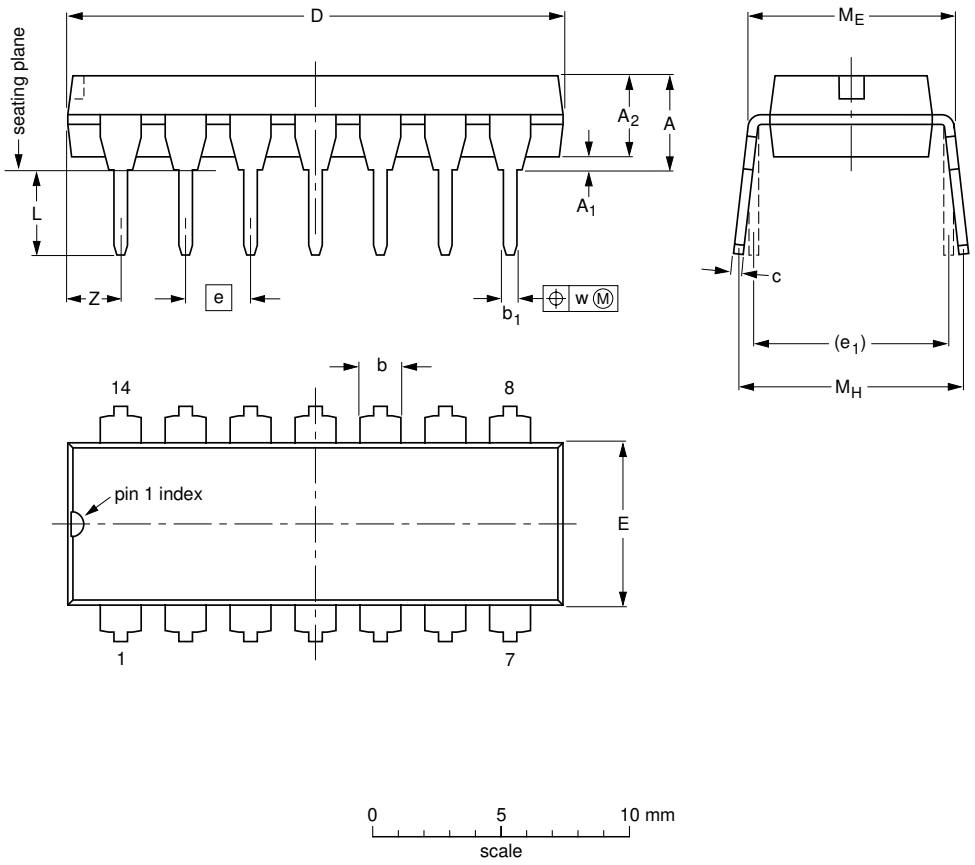
13. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 10. Package outline SOT27-1 (DIP14)

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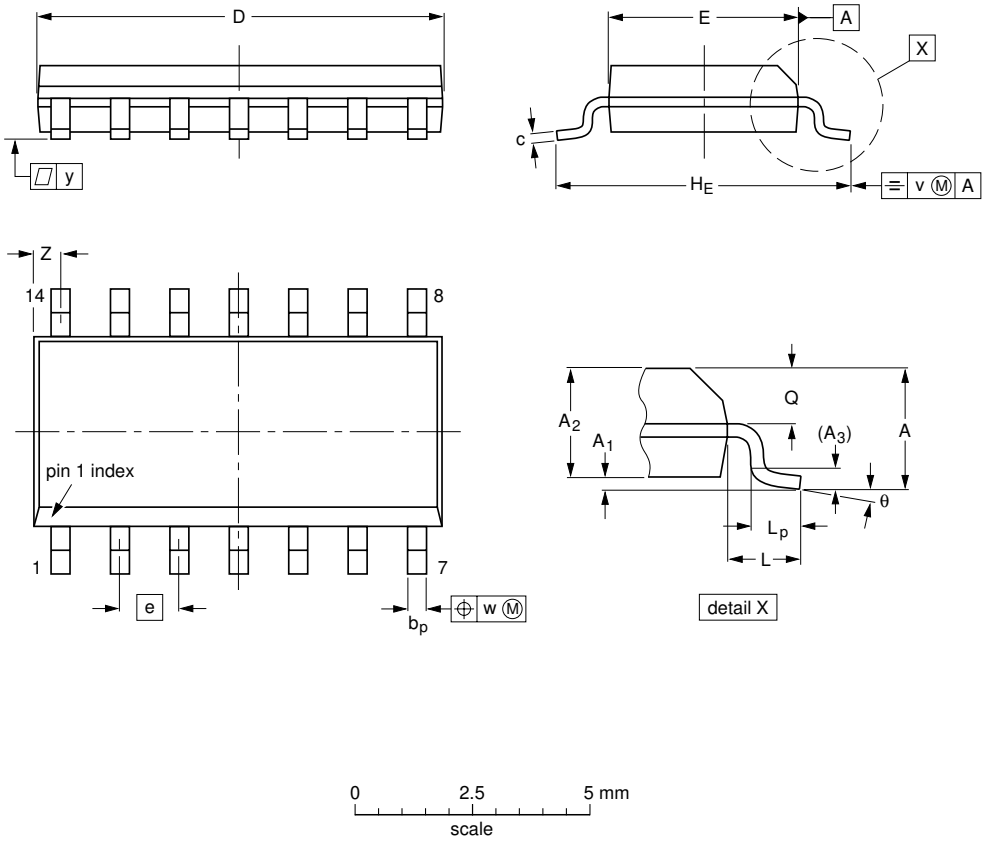
SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT108-1 (SO14)

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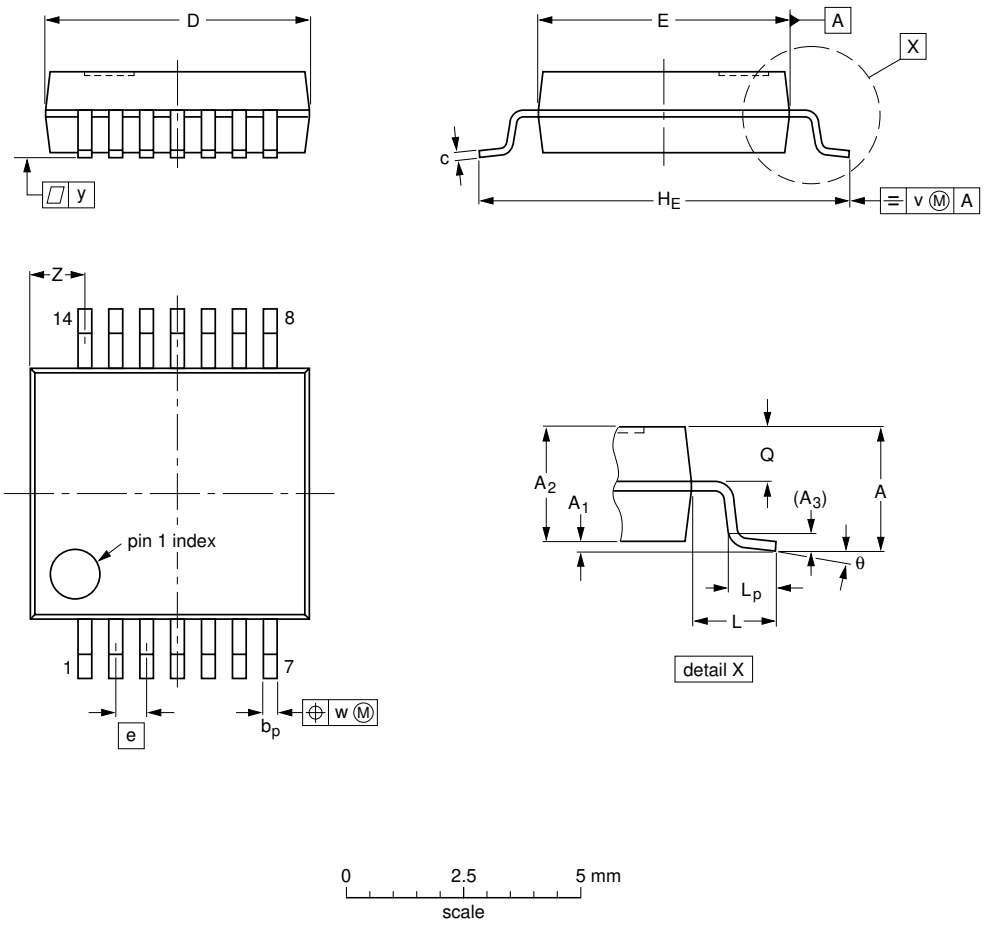
SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT337-1 (SSOP14)

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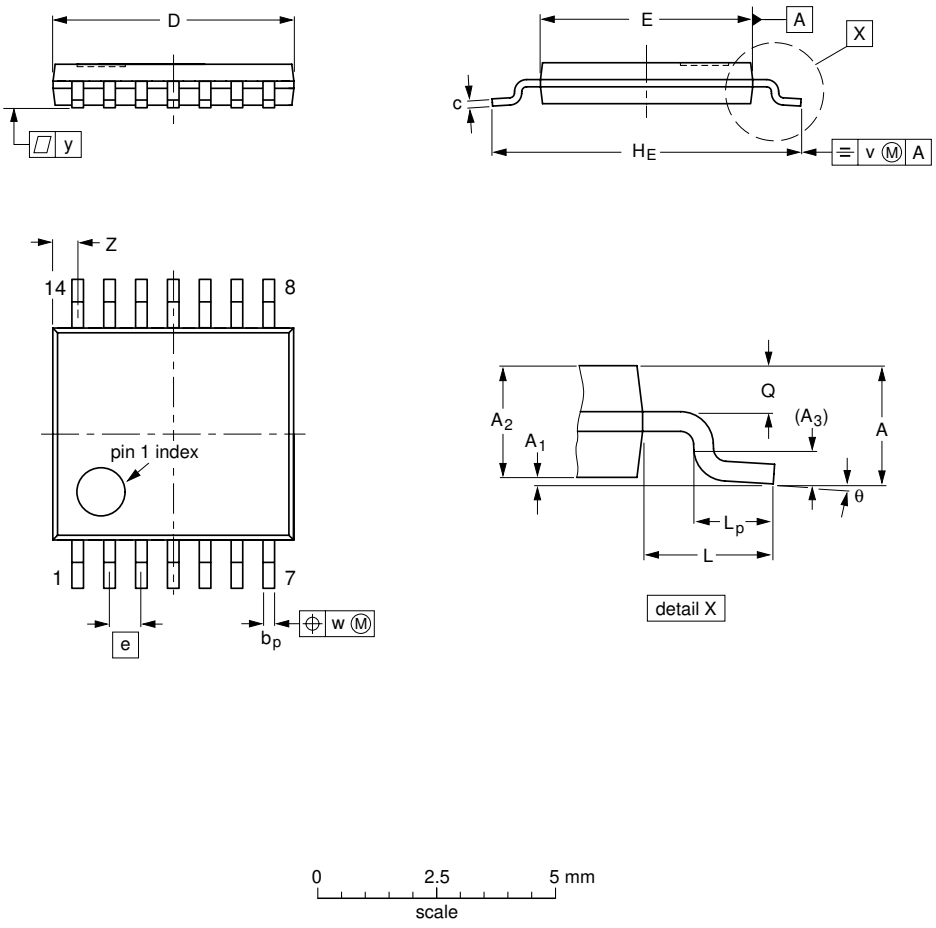
TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 13. Package outline SOT402-1 (TSSOP14)

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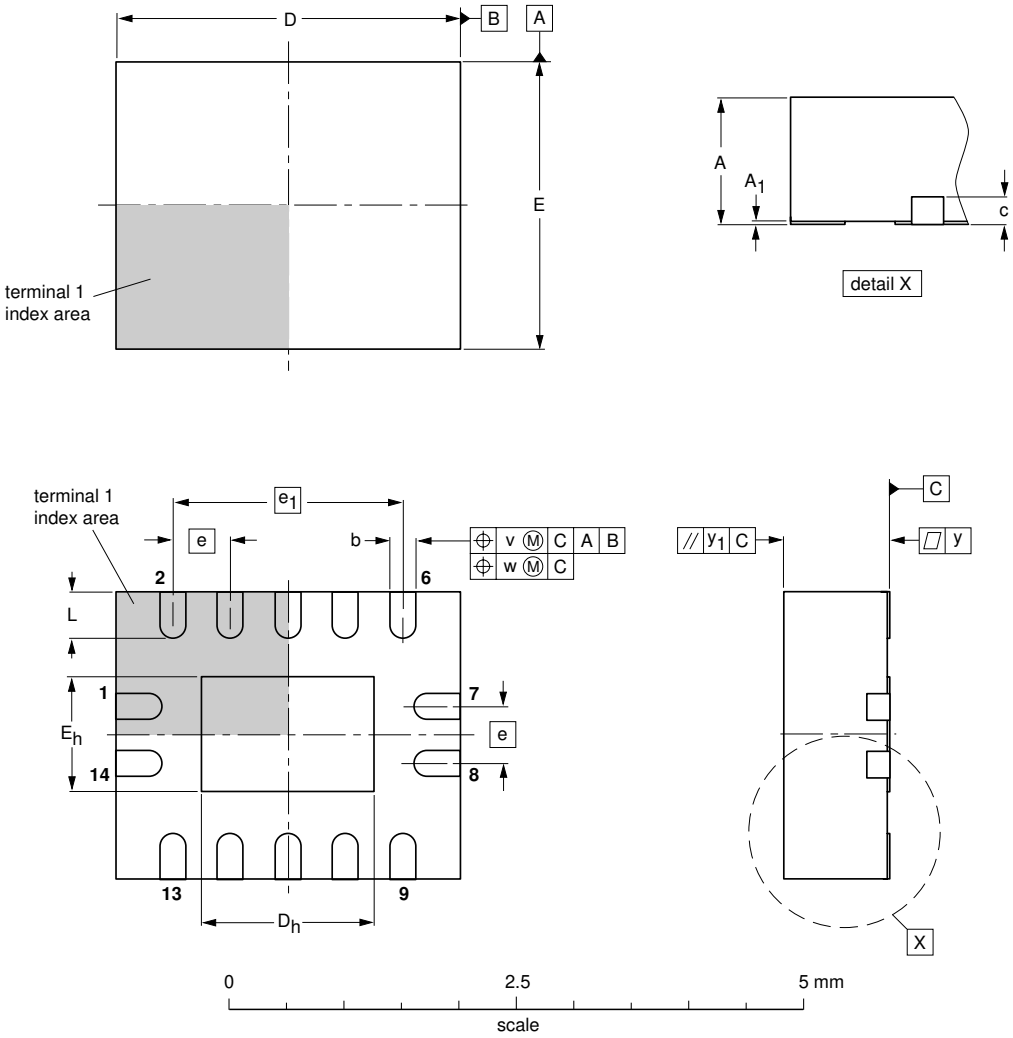
DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 14. Package outline SOT762-1 (DHVQFN14)

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14. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LV164_3	20050204	Product data sheet	-	9397 750 14501	74LV164_2
Modifications:	• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors • Added: type number 74LV164BQ (DHVQFN14 package).				
74LV164_2	19980507	Product specification	-	9397 750 04431	74LV164_1
74LV164_1	19970328	Product specification		-	-

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15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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19. Contents

1	**General description**	**1**
2	**Features**	**1**
3	**Quick reference data**	**1**
4	**Ordering information**	**2**
5	**Functional diagram**	**3**
6	**Pinning information**	**4**
6.1	Pinning	4
6.2	Pin description	4
7	**Functional description**	**5**
7.1	Function table	5
8	**Limiting values**	**5**
9	**Recommended operating conditions**	**6**
10	**Static characteristics**	**6**
11	**Dynamic characteristics**	**8**
12	**Waveforms**	**11**
13	**Package outline**	**14**
14	**Revision history**	**19**
15	**Data sheet status**	**20**
16	**Definitions**	**20**
17	**Disclaimers**	**20**
18	**Contact information**	**20**

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