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74LV4094

8-stage shift-and-store bus register

Rev. 4 — 19 December 2011 Product data sheet

1. General description

The 74LV4094 is a low voltage Si-gate CMOS device and is pin and functional compatible with 74HC4094; 74HCT4094.

The 74LV4094 is an 8-stage serial shift register. It has a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs QP0 to QP7. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the outputs whenever the output enable (OE) signal is HIGH.

Two serial outputs (QS1 and QS2) are available for cascading a number of 74LV4094 devices. Serial data is available at QS1 on positive-going clock edges to allow high-speed operation in cascaded systems with a fast clock rise time. The same serial data is available at QS2 on the next negative going clock edge. This is used for cascading 74LV4094 devices when the clock has a slow rise time.

2. Features and benefits

- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical output ground bounce < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Typical HIGH-level output voltage (V_{OH}) undershoot: > 2 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

3. Applications

- Serial-to-parallel data conversion
- Remote control holding register

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV4094N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74LV4094D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV4094DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LV4094PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram

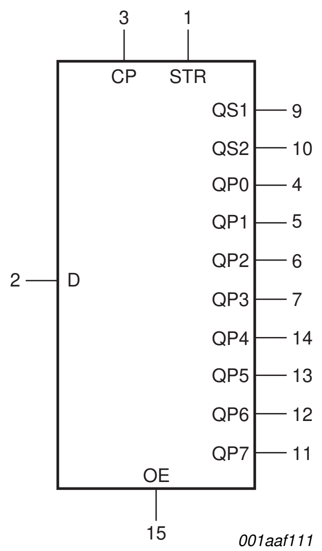


Fig 1. Functional diagram

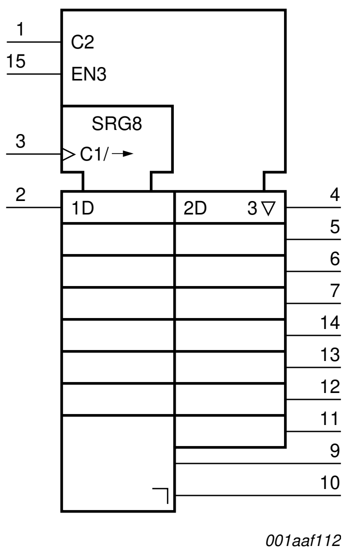


Fig 2. Logic symbol

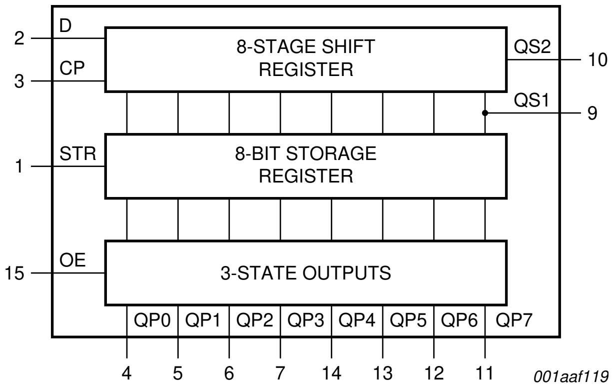


Fig 3. Logic diagram

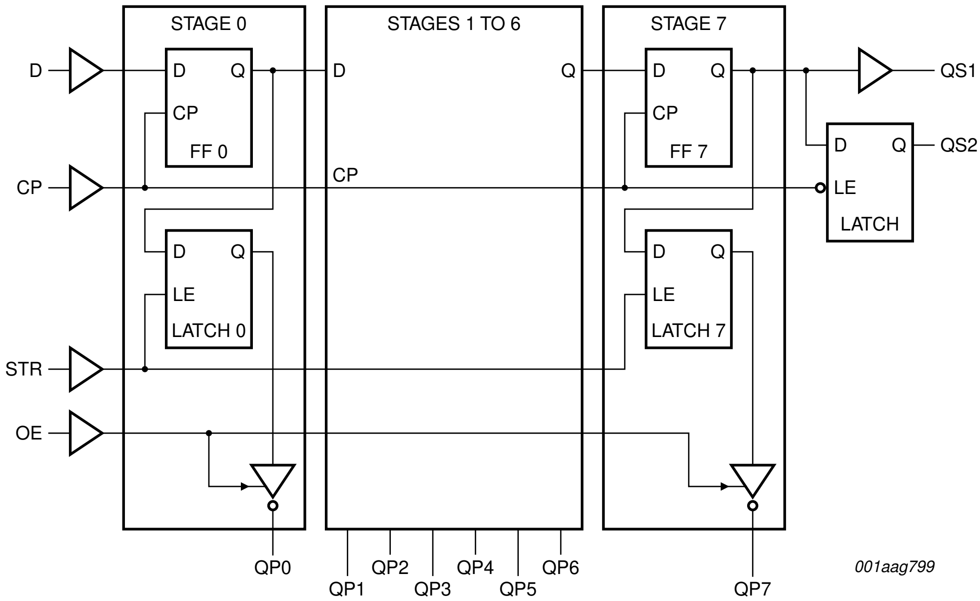


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning

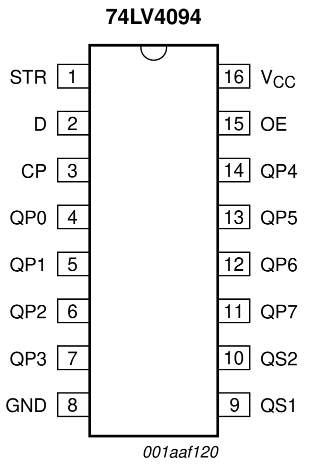


Fig 5. Pin configuration DIP16 and SO16

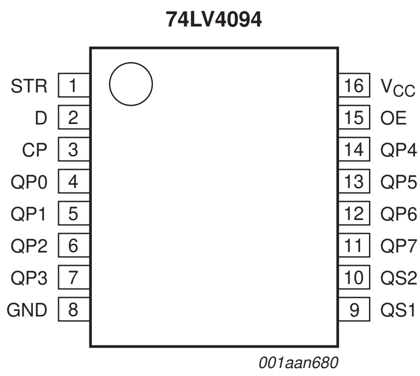


Fig 6. Pin configuration SSOP16 and TSSOP16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
STR	1	strobe input
D	2	data input
CP	3	clock input
QP0 to QP7	4, 5, 6, 7, 14, 13, 12, 11	parallel output
V_{SS}	8	ground supply voltage
QS1, QS2	9,10	serial output
OE	15	output enable input
V_{DD}	16	supply voltage

7. Functional description

Table 3. Function table[1]

Inputs				Parallel outputs		Serial outputs	
CP	**OE**	**STR**	**D**	**QP0**	**QPn**	**QS1**	**QS2**
↑	L	X	X	Z	Z	Q6S	NC
↓	L	X	X	Z	Z	NC	Q7S
↑	H	L	X	NC	NC	Q6S	NC
↑	H	H	L	L	QPn −1	Q6S	NC
↑	H	H	H	H	QPn −1	Q6S	NC
↓	H	H	H	NC	NC	NC	Q7S

[1] At the positive clock edge, the information in the 7th register stage is transferred to the 8th register stage and the QSn outputs.
H = HIGH voltage level; L = LOW voltage level; X = don’t care;
↑ = positive-going transition; ↓ = negative-going transition;
Z = HIGH-impedance OFF-state; NC = no change;
Q6S = the data in register stage 6 before the LOW to HIGH clock transition;
Q7S = the data in register stage 7 before the HIGH to LOW clock transition.

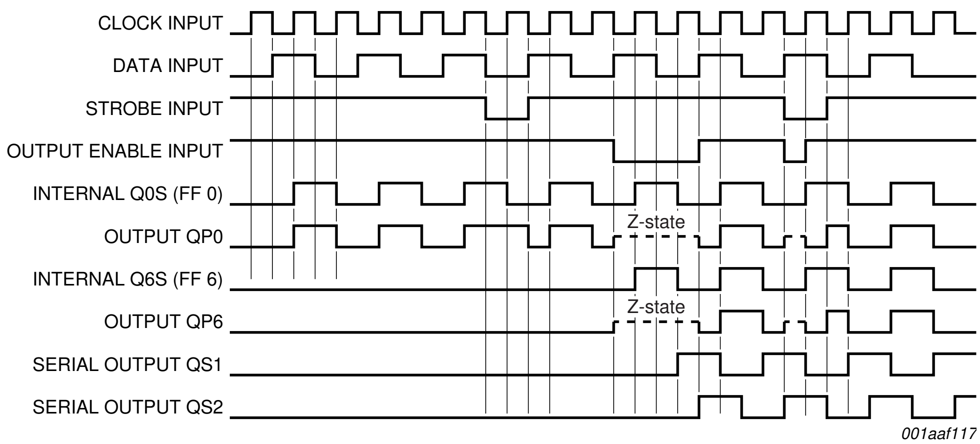


Fig 7. Timing diagram

8. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±50	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)		-	±25	mA
I_{CC}	supply current			-	+50	mA
I_{GND}	ground current			–50	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C				
	DIP16 package		[1]	-	750	mW
	SO16 package		[2]	-	500	mW
	(T)SSOP16 package		[3]	-	500	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage		[1]	1.0	3.3	3.6	V
V_I	input voltage			0	-	V_{CC}	V
V_O	output voltage			0	-	V_{CC}	V
T_{amb}	ambient temperature			–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0$ V to 2.0 V		-	-	500	ns/V
		$V_{CC} = 2.0$ V to 2.7 V		-	-	200	ns/V
		$V_{CC} = 2.7$ V to 3.6 V		-	-	100	ns/V

[1] The static characteristics are guaranteed from $V_{CC} = 1.2$ V to $V_{CC} = 5.5$ V, but LV devices are guaranteed to function down to $V_{CC} = 1.0$ V (with input levels GND or V_{CC}).

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to 85 °C			−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	V_{CC}	0.6	-	V_{CC}	-	V
		V_{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	0.4	GND	-	GND	V
		V_{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; all pins						
		I_O = −100 μA; V_{CC} = 1.2 V	-	1.2	-	-	-	V
		I_O = −100 μA; V_{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		I_O = −100 μA; V_{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		I_O = −100 μA; V_{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		V_I = V_{IH} or V_{IL}; pins QPn						
		I_O = −6 mA; V_{CC} = 3.0 V	2.40	2.82	-	2.20	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; all pins						
		I_O = 100 μA; V_{CC} = 1.2 V	-	0	-	-	-	V
		I_O = 100 μA; V_{CC} = 2.0 V	-	0	0.2	-	0.2	V
		I_O = 100 μA; V_{CC} = 2.7 V	-	0	0.2	-	0.2	V
		I_O = 100 μA; V_{CC} = 3.0 V	-	0	0.2	-	0.2	V
		V_I = V_{IH} or V_{IL}; pins QPn						
		I_O = 6 mA; V_{CC} = 3.0 V	-	0.25	0.40	-	0.50	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 3.6 V	-	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 3.6 V	-	-	±5.0	-	±10.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 3.6 V	-	-	20.0	-	160	μA
ΔI_{CC}	additional supply current	per input; V_I = V_{CC} − 0.6 V; V_{CC} = 2.7 V to 3.6 V	-	-	500.0	-	850	μA
C_I	input capacitance		-	3.5	-			pF

[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 12.

Symbol	Parameter	Conditions		−40 °C to 85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	CP to QS1; see Figure 8	[3]						
		V_{CC} = 1.2 V		-	90	-	-	-	ns
		V_{CC} = 2.0 V		-	31	58	-	70	ns
		V_{CC} = 2.7 V		-	23	43	-	51	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	-	17	34	-	41	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	14	-	-	-	ns
		CP to QS2; see Figure 8	[3]						
		V_{CC} = 1.2 V		-	80	-	-	-	ns
		V_{CC} = 2.0 V		-	27	51	-	61	ns
		V_{CC} = 2.7 V		-	20	38	-	45	ns
		V_{CC} = 3.0 V to 3.6 V		-	14	30	-	36	ns
		V_{CC} = 3.3 V; C_L = 15 pF	[2]	-	13	-	-	-	ns
		CP to QPn; see Figure 8	[3]						
		V_{CC} = 1.2 V		-	115	-	-	-	ns
		V_{CC} = 2.0 V		-	39	75	-	90	ns
		V_{CC} = 2.7 V		-	29	55	-	66	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	-	22	44	-	53	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	18	-	-	-	ns
		STR to QPn; see Figure 9	[3]						
		V_{CC} = 1.2 V		-	105	-	-	-	ns
		V_{CC} = 2.0 V		-	36	68	-	82	ns
		V_{CC} = 2.7 V		-	26	50	-	60	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	-	20	40	-	48	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	17	-	-	-	ns
t_{en}	enable time	OE to QPn; see Figure 11	[4]						
		V_{CC} = 1.2 V		-	100	-	-	-	ns
		V_{CC} = 2.0 V		-	34	65	-	77	ns
		V_{CC} = 2.7 V		-	25	48	-	56	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	-	19	38	-	45	ns
t_{dis}	disable time	OE to QPn; see Figure 11	[5]						
		V_{CC} = 1.2 V		-	65	-	-	-	ns
		V_{CC} = 2.0 V		-	24	40	-	49	ns
		V_{CC} = 2.7 V		-	18	32	-	37	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	-	14	26	-	30	ns

Table 7. Dynamic characteristics *...continued*
Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 12.

Symbol	Parameter	Conditions		−40 °C to 85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_W	pulse width	CP HIGH or LOW; see Figure 8							
		V_{CC} = 2.0 V		34	9	-	41	-	ns
		V_{CC} = 2.7 V		25	6	-	30	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	20	5	-	24	-	ns
		STR HIGH; see Figure 9							
		V_{CC} = 2.0 V		34	9	-	41	-	ns
		V_{CC} = 2.7 V		25	6	-	30	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	20	5	-	24	-	ns
t_{su}	set-up time	D to CP; see Figure 10							
		V_{CC} = 1.2 V		-	25	-	-	-	ns
		V_{CC} = 2.0 V		22	9	-	26	-	ns
		V_{CC} = 2.7 V		16	6	-	19	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	13	5	-	15	-	ns
		CP to STR; see Figure 9							
		V_{CC} = 1.2 V		-	50	-	-	-	ns
		V_{CC} = 2.0 V		43	17	-	51	-	ns
		V_{CC} = 2.7 V		31	13	-	38	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	25	10	-	30	-	ns
t_h	hold time	D to CP; see Figure 10							
		V_{CC} = 1.2 V		-	−10	-	-	-	ns
		V_{CC} = 2.0 V		5	−4	-	+5	-	ns
		V_{CC} = 2.7 V		5	−3	-	+5	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	5	−2	-	+5	-	ns
		CP to STR; see Figure 9							
		V_{CC} = 1.2 V		-	−25	-	-	-	ns
		V_{CC} = 2.0 V		5	−9	-	+5	-	ns
		V_{CC} = 2.7 V		5	−6	-	+5	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	5	−5	-	+5	-	ns
f_{max}	maximum frequency	CP; see Figure 8							
		V_{CC} = 2.0 V		14	52	-	12	-	MHz
		V_{CC} = 2.7 V		19	70	-	16	-	MHz
		V_{CC} = 3.0 V to 3.6 V		24	87	-	20	-	MHz
		V_{CC} = 3.3 V; C_L = 15 pF	[2]	-	95	-	-	-	MHz

Table 7. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 12.

Symbol	Parameter	Conditions		−40 °C to 85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC}	[7]	-	83	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] All typical values are measured at V_{CC} = 3.3 V.

[3] t_{pd} is the same as t_{PLH} and t_{PHL}.

[4] t_{en} is the same as t_{PZH} and t_{PZL}.

[5] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[6] t_t is the same as t_{THL} and t_{TLH}.

[7] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

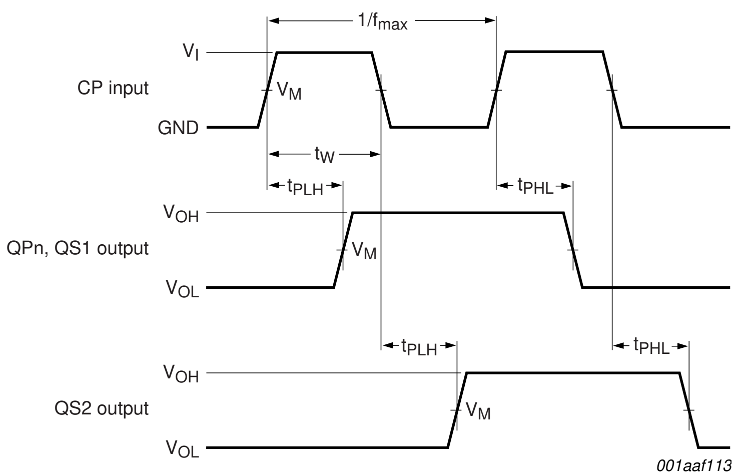
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

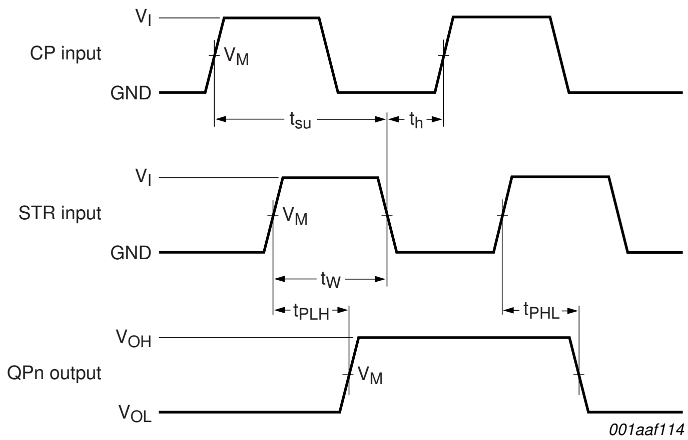
12. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

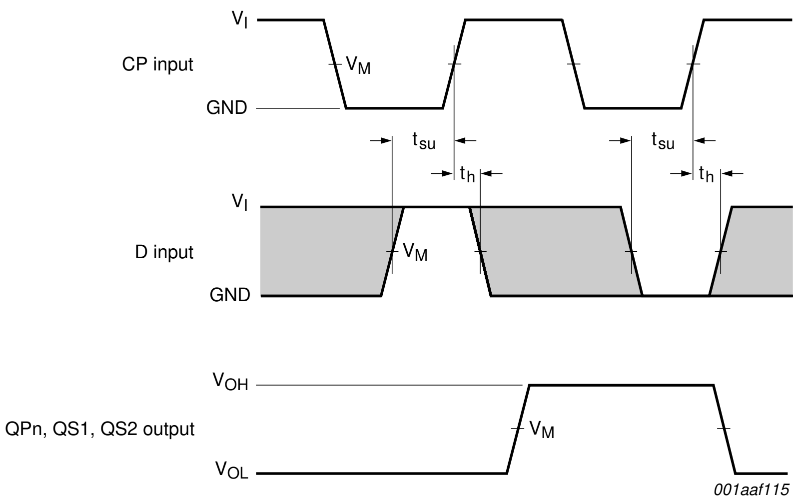
Fig 8. Propagation delay input (CP) to output (QPn, QS1, QS2), output transition time, clock input (CP) pulse width and the maximum frequency (CP)



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

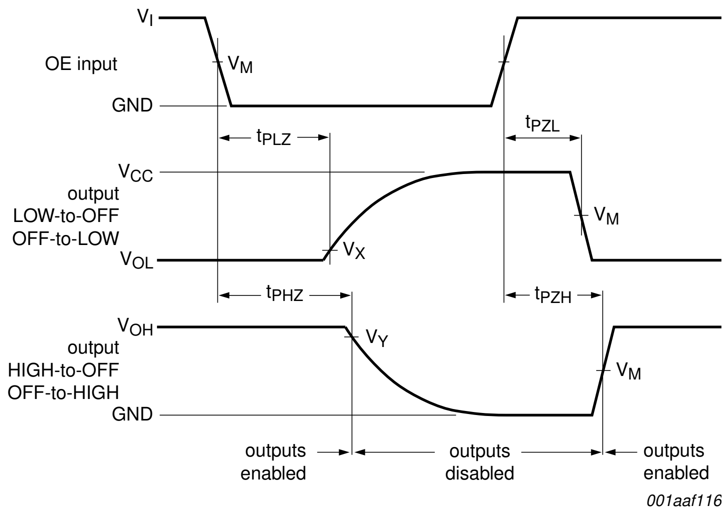
Fig 9. Propagation delay strobe input (STR) to output (QPn), strobe input (STR) pulse width and the clock set-up and hold times for strobe input



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 10. The data input (D) to clock input (CP) set-up times and clock input (CP) to data input (D) hold times



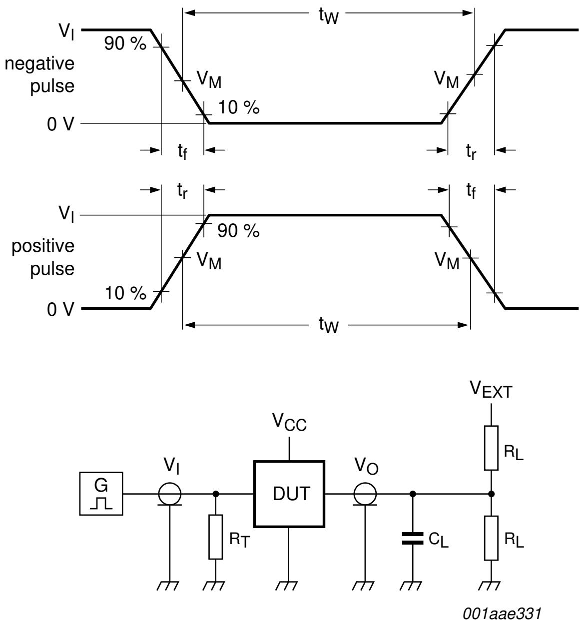
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 11. Enable and disable times

Table 8. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

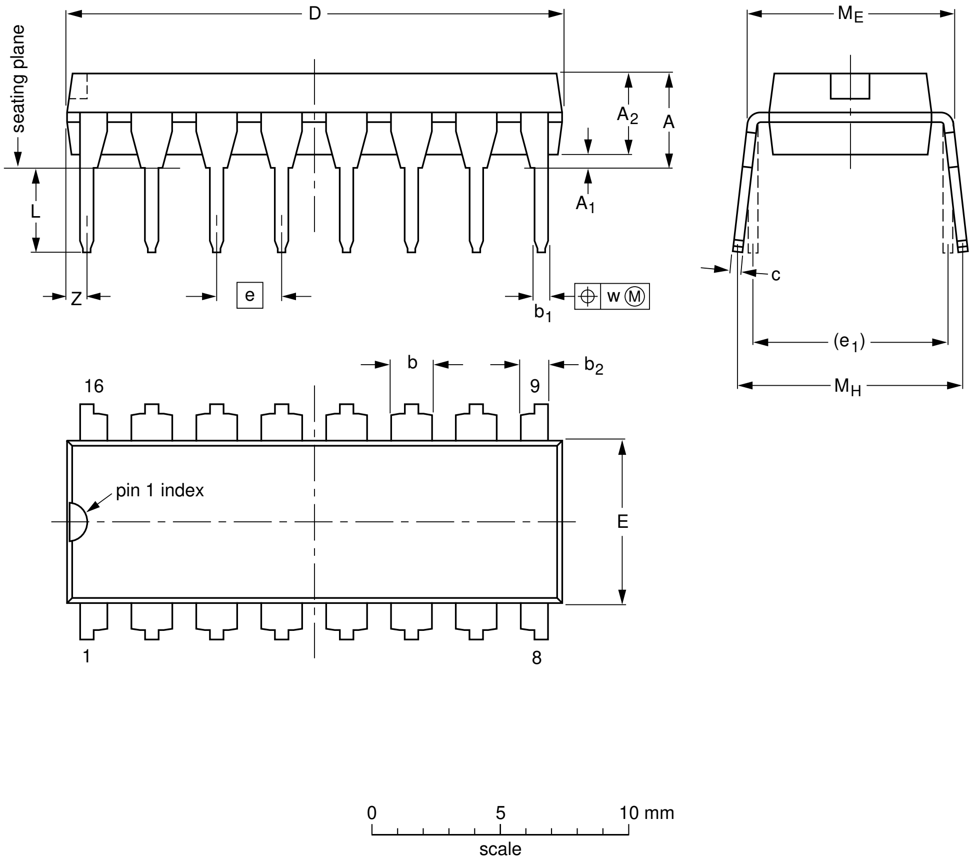
Fig 12. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
< 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	open	GND	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	15 pF, 50 pF	1 kΩ	open	GND	$2V_{CC}$

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D [1]	E [1]	e	e_1	L	M_E	M_H	w	Z [1] max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

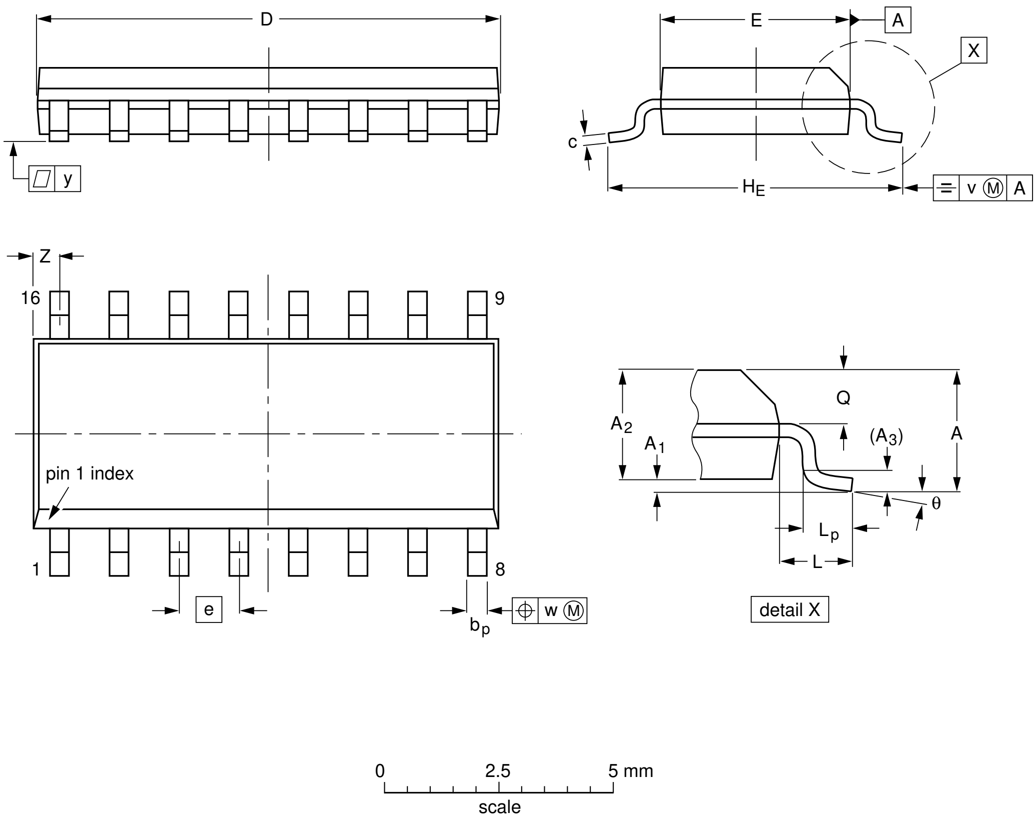
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 13. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

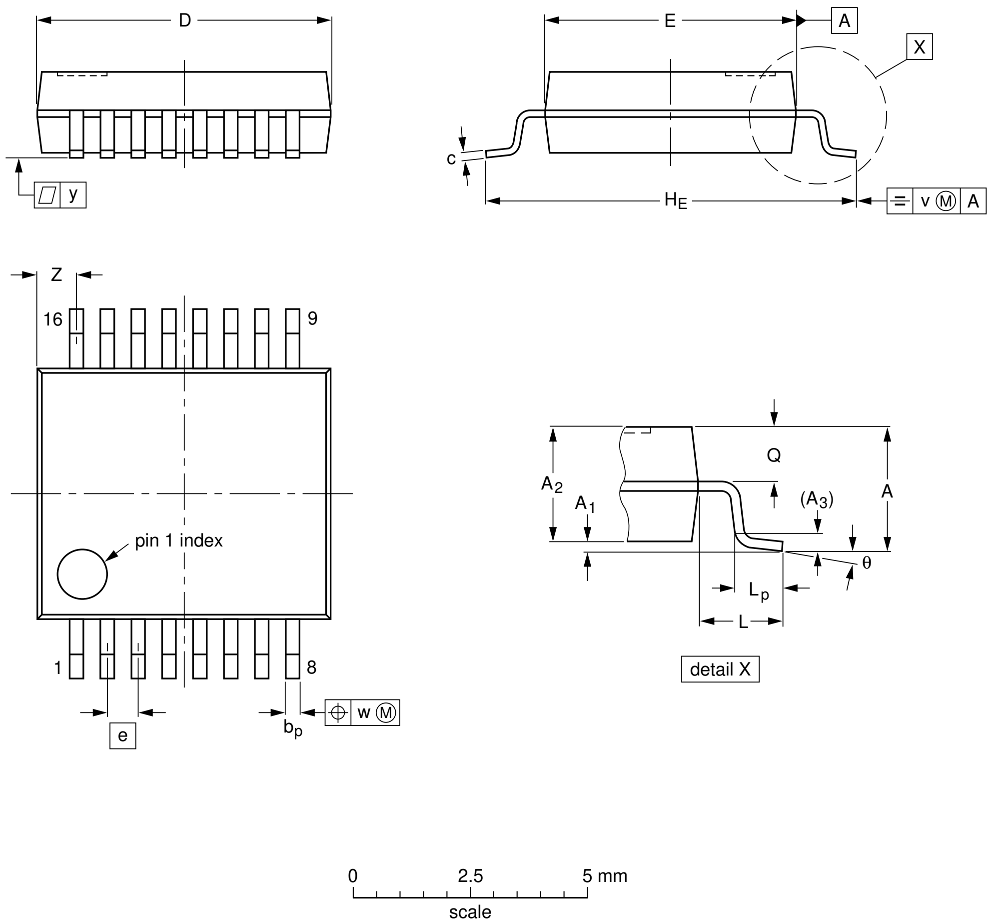
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 14. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

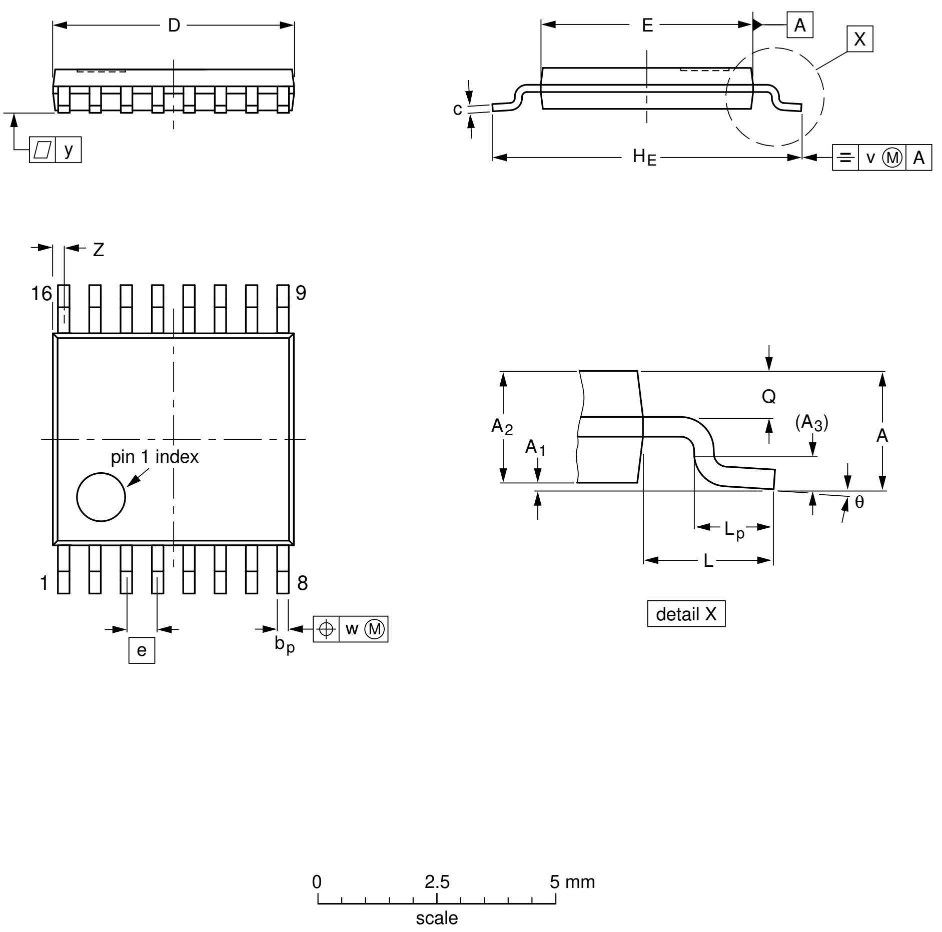
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 15. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 16. Package outline SOT403-1 (TSSOP16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV4094 v.4	20111219	Product data sheet	-	74LV4094 v.3
Modifications:	• Legal pages updated.			
74LV4094 v.3	20110307	Product data sheet	-	74LV4094 v.2
74LV4094 v.2	20060629	Product data sheet	-	74LV4094 v.1
74LV4094 v.1	19980623	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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Date of release: 19 December 2011

Document identifier: 74LV4094