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74LVC1G98

Low-power configurable multiple function gate Rev. 4 — 19 December 2016

Product data sheet

General description 1.

The 74LVC1G98 is a configurable multiple function gate with Schmitt-trigger inputs. The device can be configured as any of the following logic functions MUX, AND, OR, NAND, NOR, inverter and buffer; using the 3-bit input. All inputs can be connected to V_{CC} or GND.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. **Features and benefits**

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8B/JESD36 (2.7 V to 3.6 V).
- \blacksquare ±24 mA output drive (V_{CC} = 3.0 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101E exceeds 1000 V
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C.



Low-power configurable multiple function gate

3. Ordering information

Table 1. Ordering information

Type number	Package						
	Temperature range	Name	Description	Version			
74LVC1G98GW	-40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363			
74LVC1G98GV	-40 °C to +125 °C	SC-74	plastic surface mounted package; 6 leads	SOT457			
74LVC1G98GM	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body $1 \times 1.45 \times 0.5$ mm	SOT886			
74LVC1G98GF	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body $1 \times 1 \times 0.5$ mm	SOT891			
74LVC1G98GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $0.9 \times 1.0 \times 0.35$ mm	SOT1115			
74LVC1G98GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $1.0 \times 1.0 \times 0.35$ mm	SOT1202			

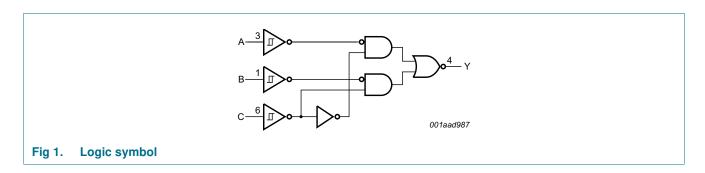
4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74LVC1G98GW	V9
74LVC1G98GV	V98
74LVC1G98GM	V9
74LVC1G98GF	V9
74LVC1G98GN	V9
74LVC1G98GS	V9

^[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

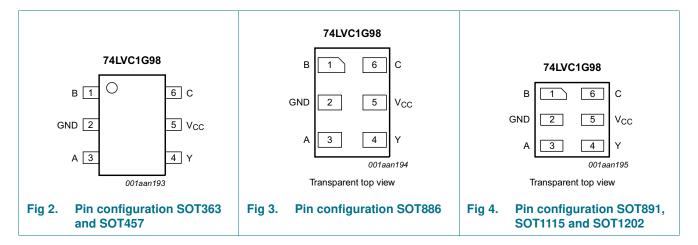
5. Functional diagram



Low-power configurable multiple function gate

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
В	1	data input
GND	2	ground (0 V)
A	3	data input
Υ	4	data output
V _{CC}	5	supply voltage
С	6	data input

7. Functional description

Table 4. Function table[1]

Input	Output		
С	В	A	Υ
L	L	L	Н
L	L	Н	Н
L	Н	L	L
L	Н	Н	L
Н	L	L	Н
Н	L	Н	L
Н	Н	L	Н
Н	Н	Н	L

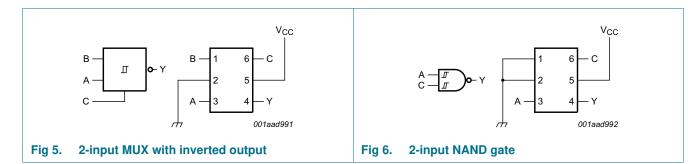
[1] H = HIGH voltage level; L = LOW voltage level.

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7.1 Logic configurations

Table 5. Function selection table

Logic function	Figure
2-input MUX with inverted output	see Figure 5
2-input NAND	see Figure 6
2-input NOR with one input inverted	see Figure 7
2-input AND with one input inverted	see Figure 7
2-input NAND with one input inverted	see Figure 8
2-input OR with one input inverted	see Figure 8
2-input NOR	see Figure 9
Buffer	see Figure 10
Inverter	see Figure 11



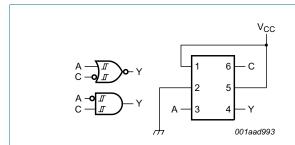


Fig 7. 2-input AND gate with input A inverted or 2-input NOR gate with inverted C input

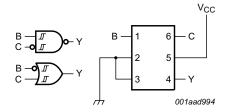
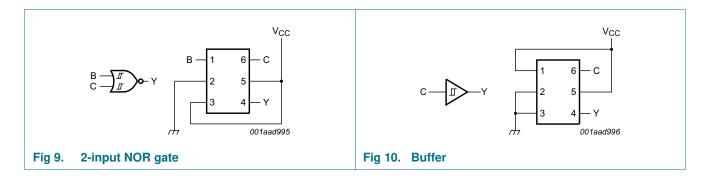
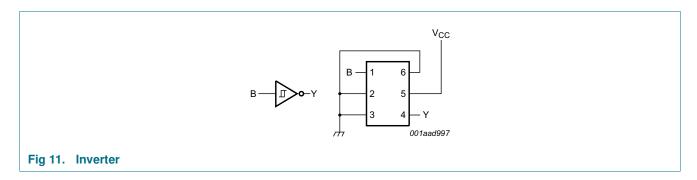


Fig 8. 2-input OR gate with input B inverted or 2-input NAND gate with input C inverted



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8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V		-50	-	mA
VI	input voltage		[1]	-0.5	+6.5	V
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
Vo	output voltage	Active mode	[1][2]	-0.5	+6.5	V
		Power-down mode	[1][2]	-0.5	+6.5	V
I _O	output current	$V_O = 0 \text{ V to } V_{CC}$		-	±50	mA
I _{CC}	supply current			-	+100	mA
I _{GND}	ground current			-100	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	[3]	-	250	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	٧
VI	input voltage		0	-	5.5	٧
Vo	output voltage	Active mode	0	-	V_{CC}	٧
		V _{CC} = 0 V; Power-down mode	0	-	5.5	٧
T _{amb}	ambient temperature		-40	-	+125	°C

^[2] When $V_{CC} = 0 \text{ V}$ (Power-down mode), the output voltage can be 5.5 V in normal operation.

^[3] For SC-88 and SC-74 packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K. For XSON6 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

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10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	r Conditions	-40	°C to +85	°C	-40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
V _{OL}	LOW-level	V _I = V _{CC} or GND						
	output voltage	$I_O = 100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	-	0.1	-	0.1	V
		$I_O = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.45	-	0.7	V
		$I_{O} = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.3	-	0.45	V
		$I_O = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	-	0.4	-	0.6	V
		$I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	-	0.8	V
		$I_O = 32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.55	-	0.8	٧
V _{OH}	HIGH-level	$V_I = V_{CC}$ or GND						
	output voltage	$I_O = -100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	V _{CC} - 0.1	-	-	V _{CC} - 0.1	-	V
		$I_{O} = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.2	-	-	0.95	-	٧
		$I_{O} = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.9	-	-	1.7	-	٧
		$I_{O} = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	-	-	1.9	-	٧
		$I_{O} = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.3	-	-	2.0	-	٧
		$I_O = -32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.8	-	-	3.4	-	٧
l _l	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	±0.1	±1	-	±1	μА
I _{OFF}	power-off leakage current	V_{I} or $V_{O} = 5.5 \text{ V}$; $V_{CC} = 0 \text{ V}$	-	±0.1	±2	-	±2	μА
I _{CC}	supply current	V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V	-	0.1	4	-	4	μΑ
Δl _{CC}	additional supply current	$V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A};$ $V_{CC} = 2.3 \text{ V} \text{ to } 5.5 \text{ V}$	-	5	500	-	500	μА
Cı	input capacitance		-	2.5	-	-	-	pF

^[1] Typical values are measured at maximum V_{CC} and T_{amb} = 25 °C.

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11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 13.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to	C to +125 °C U	
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	A, B, C to Y; see Figure 12						
		V _{CC} = 1.65 V to 1.95 V	1.0	6.0	14.4	1.0	18.0	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	3.5	8.3	0.5	10.4	ns
		V _{CC} = 2.7 V	0.5	4.2	8.5	0.5	10.6	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	3.8	6.3	0.5	7.9	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	3.0	5.1	0.5	6.4	ns
C _{PD}	power dissipation capacitance	$V_{CC} = 3.3 \text{ V}; V_I = \text{GND to } V_{CC}$ [3]	-	20	-	-	-	pF

- [1] Typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}{}^2 \times f_o) \text{ where:}$

 f_i = input frequency in MHz;

fo = output frequency in MHz;

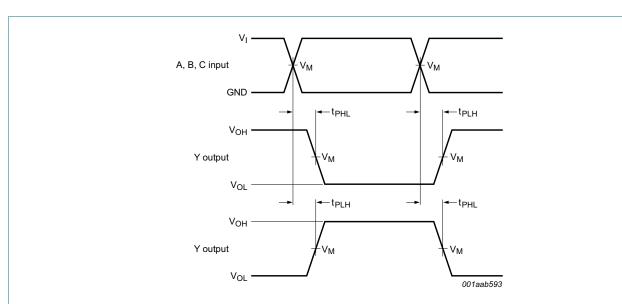
C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}{}^2 \times f_o) = sum \ of \ outputs.$

12. Waveforms



Measurement points are given in Table 10.

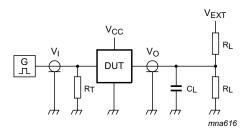
 $\ensuremath{V_{\text{OL}}}$ and $\ensuremath{V_{\text{OH}}}$ are typical output voltage levels that occur with the output load.

Fig 12. Input A, B and C to output Y propagation delay times

Low-power configurable multiple function gate

Table 10. Measurement points

Supply voltage	Input	Input	
V _{CC}	V _M	VI	V _M
1.65 V to 1.95 V	0.5V _{CC}	V _{CC}	0.5V _{CC}
2.3 V to 2.7 V	0.5V _{CC}	V _{CC}	0.5V _{CC}
2.7 V	1.5 V	2.7 V	1.5 V
3.0 V to 3.6 V	1.5 V	2.7 V	1.5 V
4.5 V to 5.5 V	0.5V _{CC}	V _{CC}	0.5V _{CC}



Measurement points are given in <u>Table 11</u>.

Definitions test circuit:

 R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig 13. Test circuit for measuring switching times

Table 11. Measurement points

Supply voltage	Input		Load	V _{EXT}	
V _{CC}	VI	$t_r = t_f$	CL	R _L	t _{PLH} , t _{PHL}
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open

Low-power configurable multiple function gate

13. Transfer characteristics

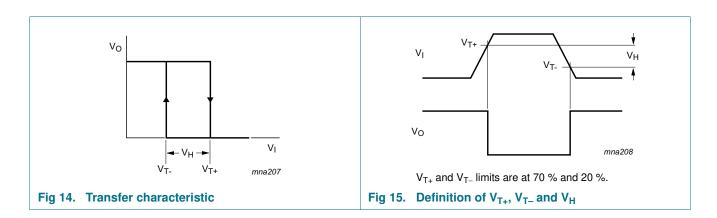
Table 12. Transfer characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

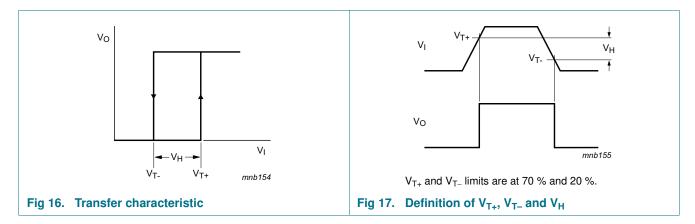
Symbol	Parameter	Conditions	-40	-40 °C to +85 °C			-40 °C to +125 °C		
			Min	Typ[1]	Max	Min	Max		
V_{T+}	positive-going threshold voltage	see Figure 14, Figure 15, Figure 16 and Figure 17							
		V _{CC} = 1.8 V	0.70	1.02	1.20	0.67	1.20	V	
		V _{CC} = 2.3 V	1.11	1.42	1.60	1.08	1.60	V	
		V _{CC} = 3.0 V	1.50	1.79	2.00	1.47	2.00	V	
		V _{CC} = 4.5 V	2.16	2.52	2.74	2.13	2.74	V	
		V _{CC} = 5.5 V	2.61	2.99	3.33	2.58	3.33	V	
V_{T-}	negative-going threshold voltage	see Figure 14, Figure 15, Figure 16 and Figure 17							
		V _{CC} = 1.8 V	0.30	0.53	0.72	0.30	0.75	٧	
		V _{CC} = 2.3 V	0.58	0.77	1.00	0.58	1.03	٧	
		V _{CC} = 3.0 V	0.80	1.04	1.30	0.80	1.33	V	
		V _{CC} = 4.5 V	1.21	1.55	1.90	1.21	1.93	V	
		V _{CC} = 5.5 V	1.45	1.86	2.29	1.45	2.32	V	
V _H	hysteresis voltage	(V _{T+} – V _{T-}) See <u>Figure 14</u> , <u>Figure 15</u> , <u>Figure 16</u> and <u>Figure 17</u>							
		V _{CC} = 1.8 V	0.30	0.48	0.62	0.23	0.62	V	
		V _{CC} = 2.3 V	0.40	0.64	0.80	0.34	0.80	V	
		V _{CC} = 3.0 V	0.50	0.75	1.00	0.44	1.00	V	
		V _{CC} = 4.5 V	0.71	0.97	1.20	0.65	1.20	V	
		V _{CC} = 5.5 V	0.71	1.13	1.40	0.65	1.40	V	

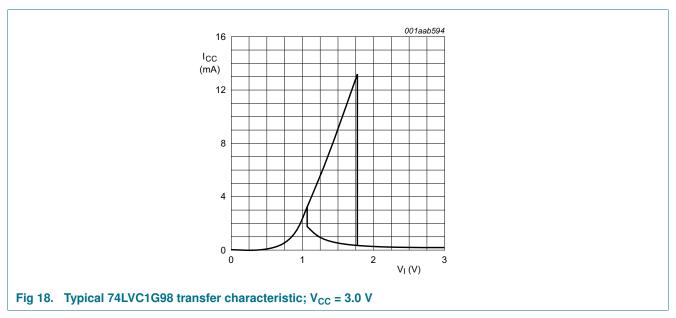
^[1] Typical values are measured at T_{amb} = 25 °C.

14. Waveforms transfer characteristics



Low-power configurable multiple function gate





Low-power configurable multiple function gate

15. Package outline

Plastic surface-mounted package; 6 leads

SOT363

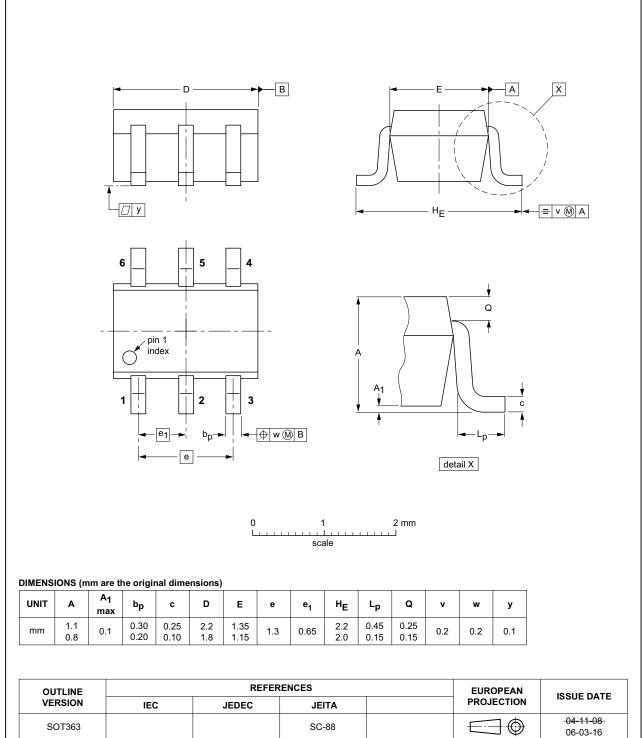


Fig 19. Package outline SOT363 (SC-88)

Low-power configurable multiple function gate

Plastic surface-mounted package (TSOP6); 6 leads **SOT457** В Α = v (M) A 6 pin 1 index 3 2 - | w M B detail X scale **DIMENSIONS** (mm are the original dimensions) UNIT Ε Q ΗE $L_{\mathbf{p}}$ 0.1 0.26 0.10 3.1 2.7 1.7 3.0 2.5 0.33 0.23 1.1 0.40 0.6 0.95 0.2 0.2 0.1 mm 0.013 0.25 1.3 0.9 REFERENCES **EUROPEAN** OUTLINE ISSUE DATE **PROJECTION** VERSION IEC JEDEC JEITA 05-11-07 06-03-16 SOT457 SC-74 $\exists \, \oplus$

Fig 20. Package outline SOT457 (SC-74)

Low-power configurable multiple function gate

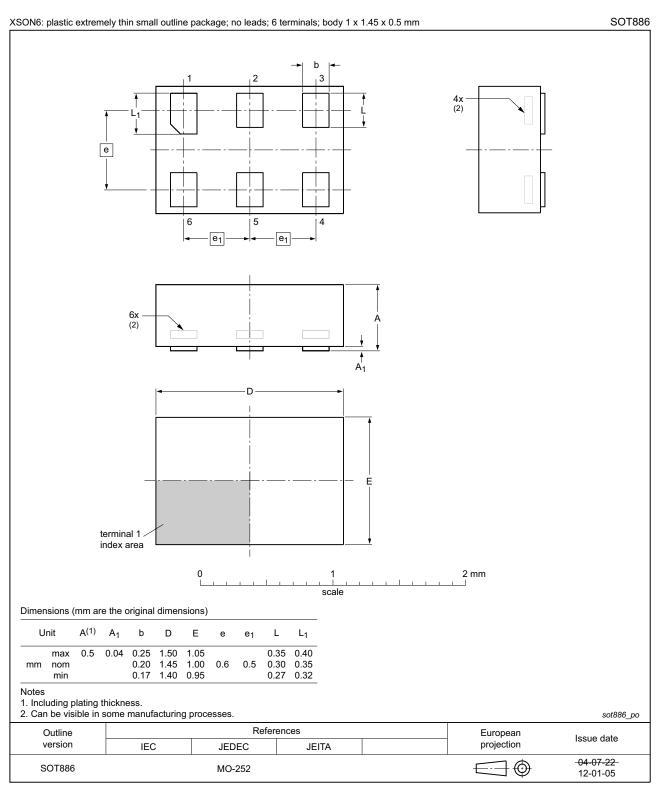


Fig 21. Package outline SOT886 (XSON6)

Low-power configurable multiple function gate

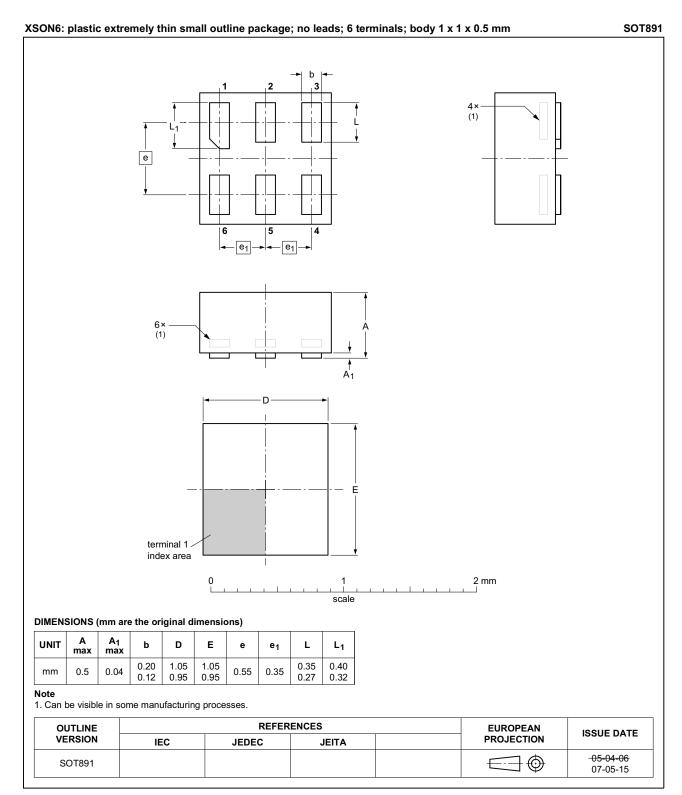


Fig 22. Package outline SOT891 (XSON6)

Low-power configurable multiple function gate

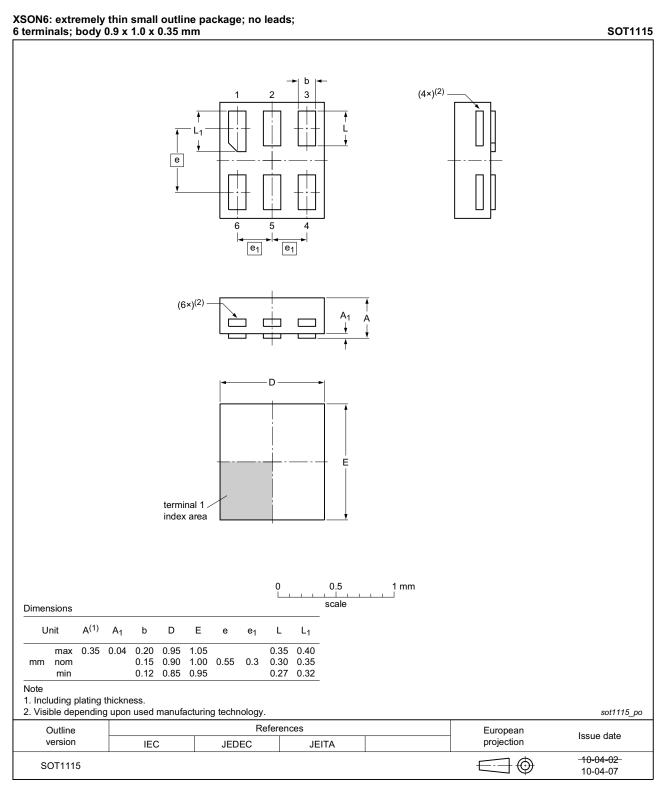


Fig 23. Package outline SOT1115 (XSON6)

Low-power configurable multiple function gate

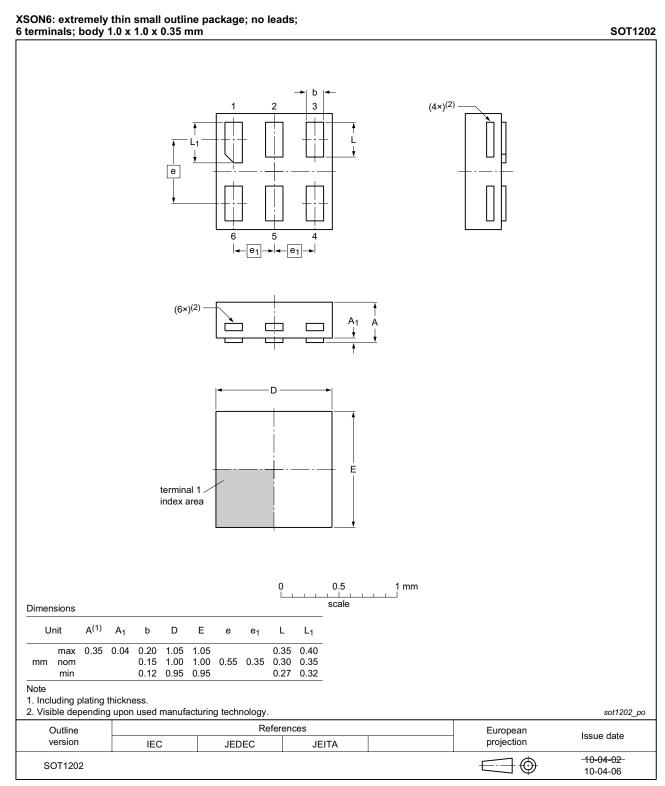


Fig 24. Package outline SOT1202 (XSON6)

Low-power configurable multiple function gate

16. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
TTL	Transistor-Transistor Logic
HBM	Human Body Model
ESD	ElectroStatic Discharge
MM	Machine Model
DUT	Device Under Test

17. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G98 v.4	20161219	Product data sheet	-	74LVC1G98 v.3
Modifications:	• Table 8: The r	maximum limits for leakage cui	rent and supply cur	rent have changed.
74LVC1G98 v.3	20111201	Product data sheet	-	74LVC1G98 v.2
74LVC1G98 v.2	20111201	Product data sheet	-	74LVC1G98 v.1
74LVC1G98 v.1	20101221	Product data sheet	-	-

Low-power configurable multiple function gate

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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