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74LVC2952A

Octal registered transceiver with 5 V tolerant inputs/outputs; 3-state

Rev. 02 — 29 June 2004 Product data sheet

1. General description

The 74LVC2952A is a high-performance, low power, low voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices as translators in a mixed 3.3 V and 5 V environment.

The 74LVC2952A is an octal non-inverting registered transceiver. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the clock (CPAB, CPBA) provided that the clock enable ($\overline{CEAB}$, $\overline{CEBA}$) input is LOW. The data is then present at the 3-state output buffers, but is only accessible when the output enable ($\overline{OEAB}$, $\overline{OEBA}$) input is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

2. Features

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Flow-through pin-out architecture
- Complies with JEDEC standard JESD8-B/JESD36
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C.

PHILIPS

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay CPAB, CPBA to An, Bn	C_L = 50 pF; V_{CC} = 3.3 V		-	3.6	-	ns
f_{max}	maximum clock frequency	C_L = 50 pF; V_{CC} = 3.3 V		-	250	-	MHz
C_I	input capacitance			-	5.0	-	pF
$C_{I/O}$	input/output capacitance			-	10.0	-	pF
C_{PD}	power dissipation capacitance per latch	outputs enabled; V_{CC} = 3.3 V	[1] [2]	-	15.0	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC2952AD	–40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74LVC2952ADB	–40 °C to +125 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74LVC2952APW	–40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

5. Functional diagram

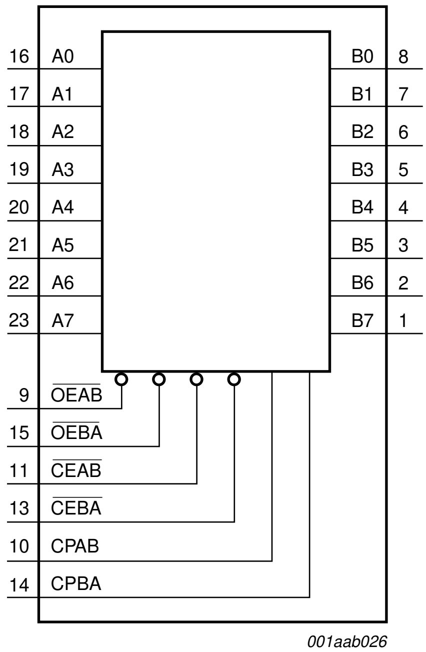


Fig 1. Functional diagram.

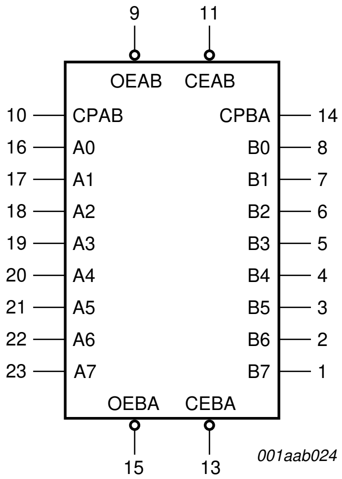


Fig 2. Logic symbol.

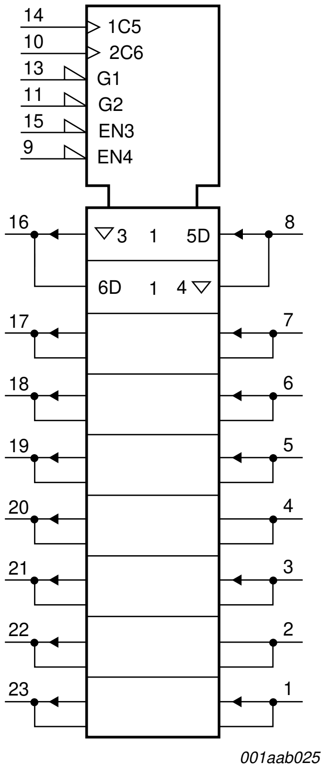


Fig 3. IEC logic symbol.

6. Pinning information

6.1 Pinning

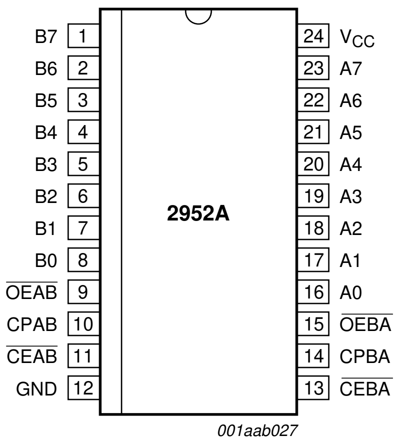


Fig 4. Pin configuration.

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
B7	1	B data input/output
B6	2	B data input/output
B5	3	B data input/output
B4	4	B data input/output
B3	5	B data input/output
B2	6	B data input/output
B1	7	B data input/output
B0	8	B data input/output
$\overline{OEAB}$	9	A to B output enable input (active LOW)
CPAB	10	A to B clock input (LOW-to-HIGH, edge-triggered)
$\overline{CEAB}$	11	A to B clock enable input (active LOW)
GND	12	ground (0 V)
$\overline{CEBA}$	13	B to A clock enable input (active LOW)
CPBA	14	B to A clock input (LOW-to-HIGH, edge-triggered)
$\overline{OEBA}$	15	B to A output enable input (active LOW)
A0	16	A data input/output
A1	17	A data input/output
A2	18	A data input/output
A3	19	A data input/output
A4	20	A data input/output
A5	21	A data input/output
A6	22	A data input/output
A7	23	A data input/output
V_{CC}	24	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table for register An or Bn [1]

Operating mode	Input			Internal latch
	An or Bn	CPxx	$\overline{CExx}$	
Hold data	X	X	H	NC
Load data	L	↑	L	L
Load data	H	↑	L	H

Table 5: Function table for output enable [1]

Operating mode	Input $\overline{OExx}$	Internal latch	Output An or Bn
Disable outputs	H	X	Z
Enable outputs	L	L	L
Enable outputs	L	H	H

[1] H = HIGH voltage level;
L = LOW voltage level;
Z = high-impedance OFF-state;
NC = no change;
X = don't care;
↑ = LOW-to-HIGH level transition.

8. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$ V		-	−50	mA
V_I	input voltage		[1]	−0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	output HIGH or LOW state	[1]	−0.5	V_{CC} + 0.5	V
		output 3-state	[1]	−0.5	+6.5	V
I_O	output source or sink current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±100	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	power dissipation	T_{amb} = −40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO24 packages: above 70 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For T(SSOP)24 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

9. Recommended operating conditions

Table 7: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	for maximum speed performance	2.7	-	3.6	V
		for low-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	operating ambient temperature	in free air	−40	-	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

10. Static characteristics

Table 8: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]							
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V		V_{CC}	-	-	V
		V_{CC} = 2.7 V to 3.6 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V		-	-	GND	V
		V_{CC} = 2.7 V to 3.6 V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 μA; V_{CC} = 2.7 V to 3.6 V	[2]	V_{CC} − 0.2	V_{CC}	-	V
		I_O = −12 mA; V_{CC} = 2.7 V		V_{CC} − 0.5	-	-	V
		I_O = −18 mA; V_{CC} = 3.0 V		V_{CC} − 0.6	-	-	V
		I_O = −24 mA; V_{CC} = 3.0 V		V_{CC} − 0.8	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA; V_{CC} = 2.7 V to 3.6 V	[2]	-	GND	0.2	V
		I_O = 12 mA; V_{CC} = 2.7 V		-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V		-	-	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 3.6 V		-	±0.1	±5	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND; V_{CC} = 3.6 V	[3]	-	0.1	±10	μA
I_{off}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V		-	0.1	±10	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 3.6 V		-	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per pin	V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 2.7 V to 3.6 V	[2]	-	5	500	μA
C_I	input capacitance			-	5.0	-	pF
$C_{I/O}$	input/output capacitance			-	10.0	-	pF

Table 8: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C							
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V		V_{CC}	-	-	V
		V_{CC} = 2.7 V to 3.6 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V		-	-	0	V
		V_{CC} = 2.7 V to 3.6 V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 μA; V_{CC} = 2.7 V to 3.6 V		V_{CC} − 0.3	-	-	V
		I_O = −12 mA; V_{CC} = 2.7 V		V_{CC} − 0.65	-	-	V
		I_O = −18 mA; V_{CC} = 3.0 V		V_{CC} − 0.75	-	-	V
		I_O = −24 mA; V_{CC} = 3.0 V		V_{CC} − 1	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA; V_{CC} = 2.7 V to 3.6 V		-	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.7 V		-	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V		-	-	0.8	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 3.6 V		-	-	±20	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND; V_{CC} = 3.6 V	[3]	-	-	±20	μA
I_{off}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V		-	-	±20	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 3.6 V		-	-	40	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 2.7 V to 3.6 V		-	-	5000	μA

[1] All typical values are measured at T_{amb} = 25 °C.

[2] These typical values are measured at V_{CC} = 3.3 V.

[3] For transceivers, the parameter I_{OZ} includes the input leakage current.

11. Dynamic characteristics

Table 9: Dynamic characteristics

GND = 0 V; see Figure 8 for test circuit.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]							
t_{PHL}, t_{PLH}	propagation delay CPBA, CPAB to An and Bn	see Figure 5					
		V_{CC} = 1.2 V		-	16	-	ns
		V_{CC} = 2.7 V		1.5	4.4	8.6	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.5	3.6	7.6	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OEBA}$, $\overline{OEAB}$ to An and Bn	see Figure 7					
		V_{CC} = 1.2 V		-	16	-	ns
		V_{CC} = 2.7 V		1.5	4.7	8.6	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	3.9	7.6	ns

Table 9: Dynamic characteristics *...continued*

GND = 0 V; see Figure 8 for test circuit.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OEBA}$, $\overline{OEAB}$ to An and Bn	see Figure 7					
		V_{CC} = 1.2 V		-	8	-	ns
		V_{CC} = 2.7 V		1.5	3.8	7.6	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.5	3.4	6.6	ns
t_W	clock pulse width HIGH or LOW CPAB or CPBA	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		3.0	1.5	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	3.0	1.5	-	ns
t_{su}	set-up time HIGH or LOW An, Bn to CPAB, CPBA	see Figure 6					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.7	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	+1.3	−0.5	-	ns
	set-up time HIGH or LOW $\overline{CEAB}$, $\overline{CEBA}$ to CPAB, CPBA	see Figure 6					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.3	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	+1.1	−0.5	-	ns
t_h	hold time An, Bn to CPAB, CPBA	see Figure 6					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.5	0.6	-	ns
	hold time $\overline{CEAB}$, $\overline{CEBA}$ to CPAB, CPBA	see Figure 6					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.4	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	+1.1	−0.6	-	ns
f_{max}	maximum clock pulse frequency	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	MHz
		V_{CC} = 2.7 V		150	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V	[2]	150	250	-	MHz
$t_{sk(0)}$	skew		[3]	-	-	1.0	ns
C_{PD}	power dissipation capacitance per latch	outputs enabled; V_{CC} = 3.3 V	[4] [5]	-	15.0	-	pF
T_{amb} = −40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay CPBA, CPAB to An, Bn	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.5	-	11	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	-	9.5	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OEBA}$, $\overline{OEAB}$ to An, Bn	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.5	-	11	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	-	9.5	ns

Table 9: Dynamic characteristics *…continued*

GND = 0 V; see Figure 8 for test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OEBA}$, $\overline{OEAB}$ to An, Bn	see Figure 7				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.7 V	1.5	-	9.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	-	8.5	ns
t_W	clock pulse width HIGH or LOW CPAB or CPBA	see Figure 5				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.7 V	3.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	3.0	-	-	ns
t_{su}	set-up time HIGH or LOW An, Bn to CPAB, CPBA	see Figure 6				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.7 V	1.7	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.3	-	-	ns
	set-up time HIGH or LOW $\overline{CEAB}$, $\overline{CEBA}$ to CPAB, CPBA	see Figure 6				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.7 V	1.3	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.1	-	-	ns
t_h	hold time An, Bn to CPAB, CPBA	see Figure 6				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.7 V	1.5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	-	-	ns
	hold time $\overline{CEAB}$, $\overline{CEBA}$ to CPAB, CPBA	see Figure 6				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.7 V	1.4	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.1	-	-	ns
f_{max}	maximum clock pulse frequency	see Figure 5				
		V_{CC} = 1.2 V	-	-	-	MHz
		V_{CC} = 2.7 V	150	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V	150	-	-	MHz
$t_{sk(0)}$	skew	[3]	-	-	1.5	ns

[1] All typical values are measured at T_{amb} = 25 °C.

[2] These typical values are measured at V_{CC} = 3.3 V.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

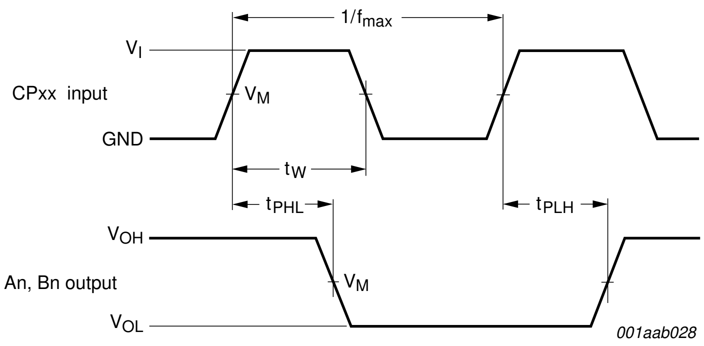
V_{CC} = supply voltage in V;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[5] The condition is V_I = GND to V_{CC}.

12. Waveforms



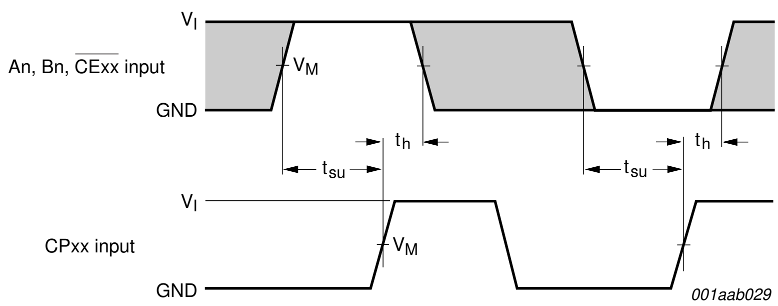
Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 5. Clock input (CPBA, CPAB) to output (An, Bn) propagation delays, the clock pulse width and the maximum clock pulse frequency.

Table 10: Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
< 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
≥ 2.7 V	1.5 V	1.5 V



Measurement points are given in Table 11.

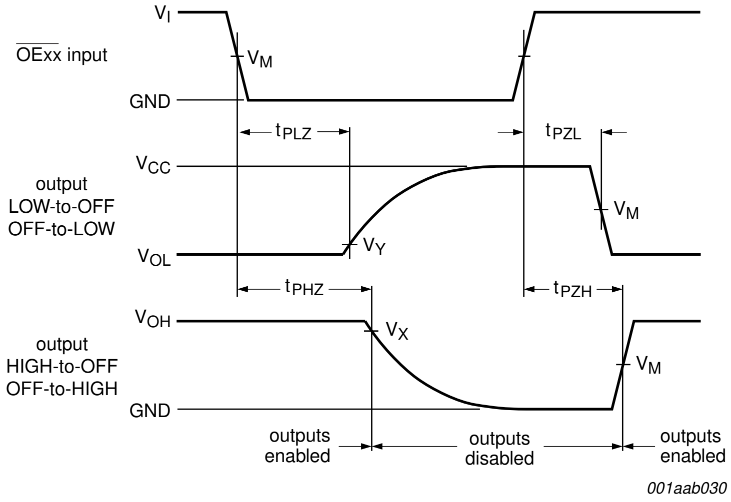
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

The shaded areas indicate when the input is permitted to change for predicable output performance.

Fig 6. Set-up and hold times for the An, Bn and $\overline{CExx}$ inputs.

Table 11: Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
< 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
≥ 2.7 V	1.5 V	1.5 V



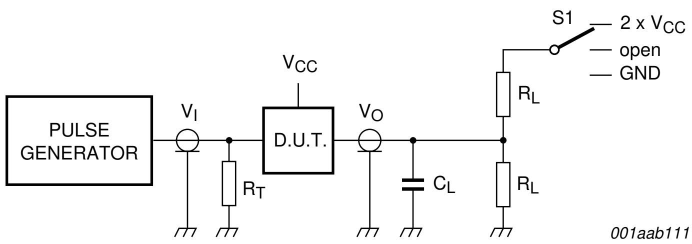
Measurement points are given in Table 12.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 7. 3-state enable and disable times.

Table 12: Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
< 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.1 \times V_{CC}$	$V_{OH} - 0.1 \times V_{CC}$
≥ 2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V



Test data is given in Table 13.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

Fig 8. Load circuitry for switching times.

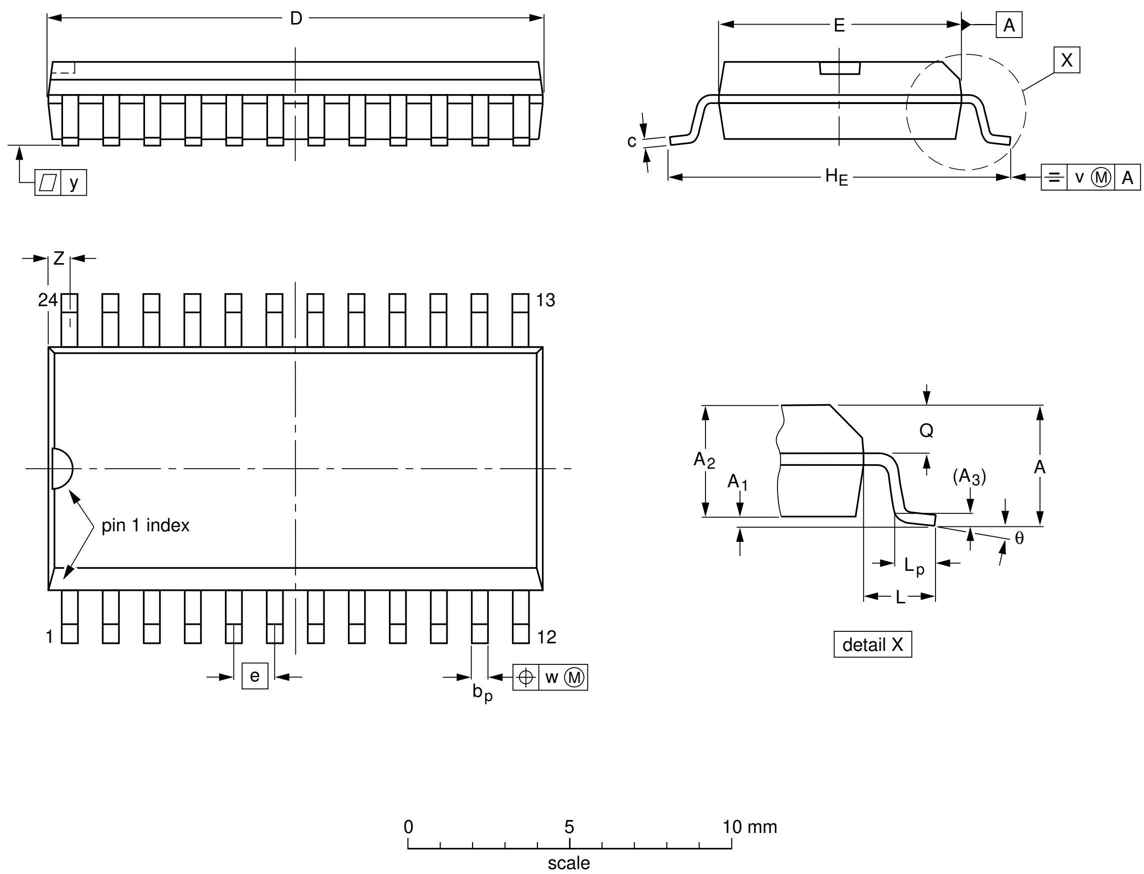
Table 13: Test data

Supply voltage	Input		Load		S1		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.2 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω [1]	open	GND	2 × V_{CC}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	2 × V_{CC}
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	2 × V_{CC}

[1] The circuit performs better when R_L = 1000 Ω.

13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

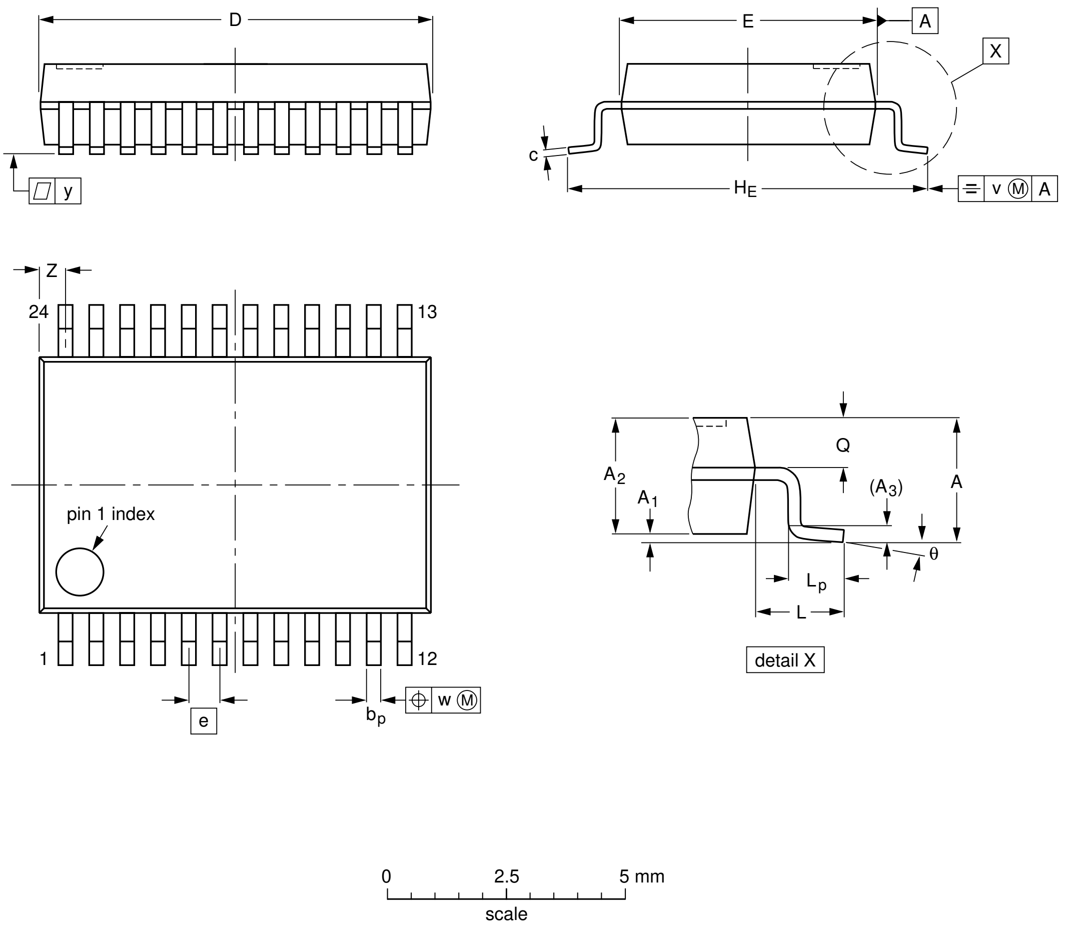
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 9. Package outline SO24.

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

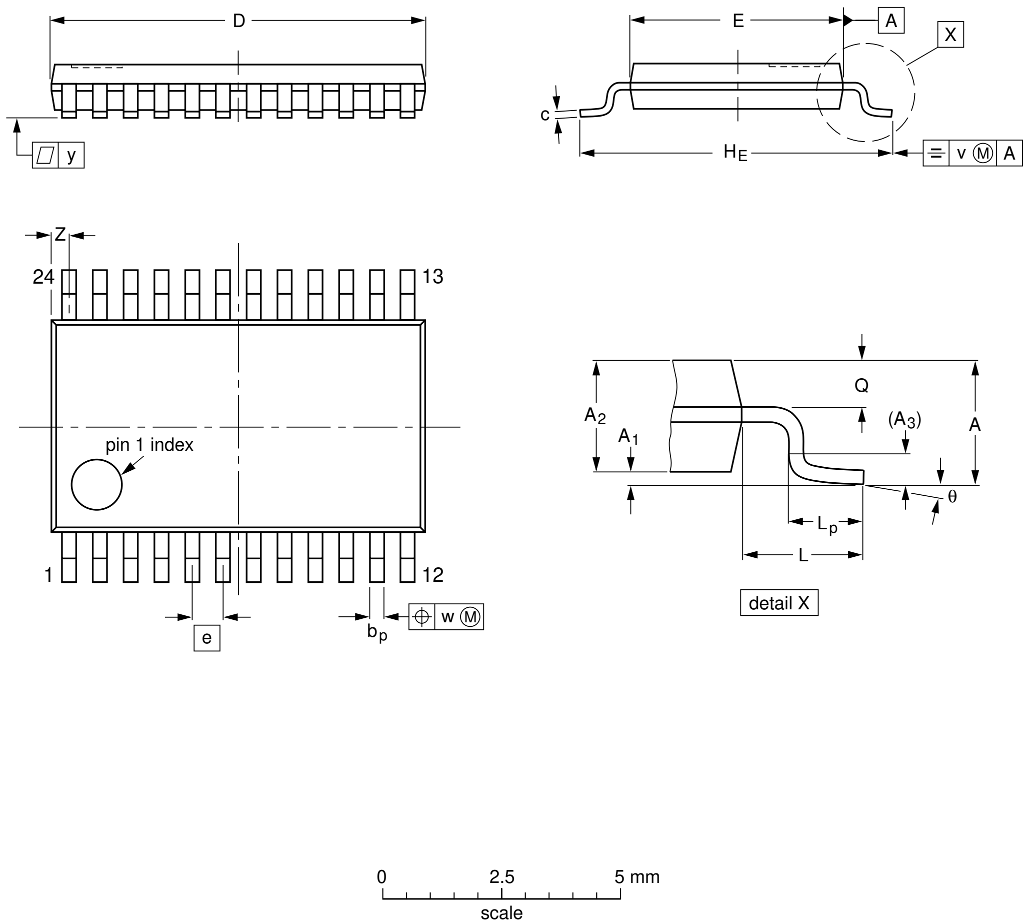
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 10. Package outline SSOP24.

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

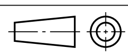
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 11. Package outline TSSOP24.

14. Revision history

Table 14: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
74LVC2952A_2	20040629	Product data sheet	-	9397 750 13251	74LVC2952A_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors • Table 1: changed various values • Table 8: changed maximum value of I_{OZ} from ±5 μA to ±10 μA • Table 8: added values for T_{amb} = −40 °C to +125 °C • Table 9: changed various values • Table 9: added values for T_{amb} = −40 °C to +125 °C.				
74LVC2952A_1	19980729	Product specification	-	9397 750 04524	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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19. Contents

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